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Multilevel Inverter Topology with Reduced Switch Count

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Abstract- Multilevel Inverters have created a new wave of interest in industries and research. While the classical topologies proved to be a viable alternate in wide range of high power medium-voltage applications, there has been an active interest in the evolution of newer topologies. Reduction in overall switch count as compared to the classical topologies has been an important objective in the recently introduced topics. In this paper a new topology for Multilevel inverters is proposed, which reduces the number of switches when compared to previous topologies. In this proposed topology we could able to get seven levels with eight switches, one input source and three input capacitors. We can also enhance the levels to nine level with one more switch adding to the proposed topology and with proper switching sequence. The total circuit configuration is developed in Matlab/simulink software.

Keywords: Multilevel inverters, Types of Multilevel Inverters, Cascaded H-Bridge inverter, PWM Technique.

1.INTRODUCTION

Recent advances in the power-handling capabilities of static switch devices such as IGBTs with voltage rating up to 4.5 kV commercially available, has made the use of the voltage source inverters (VSI) feasible for high-power applications. High power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three phase ac systems. A half-bridge is the simplest topology, which is used to produce a two level square-wave output waveform. A center-tapped voltage source supply is needed in such a topology. It may be possible to use a simple supply with two well-matched capacitors in series to provide the center tap. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs.

Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. The multilevel inverter structures are the main focus of discussion in this chapter; however, the illustrated

structures can be implemented for rectifying operation as well. Although each type of multilevel converters share the advantages of multilevel voltage source inverters, they may be suitable for specific application due to their structures and drawbacks. Operation and structure of some important type of multilevel converters are discussed in the following sections. The purpose of the multilevel topology is to reduce the voltage rating of the power switch. Therefore, it usually is used at high-power application. By combining output voltages in multilevel form, it has advantages of low dv/dt, low input current distortion, and lower switching frequency. As a result of advantages of multilevel topology, several topologies have emerged in recent years [7], [8].

A digital signal processor (DSP) is a specialized microprocessor (or a SIP block), with its architecture optimized for the operational needs of digital signal processing.The goal of DSPs is usually to measure, filter and/or compress continuous real-world analog signals. Most general-purpose microprocessors can also execute digital signal processing algorithms successfully, but dedicated DSPs usually have better power efficiency thus they are more suitable in portable devices such as mobile phones because of power consumption constraints. DSPs often use special memory architectures that are able to fetch multiple data and/or instructions at the same time.

Digital signal processing algorithms typically require a large number of mathematical operations to be performed quickly and repeatedly on a series of data samples. Signals (perhaps from audio or video sensors) are constantly converted from analog to digital, manipulated digitally, and then converted back to analog form. Many DSP applications have constraints on latency; that is, for the system to work, the DSP operation must be completed within some fixed time, and deferred (or batch) processing is not viable.

II. POWER STAGE

A. Circuit Configuration

Fig. 2 shows the proposed novel topology used in the seven level inverter. An input voltage divider is composed of three series capacitors C_1, C_2, and C_3. The divided voltage is transmitted to H-bridge by four MOSFETs, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design.

B.Operating Principles

1)The required seven voltage output levels ($\pm 1/3V_{dc}$, $\pm 2/3V_{dc}$, $\pm V_{dc}$, 0) are generated as follows.

1) To generate a voltage level $V_0 = 1/3V_{dc}$, $S1$ is turned on at the positive half cycle. Energy is provided by the capacitor $C1$ and the voltage across H-bridge is $1/3V$dc. S_5 and S_8 are turned on, and the voltage applied to the load terminals is $1/3V_{dc}$. Fig. 3 shows the current path at this mode.

2)To generate a voltage level $Vo = 2/3V_{dc}$, $S1$ and $S4$ are turned on. Energy is provided by the capacitor $C1$ and $C2$. The voltage across H-bridge is $2/3V_{dc}$. $S5$ and $S8$ are turned on, and the voltage applied to the load terminals is $2/3V$dc. Fig. 4 shows the current path at this mode.

3)To generate a voltage level $V_0 = V_{dc}$, $S1$ and $S2$ are turned on. Energy is provided by the capacitor $C1$, $C2$, and $C3$.

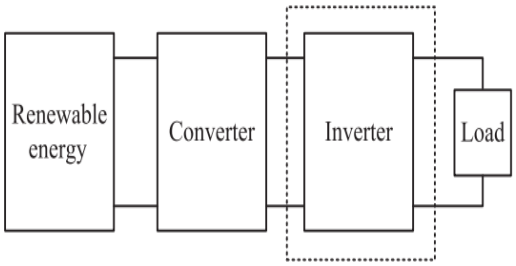

Fig. 1. Block diagram of renewable system.

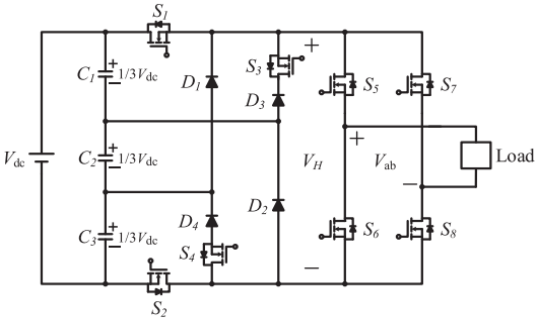

Fig. 2. Proposed seven-level inverter topology

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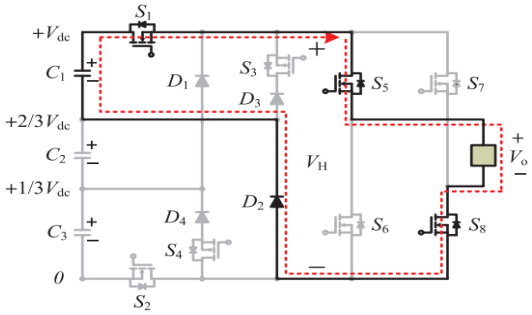

Fig. 3. Switching combination of output voltage level 1/3Vdc.

The voltage across H-bridge is V_{dc}. S_5 and S_8 are turned on, and the voltage applied to the load terminals is V_{dc}. Fig. 5 shows the current path at this mode.

4)To generate a voltage level V_0 = -1/3V_{dc}, $S2$ is turned on at the negative half cycle. Energy is provided by the capacitorC_3, and the voltage across H-bridge is 1/3V_{dc}. $S6$ and S_7 are turned on, and the voltage applied to the load terminals is -1/3V_{dc}. Fig. 6 shows the current path at this mode.

5)To generate a voltage level Vo = -2/3V_{dc}, S_2 and S_3 are turned on. Energy is provided by the capacitor C_2 and C_3. The voltage across H-bridge is 2/3V_{dc}. S_6 and S_7 are turned on, and the voltage applied to the load terminals is -2/3V_{dc}. Fig. 7 shows the current path at this mode.

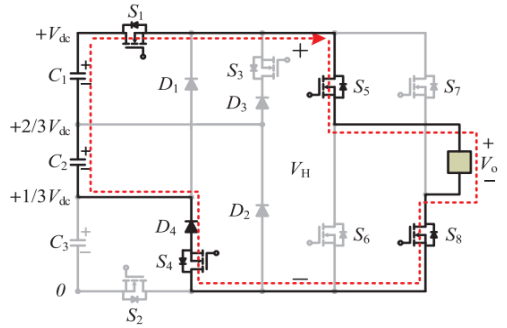

Fig. 4. Switching combination of output voltage level 2/3Vdc

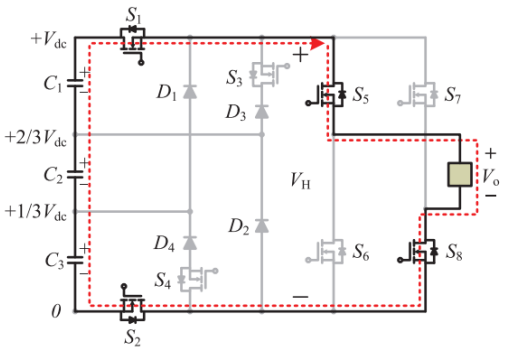

Fig. 5. Switching combination of output voltage level Vdc.

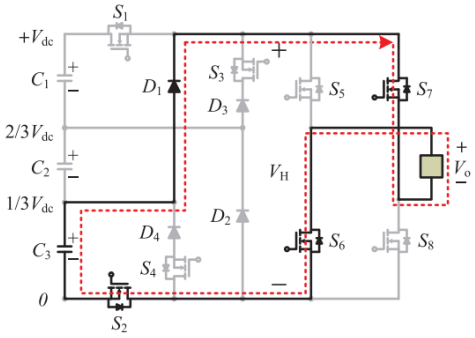

Fig. 6. Switching combination of output voltage level -1/3Vdc.

6)To generate a voltage level V_0 = -V_{dc}, S_1 and S_2 are turned on. Energy is provided by the capacitor C_1,C_2, and C_3, the voltage across H-bridge is V_{dc}. S_6 and S_7 is turned on, the voltage applied to the load terminals is -V_{dc}. Fig. 8 shows the current path at this mode.

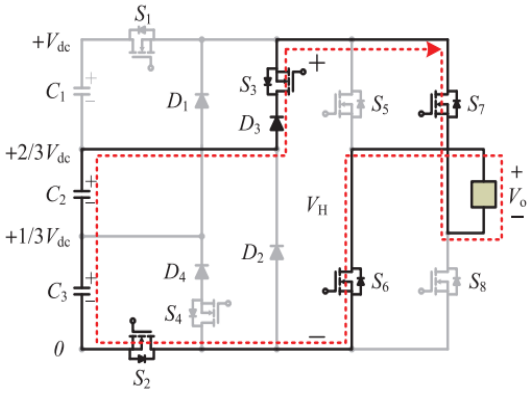

Fig. 7. Switching combination of output voltage level -2/3Vdc.

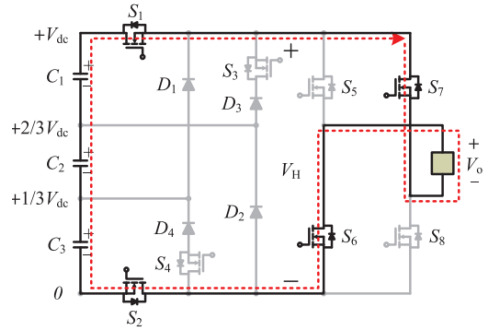

Fig. 8. Switching combination of output voltage level -*V*dc.

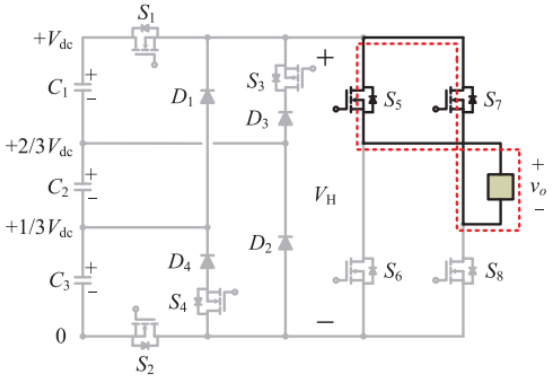

Fig. 9. Switching combination of output voltage level 0.

7) To generate a voltage level Vo = 0, S_5 and S To generate a voltage level V_0 = 0, S_5 and S_7 are turned on. The voltage applied to the load terminals is zero.Fig. 9 shows the current path at this modeTable I lists the switching combinations at different output levels

C.Topology Comparison

Table II presents the number of components required to implement a seven-level inverter using the proposed topology

TABLE I
SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

TABLE II
COMPONENTS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

TABLE III
VOLTAGE STRESS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

and three previously ones [9], [10] that can be considered as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multicell inverter.

Table II shows that the new topology achieves the reduction in the number of power devices. Table III shows the voltage stress comparison between different type inverters.

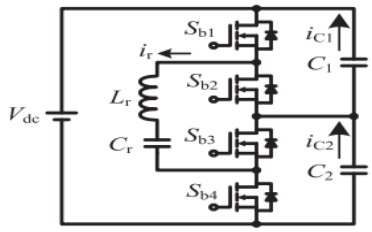

Fig. 10. Circuit configuration of RSCC

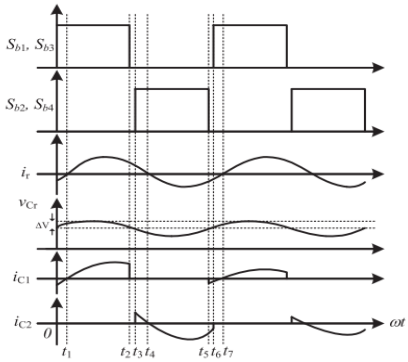

Fig. 11. Waveforms of RSCC.

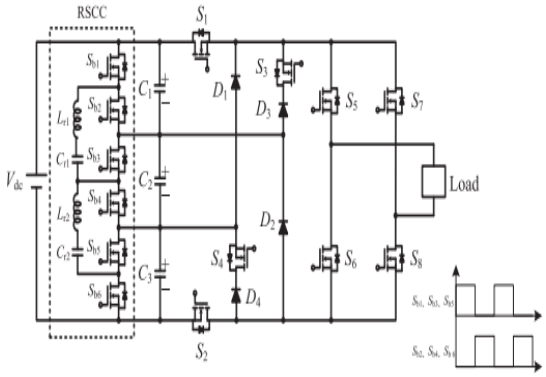

Fig. 12. Proposed multilevel inverter with RSCC.

III. VOLTAGE BALANCING CIRCUIT BASED ON RSCC

Since the voltage deviation causes larger harmonics distortion in the output voltage, voltage-balancing circuits are indispensable for the capacitors in the multilevel inverters [11]–[15]. By using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Fig. 10 shows the circuit configuration of a unit of the resonant switched-capacitor converter (RSCC). The duty cycle of every switch is equal to 50%. The voltage of $C_1$is higher than the voltage of C_2. Since the average current of C_1 is higher than that of C_2 at one switching cycle, most of the charges flow from C_1 to C_2. After few switching cycles, the voltages of C_1 and C_2 are equal. Fig. 11 shows the waveforms of the RSCCFig. 12 shows the configuration of proposed seven-level inverter with RSCC. To apply RSCC at seven-level configuration, two switches S_{b5} and S_{b6}, resonant inductor L_r, and resonant capacitor C_r are added. In this application, switches S_{b1}, S_{b3}, and S_{b5} are turned on at the same time; S_{b2}, S_{b4}, and

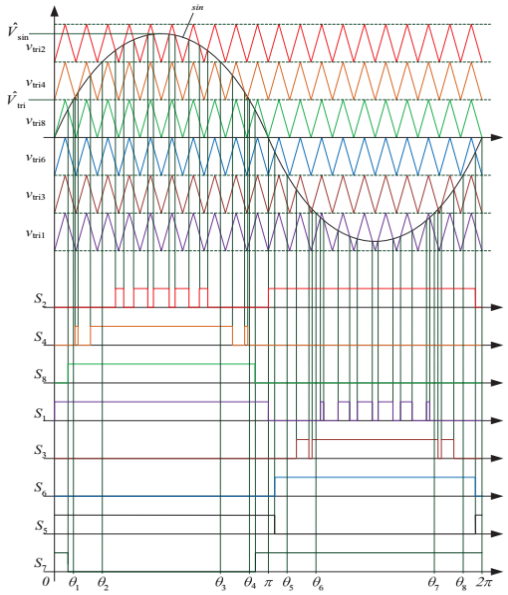

Fig. 13. Reference sine wave, carriers, and control signals of switches

*S*b6 are turned on at the same time. The duty of each switch is equal to 50%.

IV. APPLICATION OF SPWM

In this paper, several triangular carriers are distributed by phase disposition technique. The advantage of phase disposition technique is uncomplicated to realize and less total harmonic distortion [16], [17]. These carriers are compared with a reference sine waveform v_{sin} to get signal of switches. The peak-to-peak value of triangular carrier is $\hat{V}_{tri}$. The frequency of carrier is switching frequency of inverter. The peak value of reference sine wave is $\hat{V}_{sin}$, and the modulation index *m*A is defined as

$$m_A = \frac{\hat{V}_{\sin}}{3 \cdot \hat{V}_{\text{tri}}}. \quad (1)$$

According to (1), the relationship between the peak value of output sine wave and *m*A can be expressed as

$$V_o = m_A \cdot V_{\text{dc}}. \quad (2)$$

Fig. 13 shows the reference sine wave, carriers, and control signals of switches.

The method that determines switch signals in Fig. 12 is as follows.

1) $v_{\sin} < 0$ and $v_{\sin} > v_{\text{tri2}} \rightarrow S_2$ are turned on
2) $v_{\sin} > v_{\text{tri4}} \rightarrow S_4$ is turned on.
3) $v_{\sin} < v_{\text{tri8}} \rightarrow S_7$ is turned on.
4) $v_{\sin} > v_{\text{tri8}} \rightarrow S_8$ is turned on.

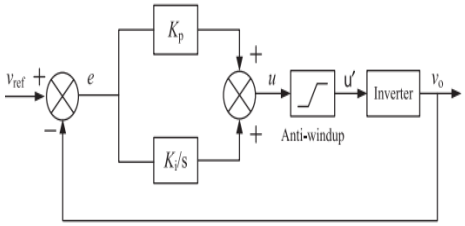

Fig. 14. Block diagram of PI control

5) $v_{\sin} > 0$ and $v_{\sin} < v_{\text{tri1}} \rightarrow S_1$ are turned on.
6) $v_{\sin} < v_{\text{tri3}} \rightarrow S_3$ is turned on.
7) $v_{\sin} > v_{\text{tri6}} \rightarrow S_5$ is turned on.
8) $v_{\sin} < v_{\text{tri6}} \rightarrow S_6$ is turned on.

V. PI CONTROL USED IN MODIFIED SPWM

Modified SPWM based on PI control is used in this paper [18], [19]. Fig. 14 shows the block diagram of PI control. The block diagram can be expressed in S domain as

$$u(s) = \left[K_p + \frac{K_i}{s}\right] e(s). \tag{3}$$

From (3), the equation can be transformed in the Z domain as

$$u(z) = \left[K_p + \frac{K_i}{1 - z^{-1}}\right] e(z). \tag{4}$$

Then, transform (4) becomes a difference equation is expressed as

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1]. \tag{5}$$

Fig. 15 shows system configuration and control block. System detects output voltage first and compares this signal with a built-in reference. Then, the system feedbacks an error to PI controller. Finally, the PI controller exports a control signal to gate driver.

The main idea of modified SPWM is to record the previous error of output voltage and generate a suitable correction at the latest cycle. Because the frequency of carrier is 18 kHz and the frequency of output sine wave is 60 Hz, the number of times of switching is 300 times. Fig. 16 shows the schematic of modified SPWM.

$V_{ref}[n]$ is defined as the reference output voltage, $V_0[n]$ is the feedback of output voltage, and $e[n]$ is error between reference output and feedback output which is expressed as

$$e[n] = v_{\text{ref}}[n] - v_o[n]. \tag{6}$$

Let $K_1 = K_p + Ki$, $K_2 = K_p$ then $e[n]$ is multiplied by $K1$ and $e[n - 300]$ multiplied by K_2. Then, add the previous output signal $u[n - 300]$. Finally, it can obtain the output of PI controller after the process by the anti-windup.

$$u'[n] = K_1 \cdot e[n] - K_2 \cdot e[n-300] + u'[n-300]. \tag{7}$$

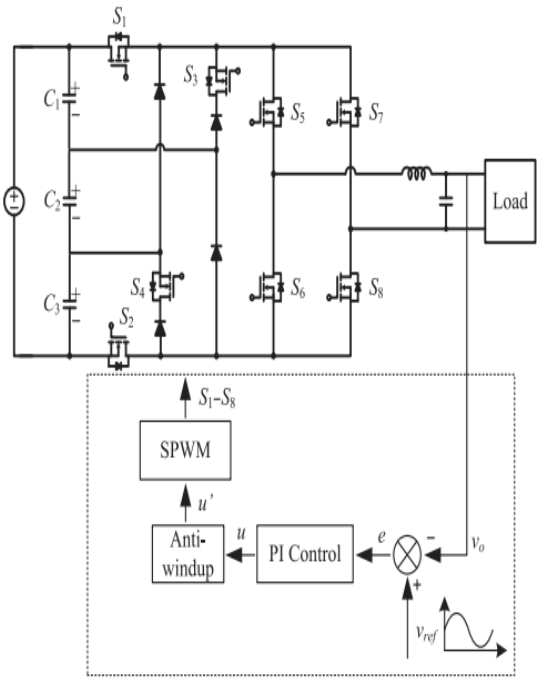

Fig. 15. Seven-level inverter with control algorithm.

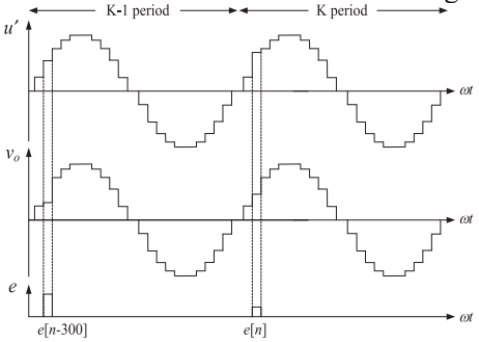

Fig. 16. Schematic of modified SPWM

TABLE IV

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SPECIFICATIONS OF THE PROPOSED INVERTER

Input voltage V_{dc}	400 V
Output voltage V_o	220 V_{rms}
Rated output power P_o	2 kW
Switching frequency f_s	18 kHz

VI.INDUCTION MOTOR

Induction Motor (1M) An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor.

Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{p}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

SIMULATION RESULTS

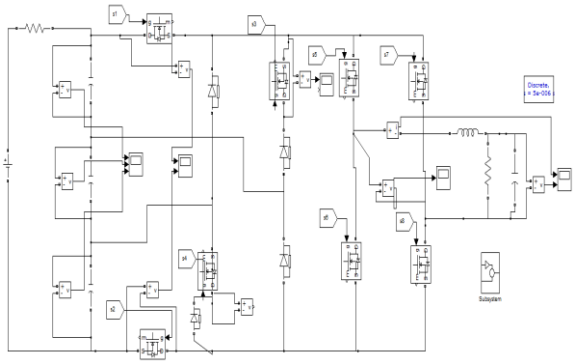

Fig.17.Simulink model of proposed seven level multilevel inverter

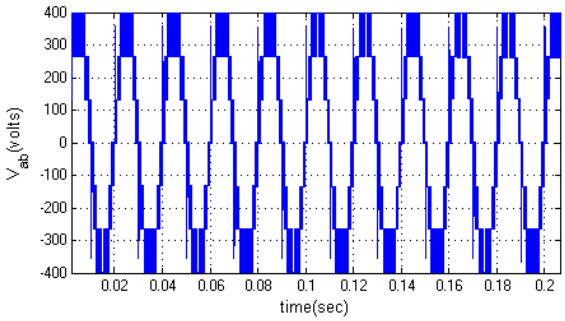

Fig.18.Waveform of V_{ab}.

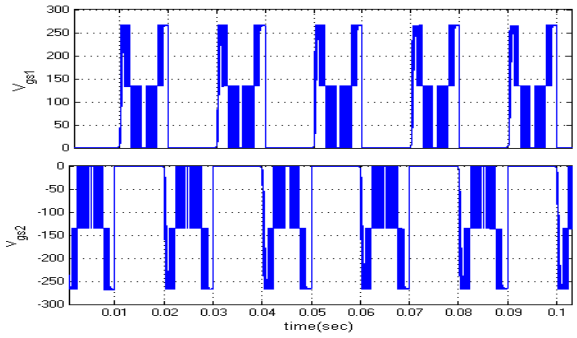

Fig.19. waveforms of V_{gs1},V_{gs2}.

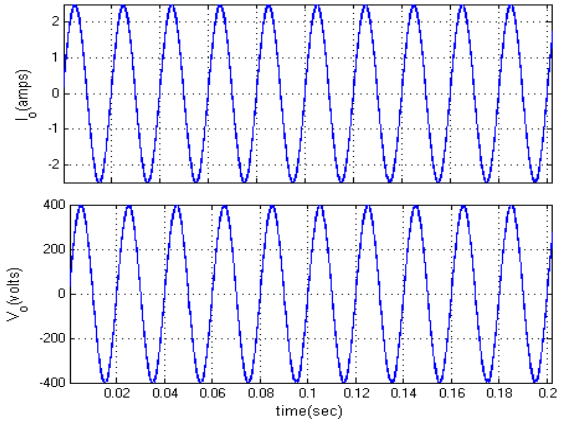

Fig.20. Output voltage & current.

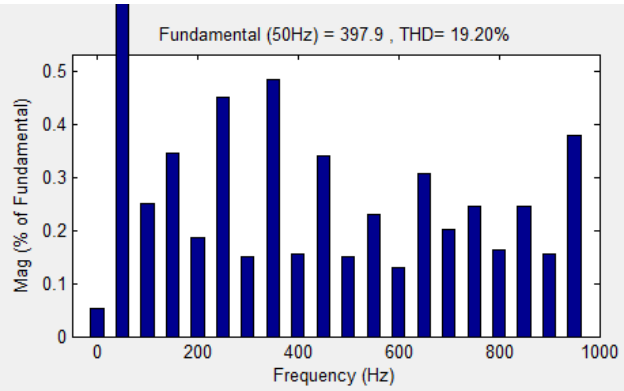

Fig.21.THD of Output voltage for seven level.

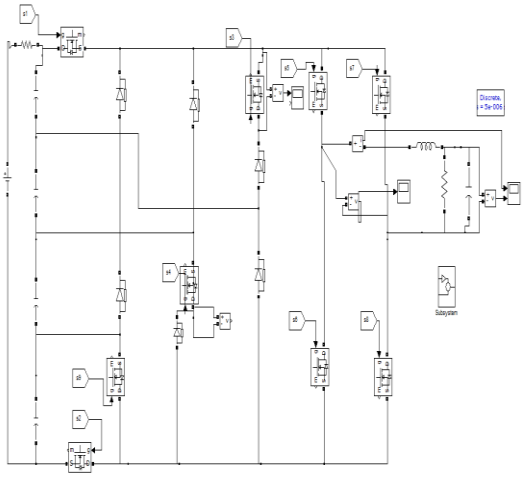

Fig.22.Simulink model of proposed MLI for Nine level Output voltage

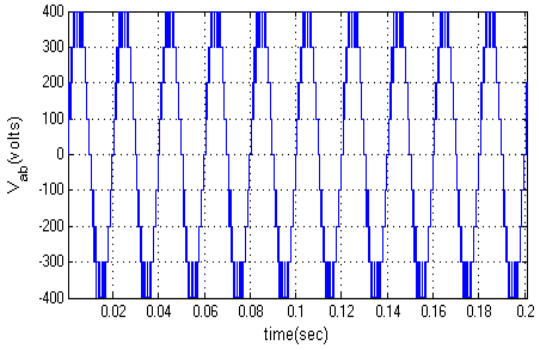

Fig.23. Waveform of v_{ab}.

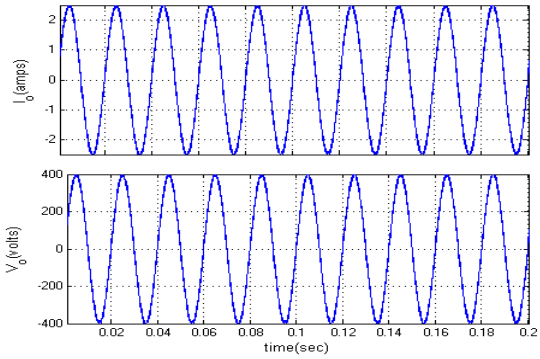

Fig.24. Output voltage & current

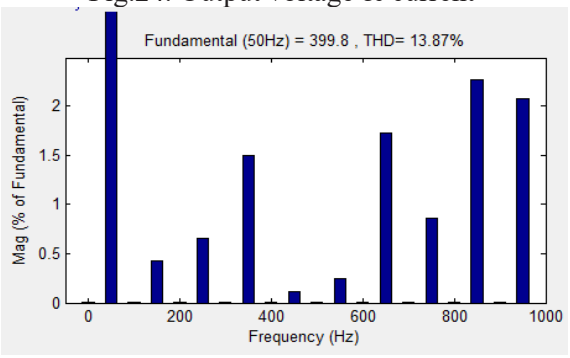

Fig.25. THD of Output voltage for Nine level

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

CONCLUSION

In conclusion it is strongly confirmed that the proposed topology could get seven levels with reduced power switches when compared with cascaded H-bridge Multilevel Inverter. The proposed topology is able to generate seven level output voltage with only 8 switches. Also the levels can enhanced by adding one more switch for the proposed topology with proper switching sequence. The overall circuit configuration is designed in Matlab/simulink software and the performance of the proposed MLI is analyzed.

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