Roburst Implementation of OFDM System Using VHDL

[1] S k. Shabana, [2] K. Hanumantha Rao

[1]M.Tech Research Scholar, Prakasam Engineering College, Kandukur, India

[2] Associate Professor, Prakasam Engineering College, Kandukur, India

Abstract:

OFDM (orthogonal frequency division multiplexing) plays important role in most of the latest communication networks such 3g, 3gs, 4g etc… To provide such abundant capabilities for these communications systems we have developed an OFDM model which based on the real time controlling systems as FSM (Finite state machine). This paper depicts the design of OFDM modulation and de-modulation systems that are generally used in the present communication systems. The complete transmitter and receiver section has been implemented using VHDL. The complete design is mainly controlled by the FSM states. The conventional system is mainly designed using analog systems hence resulting low power capabilities and design complexities. In reference to the conventional design we have implemented the OFDM system using a FFT/IFFT structures which are one of the modules of the designed system resulting in reduction of power, delay and also the area (fabricated).

Index Terms: Orthogonal frequency division Multiplexing (OFDM); Fast Fourier Transform (FFT); Inverse Fast Fourier Transform (IFFT); Finite state machines (FSM); Field Programmable Gate Arrays (FPGA)

I.INTRODUCTION:

Communication systemsis a one most import technological systems which plays important role in delivering the required information form source to destination. One of the system as OFDM is designed and implemented using Hardware description tools. To design such system we need to understand the basic block modules which are mentioned in the below figure 1.
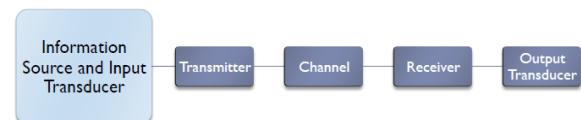

Fig 1 Communication System

In communication systems, these are classified into mainly two types based on the input data transmission as analog and digital. In the present technology, Digital transmission is more likely preferred to analog (due its low power dissipation). One such digital transmission is an orthogonal frequency division multiplexing.OFDM (Orthogonal Frequency

Division Multiplexing) has become very proficient in these days, embracing high speed data rates art wireless communications. Since the OFDM has become the core concept in the design of the latest communication systems (4th generation), it was essential to build the system which could provide a low power and reusable design flexibility.

The aim of our paper is to provide the low power and fast multiplicative architectural of implementation for OFDM for all suitable communication systems. Hence, in regards to the low power and high speed complexities the FPGA are utilized for better computational performance.

Since the FPGA's circuits are reconfigurable and reusable and hence can be easily processed the computations at faster rates and chance of enhancing the systems are also possible depending upon the design methodology. The high speed and parallel architecture provides the complete control over the degree of parallelism in the design and athematic word length.

The flexibility is the key advantage of FPGA's over traditional DSP processors. Designs based on FPGA have proven quantifiable high speed and low power capabilities for many wide range of application in networks, video and image processing techniques.In our implementation, the design multiplicity of FFT and IFFT architectures have been improved using the finite state machines resulting high speed and low power capabilities. The resource of Xilinx Virtex -5 has been suitable for the implementation as the design comprises of more thanone FFT/IFFT architectures.This paper provides a completely different design methodology using the HDL designer series, and provides an idea – what is an OFDM, its

implementation using FFT/IIFT architectures and the analysis of the obtained results. The next of the paper is organized as follows: section 2 Related Work, section 3 Overview of OFDM, section 4 VHDL emulation and simulation results and conclusions

2. RELATED WORK

Moisés Serra [3] shows the design of an OFDM transmitter as a part of an OFDM demonstrator Hiperlan/2 based, Ma. José Canet [4] shows implementation issues of a digital transmitter for an OFDM based WLAN systems and benchmarks some optimized VHDL area results against System Generator results, Canet's work is focused on the solutions for the OFDM signal generation in baseband and in intermediate frequency (IF). Chris Dick [5] emphasizes the suitability of high-level design tools whendesigning sophisticated systems, and the importance todesign FPGA systems rather than ASIC to one dayaccomplish the SDR "Software Defined Radio" conceptand gives a high-level overview of the FPGAimplementation giving some deep to the synchronization,packet detection, preamble correlate channel estimationand equalization; that is mainly at the OFDM receiver.Ludovico de Souza et al. [6] present a FPGAimplementation capable to support 802.11 wirelessmodems but just as a validating and prototyping stage foran ASIC. Joaquin Garcia, Rene Cumplido [7] focuses onthe FPGA suitability to support IF processing for the Std.IEEE 802.11a and the resource area and timing requirements either for rapid prototyping or to take advantage of re-configurability in order to be able to support different standards. Y. Awad, L. H. Crockett and R. W. Stewart [8] investigate the efficient FPGA implementation of an OFDM transceiver design for the IEEE 802.20 physical layer. Paul

Guanming Lin [9] demonstrates the concept and feasibility of an OFDM system, and investigates how its performance is changed by varying some of its major parameters. This objective is met by developing a MATLAB program to simulate a basic OFDM system. M. A. Mohamed [10] presents an FPGA technique to gain approach in the problem of OFDM system implementation.
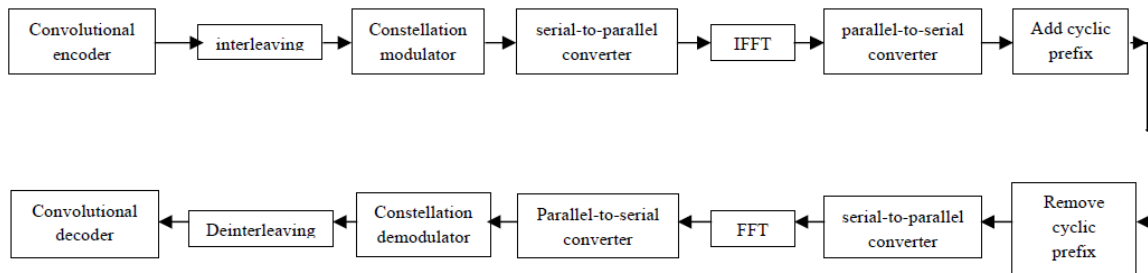
3. OVERVIEW OF OFDM

Figure 2: Representing the complete ofdm trans-receiver

3.1 OFDM Advantages

In general, OFDM systems have the following advantages:

- Efficient use of spectrum.

- Resistant to frequency selective fading

- Eliminates ISI (Inter-Symbol Interference) and ICI (Inter-Carrier Interference)

- Can recover lost symbols due to the frequency selectivity of channels;

- Channel equalization

- Computationally efficient [11].

3.2 OFDM Disadvantages

OFDM systems have the following disadvantages:

(i)High synchronism accuracy,

(ii) Multipath propagation must be avoided in other orthogonality not be affected,

(iii) Large peak-to-mean power ratio due to the superposition of all subcarrier signals, this can become a distortion problem (Crest Factor) [11].

3.3 OFDM Transceiver

The block diagram of an OFDM transceiver is shown in Fig. 2. [9].The basic component will be discussed in the next few subsections. The main components of OFDM transmitter are shown in Fig.3 [9]. The randomizer is used as random bit generator. The first three blocks are used for data coding and interleaving. The coded bits will be mapped by the constellation modulator using Gray codification, this way an + jbn values are obtained in the constellation of the modulator. The serial to parallel converter converts the data bits from the serial form to the parallel form. The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an

IFFT converts a number of complex data points, of length that is power of 2, into the same number of points but in the time domain. The number of subcarriers determines how many sub-bands the available spectrum is split into [11, 12]. The Cyclic Prefix (CP) is a copy of the last N samples from the IFFT, which are placed at the beginning of the OFDM frame to overcome ISI problem. It is important to choose the minimum necessary CP to maximize the efficiency of the system [16].

3.3.2 OFDM RECIEVER:

The main blocks of OFDM receiver are observed in Fig.3 [9]. The received signal goes through the cyclic prefix removal and a serial-to-parallel converter [11]. After that, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output. The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the time of processing and the used hardware [14]. FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT [13-15].

4. VHDL EMULATION AND ANALYSIS

The main key element is to reduce the complexity of the multiplicity of the FFT and IFFT architectures. So to implement this design we have used the HDL designer series. The figure 4 represents the block diagram of the design unit. In this design we have used FSM for the implementation of the FFT and IFFT structures in the OFDM design. This design mainly focuses on the serial to parallel conversion (vice versa), IFFT/FFT structures and

cyclic prefix. So these modules are implemented using VHDL language. The module serial to parallel conversion is mainly dealt with s-p shift register and p-s shift register. As we know that the shift register is a parallel or cascade connection of flip flop mainly D- flip flop. Hence in this design we have implemented total of 32 combination of flip-flop for both S-P and P-S conversion. The second block is coefficients generator for the real and imaginary parts of the complex terms and designed using simple multiplexing states where each output state is dependent upon the input and selection state.

Finally the third block is IFFT/FFT generator which is controlled by finite state machine. In this structure each there are total of 14 states for both IFFT and FFT. The first state is start in which all data outputs are reset to '0'. The next state is the IFFT_coeff_cond state where the coefficients are selected based on the selection for the specific structure as radix-2, radix-4, radix-8, etc… Based on the radix value we can select anyone them to operate on the input. In the previous designs we have observed that the design radix elements are only 32 or 64 or 16 or 8 etc… not all of them at the same time with respect to different timing intervals. The below figures 3, 4,represent the main block diagram and the state diagrams for both IFFT and FFT architectures.
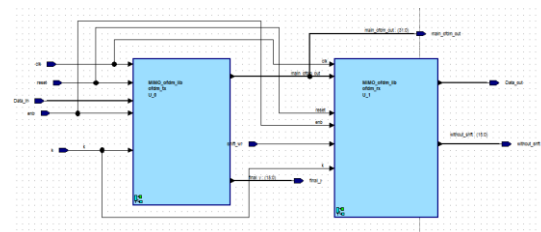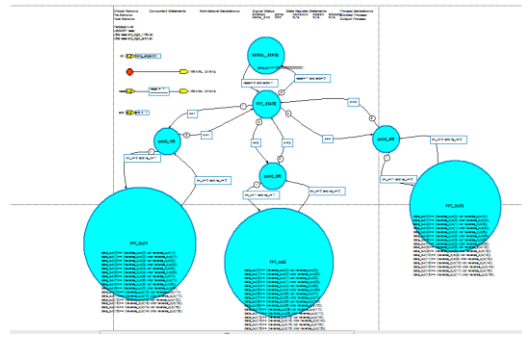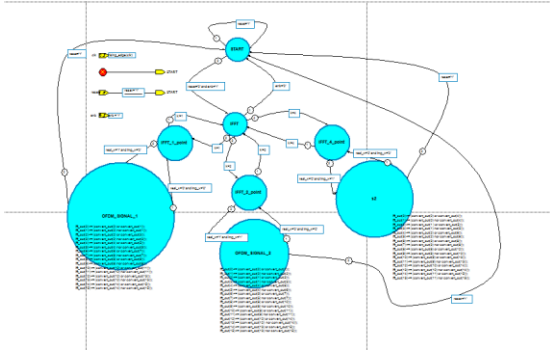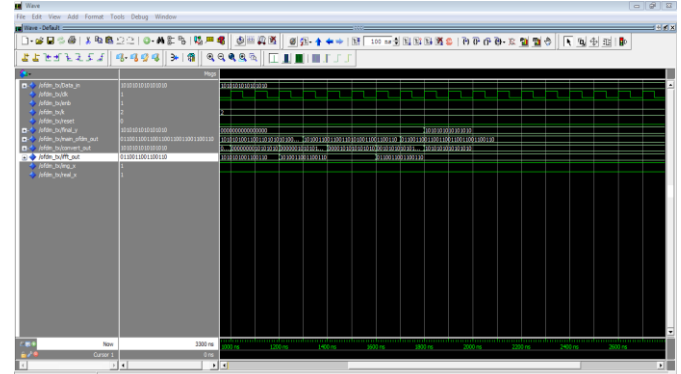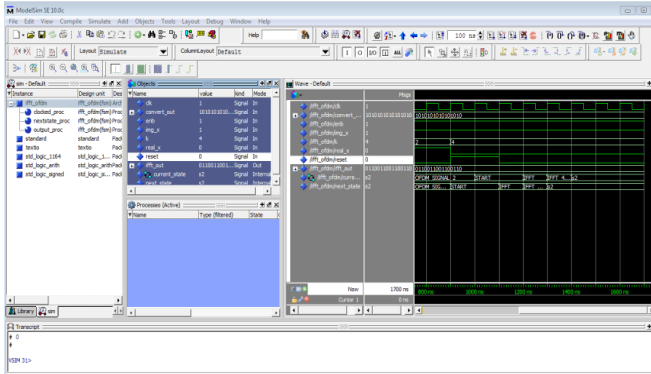

Fig 3 block diagram for both IFFT and FFT architectures.

Figs 4 state diagrams for both IFFT and FFT architectures.
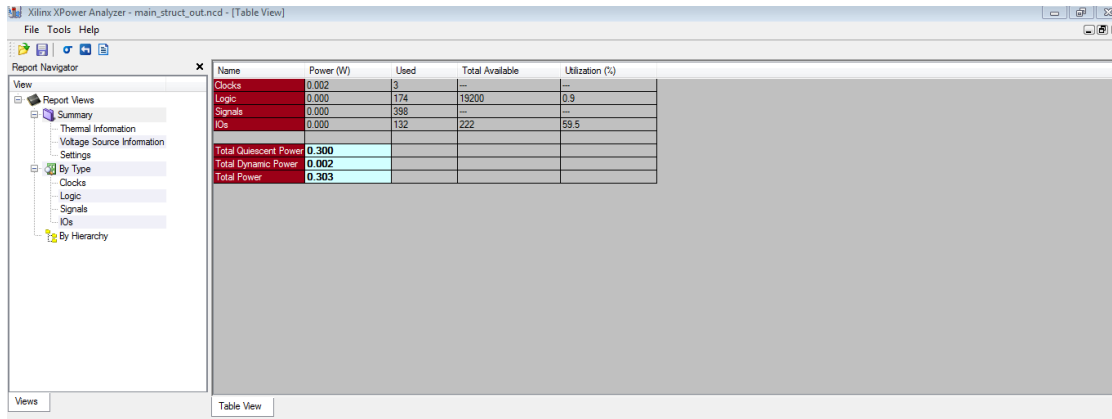
5. SIMULATION RESULTS:

Wave Forms:

AREA UTILIZATION

Device Utilization for 5VLX30FF324Virtex- 5

Sno	Resource	Used	Available	Utilization
1	IOS	132	220	60.00%
2	Global Buffers	1	32	3.13%
3	Look up tables	174	19200	0.91%
4	CLB slices	77	4800	1.6%
5	D-Flip Flops or Latches	306	19200	1.59%
6	Block RAMs	0	32	0.0%
7	DSP48Es	0	32	0.0%

POWER UTILIZATION

Total Power: 303mw

SNo	Timing Constraint	Value
1	Initial edge separation	1000
2	Source clock delay	-1.718
3	Test clock delay	+1.718
4	Setup constraint	-0.022
5	Data required time	1000.022
6	Data arrival Time	-1.771
7	Slack Obtained	998.251(87.63% cell delay, 12.37% net delay)

6. CONCLUSIONS:

This paper focuses on the robust design of OFDM system using FSM. The simulation results show completely different perspective from previously designed system. The additional radixes can be implemented with the state diagram with an ease. This paper provides a very low power design feature for the OFDM system to work in situation. The observed power is 303 mw and previously designed system has a power dissipation of 1 w which is 4 times that of the proposed one. Similarly the obtained slack is about 1ms which very significant when compared to the conventional one. Therefore the proposed design is much faster and consumes less power .Futherresearch have been done in field of the communication system specifically to improve the much latency and power capabilities for the OFDM system.

REFERENCES

[1] Joaquin Garcia, Rene Cumplido, "On the design of an FPGA-based OFDM modulator for IEEE 802.16.", proceedings of 2005 international conference on reconfigurable computing and FPGAs.

[2] Farzad Manavi, Yousef R. Shayan, "Implementation of an OFDM modem for the physical layer of IEEE 802.11a standard based on Xilinx Virtex-II FPGA.", 0-7803-8255-2/04/$20.00 2004 IEEE.

[3] Wen Fan, Chui-sing Choy, "Robust, low complexity and energy efficient downlink baseband receiver design for MB-OFDM UWB system.", IEEE transactions on circuits and system 1549-8328/$26.00 2011 IEEE.

[4] R. Van Nee, R. Prasad Publication by Artech House, "OFDM for wireless Multimedia Communications.", e-book.

[5] R.W. Chang, "Synthesis of band limited Orthoganal Signals for Multichannel data transmission," Bell syst. Tech. J., Vol. 45, pp. 1775-1776, December.1996.

[6] Salzberg, B. R., "Performance of an efficient parallel data transmission system," IEEE transaction comm., Vol. COM-15, pp.805-813, December. 1967.

[7] Weinstein, S. B., and P. M. Ebert, "Data transmission by Frequency Division Multiplexing using the DFT," IEEE Trans. Comm., Vol.COM – 19, pp. 628-634, October.1971.

[8] Horosaki B., "An orthogonally multiplexed QAM system using the DFT," IEEE Trans. Comm. Vol. COM-29, pp. 982-989, July 1981.

[9] Kitaek Bae, Student Member, IEEE, Jeffrey G. Andrews, Senior Member, IEEE, and Edward J. Powers, Life Fellow, IEEE,"Quantifying an Iterative Clipping and Filtering Technique for reducing PAPR in OFDM", IEEE Transactions on wireless communications, vol. 9, no. 5, may 2010.

[9] Michael Bernhard, Joachim Speidel on "Implementation of an IFFT for an Optical OFDM Transmitter with 12.1 Gbit/s".

[10] Chandrashekhar Kukade, R. M. Patrikar, R. B. Deshmukh, "Design & Implementation of OFDM base band for The IEEE 802.11a WLAN",at (VNIT Nagpur).

[11] William Y Zou, Yiyan Wu."COFDM:AN OVERVIEW" IEEE TRANSACTION ON BROADCASTING. VOL41, NO1, MARCH 1995