

# Design a Novel Approach to Verification the Faults in Circuit

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**ABSTRACT:** *A Globally Asynchronous Locally Synchronous (GALS) modeling tool is introduced for circuit verification. In particular, this approach enables the visualization of point-to-point causality of problems occurring among various parts of the system which are more difficult for analyzing. The reliability and quality improvements are essential for digital circuits as their complexity and density increases. Validation of VLSI circuits becomes more difficult with higher test cost. In Circuit Under Test (CUT) architectures, the Test Pattern Generator (TPG) utilizes Linear Feedback Shift Register (LFSR) generates pseudo random patterns that increases the switching activity of test patterns. The test pattern generator generates a multiple single input change vector which increases the accuracy of test response. The TPG is used in test-per-scan scheme. A combinational circuit is used as the circuit under test, and the output response of CUT is stored in Look Up Table (LUT) for error comparison in LUT method of verification. Reversible technique is also used for the testing the circuit under test.*

**Keywords:** Verification tool flow, CUT, The Multiple Single Input Change for test-per-scan schemes (MSIC-TPG).

## I.INTRODUCTION

Whilst there has been a lot of interest in researching new architectures for globally asynchronous locally synchronous (GALS) there have been few attempts at providing modeling solutions for GALS communication. Thus, modeling of GALS from specifications has been limited to hardware description languages such as Verilog, VHDL.

A graphical tool has been developed but the models here are also used at a higher level, i.e., they are not used for circuit deadlock analysis. Although the techniques are higher level they offer better modeling of things like protocols. The work is more similar in the sense that different formats are interchangeable allowing different tools to be linked which is a useful approach to take but is centered on co-simulation rather than verification or deadlock analysis.

To eliminate the various defects caused by the manufacturing process, System on Chip (SoC) circuits depends on testing. Testing is the indigenous phase which attribute towards the successful implementation of any device. Importance of testing in Integrated Circuit is to improve the quality in chip functionality that is applicable for both commercially and privately produced products. In Today's IC, as designs become more complicated. In order to test any circuit or device we require separate testing technique which should be done automatically. A CUT is used for this purpose. CUT techniques can effectively reduce the difficulty and complexity of VLSI testing. This CUT methodology aims at detecting faulty components in a system by introducing the test logic into the chip. Testing is better known for its numerous advantages such as at-speed testing and reduced need for expensive external Automatic Test Equipment (ATE). The steps in this approach are:

1) On-chip generation of test pattern.

- 2) Application of the test patterns to the circuit under test.
- 3) Analysis of circuit under test responses with on-chip output response analyzer (ORA)
- 4) Making decision whether the chip is faulty or not.

### II.EXISTED SYSTEM

The modeling and verification flow is shown in Fig. 1. Modeling is undertaken via a tool called Work craft. Work craft is a framework for a variety of plugins that aid in the visualization of different graphical interpretations but which are linked. This enables translation and cross visualization between different models at different levels, e.g., Verification, circuit Petri-nets, and, therefore, the analysis of lower level models can be related back to the original model graphically. Inside Work craft Verification circuit is translated to circuit.

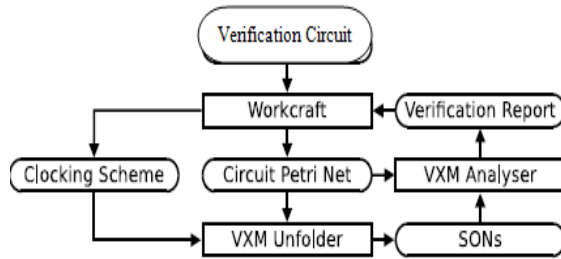


FIGURE 1. VERIFICATION TOOL FLOW

Petri-nets and then a novel unfolding algorithm is deployed using an unfold from circuit Petri-nets to structured occurrence nets (SONs). The causality of deadlocks can be difficult to analyze if significant parts of a GALS system become disabled particularly those using intricate feedback. SONs were designed to enable visualization of such complex behaviors which are more difficult to analyze and they are used for the modeling of structural links between modules. This is useful particularly when one wants to investigate point-to-point effects or how far the occurrence and effect of a problem extends between different modules.

A multilevel analyzer (VXM analyzer) is used for verification. For this a novel formalism based on blocking/idle deadlock relations is introduced which describes how deadlocks in different parts of the system relate to each other. This representation, which is derived from the SONs model, enables more detailed structural visualization of the deadlocks and their causality throughout the GALS communication system. Via feedback through Work craft it enables direct and indirect deadlocks related to synchronizer handshake and latency errors to be analyzed. It enables structural analysis of deadlocks to be carried out across communication links to reveal the following details: vulnerable parts of the system which are susceptible to shutdown; point-to-point causes of deadlock from one local module to another (using querying); multiple original causes of deadlocks and their visualization in a single instance or snapshot and difficult to detect deadlocks that are hidden or masked by other deadlocks.

### III.PROPOSED SYSTEM

The basic CUT architecture shown in Figure2 consists of a test pattern generator (TPG), circuit under test (CUT) and an output response analyzer (ORA) also called as Output Data Analyzer (ODA). Test patterns for the circuit under test are generated by the test pattern generator. A typical response analyzer is a comparator that compact stored responses of all possible inputs and analyzes the test responses to determine correctness of the circuit under test.

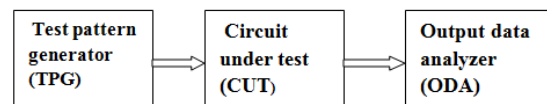


FIGURE 2: BASIC CUT ARCHITECTURE.

In conventional CUT architectures, the Linear Feedback Shift Register (LFSR) is commonly utilized in the test pattern generators due to its simplicity and effectiveness of the LFSRs. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the circuit under test, which leads to excessive power dissipation in the circuit under test. They also can damage the circuit and reduce the product yield and lifetime of CUT. The random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among the adjacent bits within each pattern. Therefore it is essential that the patterns generated by the test pattern generator must have only the minimum transitions.

Low correlation which exists between the consecutive test vectors increases the switching activity and eventually power dissipation in the circuit during the test mode. The same happens when applying low correlated patterns to scan chains. The increasing switching activity in scan chain leads to increase the power consumption in scan chain and its combinational block. Several problems are caused due to this extra power like formation of hot spots, instantaneous power surge which causes circuit damage, difficulty in performance verification and reduction of the product yield and lifetime.

#### A. MSIC-TPG for Test per Scan schemes:

The Multiple Single Input Change for test-per-scan schemes (MSIC-TPG) is shown in Figure 3. Tests per scan scheme consist of scan chains, test pattern generator, CUT, Look Up Table (LUT) block. In the seed generator circuit by clocking unique seed vector is provided. The reconfigurable Johnson counter is operated in all the three modes for producing every possible

unique Johnson codeword. After XOR operation among these seed vector and Johnson codeword, single bit change vectors are generated. These test vectors are given to CUT which should produce the expected outcome, and is stored in the LUT and to the scan chain blocks. The output of circuit under test is given to the look up table which compact the expected output of the circuit under test. The LUT makes a comparison of test response of CUT with the stored responses and decides whether the circuit is faulty or not.

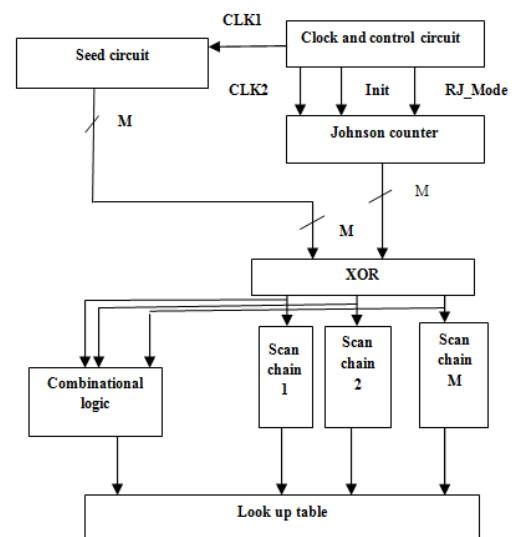


FIGURE 3: MSIC-TPG FOR TEST-PER-SCAN SCHEME

#### B. Verification of Circuit under Test:

The verification of the circuit under test is done with the test per scan technique. From the scan chains produced from the test per scan method, one of the scan chains is considered as the input to the circuit under test. For testing the circuit, the test patterns generated from the multiple single input change test pattern generator is applied as the input to the CUT. The Multiple Single Input Change (MSIC) sequence generated has the favorable features of uniform distribution and low input transition density. If

the produced test pattern of Multiple Single Input Change (MSIC) is a test pattern generator (TPG) gives the expected output of the circuit under test without any error, a conclusion can be made that the test pattern generation in Built-In Self Testing is sound. Reducing the switching activity between the test patterns can reduce the faults in the circuit under test to a great extend by eliminating errors like stuck at faults.

MSIC test patterns are single input change vectors which have only single bit transition among test patterns. A combinational circuit is utilized as the circuit under test. After applying the test patterns from the Multiple Single Input Change to the circuit under test (CUT), the verification of the CUT can be done in two ways. Initially, a reversible technique is utilizing in the circuit under test. Another method is by using a Look Up Table (LUT) method. A typical LUT works as a comparator with stored responses and analyses the test responses to determine the correctness of the CUT.

### C. Reversible Technique:

To validate the CUT, the test patterns are generated by MSIC test pattern generator is applied to the circuit under test. The circuit under test can be either combinational, sequential or a combination of both. A combinational circuit is used in this work. XOR gates are used in the combinational circuit because they possess reversible property. The XOR gate produces the same input as output, if the output of an XOR operation is XORed with any one of the input which is applied. The circuit under test (CUT) must be reversible in nature for the verification of the CUT by utilizing reversible technique.

The test patterns which are applied to the CUT provides corresponding test responses. The response of the reverse circuit of CUT obtained

by inputting the test response of CUT should generate the same pattern that is applied to the circuit under test. If this happens, a conclusion can be made that the test response produced by the CUT with MSIC patterns that has minimum transitions given as input is accurate. Figure 4 gives the idea of reversible technique used in this work. Thus we can minimize the error in the CUT by applying the MSIC patterns generated from the MSIC test pattern generator.

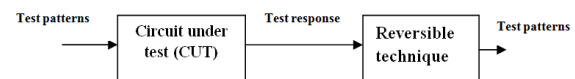


FIGURE 4: REVERSIBLE TECHNIQUE

### D. Look Up Table Method:

Look up tables may be pre-calculated and stored in static program storage or stored in hardware for application specific platforms. A combinational circuit is used as circuit under test and output response of the CUT is stored in Look Up Table (LUT) for error comparison. Depends on the circuit, output values are stored in the LUT which are corresponding to the inputs. LUT method differentiates the test response of the circuit under test and the data stored in the look up table. A typical LUT works as a comparator with stored responses and analyses the test responses for determining the correctness of the CUT. Fault is detected by verifying the output of the circuit under test and output of Look up Table. Simultaneously, Test patterns are applied for both CUT (XOR gate circuit) and LUT. Then the output from the circuit under test will be verified by comparing the output of LUT.

## IV.RESULTS

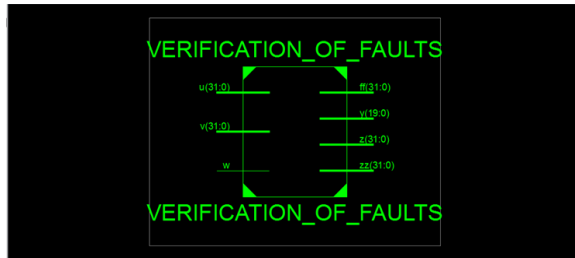


FIGURE 5: INPUT WAVE FORM

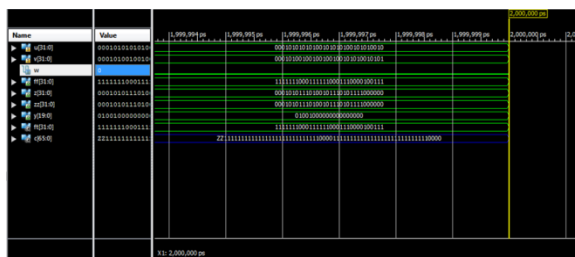


FIGURE 6: OUTPUT WAVEFORM

## V.CONCLUSION

In this paper, a low-power test pattern generation method is presented. The MSIC sequence which is produced by the MSIC test pattern generator may contain repeated test patterns but switching activity results in error is reduced. Thus the proposed system improves the test efficiency. This method also reduces the power consumption during testing mode with minimum number of switching activities between test patterns. The validation process is conducted on the combinational logic circuit and the output is verified through two techniques, the reversible technique and the LUT technique. From the comparison between these two techniques, a conclusion can be made i.e, in application where area is not a major concern, LUT method can be used. In case of compact devices, where area is considered LUT method of testing is not used.

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