International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 04
February 2018

A Novel High Speed and Area-Efficient Of Hybrid Turbo Decoders

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ABSTRACT: *Long Term Evaluation (LTE) has been used to achieve peak data rates in wireless communication system. Turbo codes are used as the channel encoding scheme. multiple maximum a posteriori (MAP) algorithm has been used as a decoding scheme. Complexity in MAP algorithm is reduced by implementing the algorithm in log domain giving rise to Log MAP algorithm. The main objective of this work is to reduce the complexity of state metric computation by employing of various algorithms and these algorithms differ only by their implementation of correction terms. The state metric calculation is implemented with the help of radix-4 Add -Compare-Select (ACS) unit. The distance calculation involved between two concurrent computations of state metric can be shared among them which give rise to Maximum Shared Resource (MSR) architecture. The proposed implementation of these algorithms leads to reduction in the power dissipation, propagation delay and the number of logical elements used for the recursion computation in turbo decoders used in LTE system.*

Keywords: Add–Compare–Select (ACS) Unit; Long-Term Evolution (LTE); Turbo Decoder; Wireless Communications);

I.INTRODUCTION

The wireless communication technology which has connected the people all over the World from anywhere anytime is now rapidly growing on demand to achieve high data rate transmissions. To accomplish this a reliable channel coding scheme has to be adopted. Turbo codes are one of the high performance channel codes with forward error correction (FEC) provides optimal performance which is approaching the Shannon limit.

This scheme is mainly utilized in the digital communication systems where the transmitted signals often get corrupted by noise due to their non-ideal behavior in realistic communication channels. So, turbo codes are used at the most in long term evolution (LTE) systems. In this paper, the architecture of turbo encoder and turbo decoder are proposed. The main aim is reducing the area occupied by computational units in decoder block by employing the ACS 4 unit along with MSR (Maximum Shared Resource) architecture by simplifying the computations.

II.EXISTED SYSTEM

3 Line to 8 Line Decoder: The decoder circuit provides 8 logic outputs for 3 inputs and has a enable pin. The circuit is designed with AND and NAND logic gates. It takes 3 binary inputs and activates one of the eight outputs. 3 to 8 line decoder circuit is also known as binary to an octal decoder.

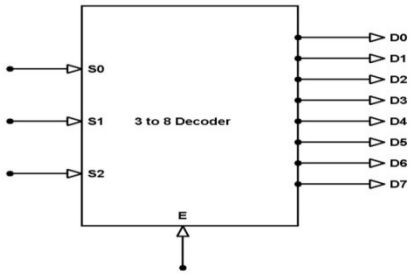

FIG 1. 3 TO 8 LINE DECODER BLOCK DIAGRAM

The block diagram of 3 to 8 decoder is shown in figure 1. The decoder circuit works only when

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the Enable pin (E) is high. Three different inputs are S0, S1 and S2 and D0, D1, D2, D3. D4. D5. D6. D7 are the eight outputs. Fig 2 shows the circuit diagram with AND and NAND logic gates.

CIRCUIT DIAGRAM:

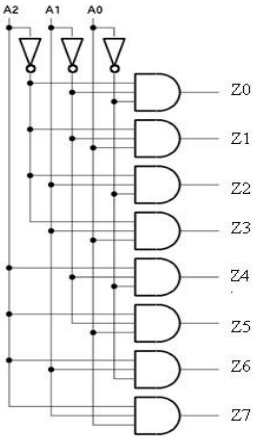

FIG 2. 3 TO 8 DECODER CIRCUIT

3 to 8 Line Decoder Truth Table:
The truth table of 3 to 8 decoder is as follows:

X2	X1	X0	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Table 1: Truth Table of 3:8 decoder

III.PROPOSED SYSTEM

A. Turbo Encoding Architecture: The coding scheme presented in LTE specification is a classic turbo coding scheme including a turbo encoder and turbo decoder.

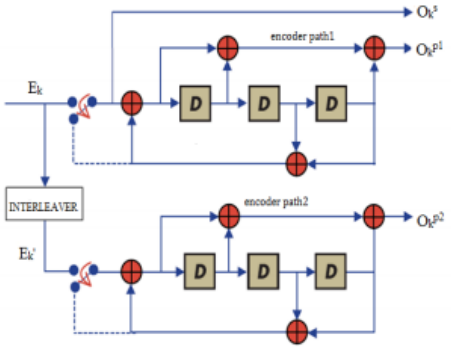

FIG 3. TURBO ENCODER

The LTE Turbo encoder includes one interleaver block and two constituent encoders. The two constituent encoders utilized are similar with generator polynomials g0 (D) = 1 + D2 + D3 and g1(D) = 1 + D + D3. This is depicted in Figure 3. The information bits along with the parity bits that are been generated by two convolution encoders are transmitted. Initially each shift register is set to zero i.e the convolutional encoder is in zero state.

The information block Ck is the input to the LTE turbo encoder which can be seen in the figure 3. The K bits relating to the input are transmitted to the output as systematic bits in a steam of Xk. At the same time, the first constituent encoder processes the information block which results in the parity bits Zk. The second constituent encoder handles the interleaved version of the information block which results in the parity bits. The interleaver is a device that permutes the data sequence in some predetermined manner. Interleaver is used to scramble bits before being input to the second

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encoder. This makes the output of one encoder different from the other encoder.

Thus, even if one of the encoders produces a low-weight occasionally, the probability of both the encoders produces a low-weight output is extremely small. This improvement is known as interleaver gain. Another purpose of interleaving is to make the outputs of the two encoders uncorrelated from each other. Combining the systematic bits and the two streams of parity bits, the following sequence is obtained at the output of the encoder. At the end of the coding process, in order to drive back the constituent encoders to the initial state, the switches from Fig. 3 are moved from position A to B.

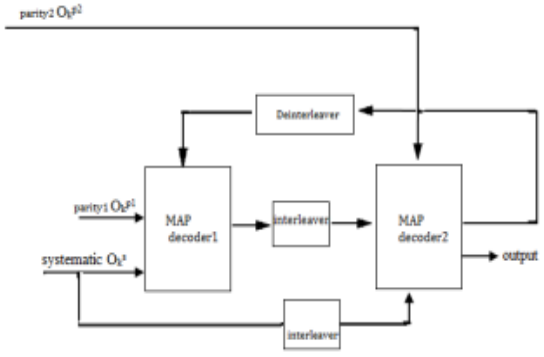

FIG 4: TURBO DECODER

The decoding plan of LTE turbo decoder is depicted in Fig. 4. In the decoder architecture, there are 2 decoders corresponding to 2 Recursive Systematic Convolutional (RSCs). Due to the existence of a feedback path as demonstrated, the operation of the turbo decoder is done in an iterative way. For every full iteration decoder comprises of two half iterations such that one for every constituent code it is used. The planning of the decoder is such that the MAP decoder 1 starts working amid the primary half iteration and MAP decoder 2 works amid the second half cycle.

The 1st MAP decoder inputs are the tainted systematic array of bits Xk, the parity stream of bits Y1k from the first RSC encoder, and from 2nd MAP decoder the deinterleaved extrinsic information. To the 2nd MAP decoder the inputs are the tainted interleaved systematic bit stream, parity stream of bits Y2k from second RSC encoder, and from 1st decoder the interleaved extrinsic information. The Maximum A Posteriori (MAP) algorithm is utilized by two Recursive Systematic Convolutional (RSC) decoders. The exemplary algorithm gives the very good decoding executions, yet it experiences a very high complexity during implementation and low decoding throughput.

IV.RESULTS

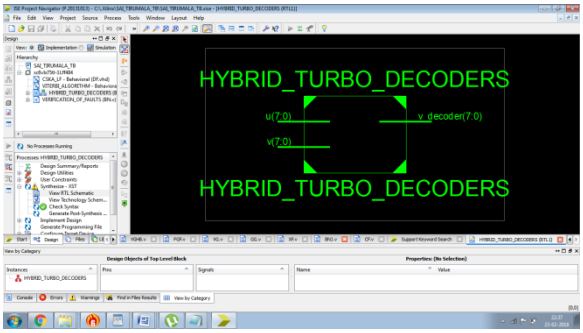

FIG 5: RTL SCHEMATIC

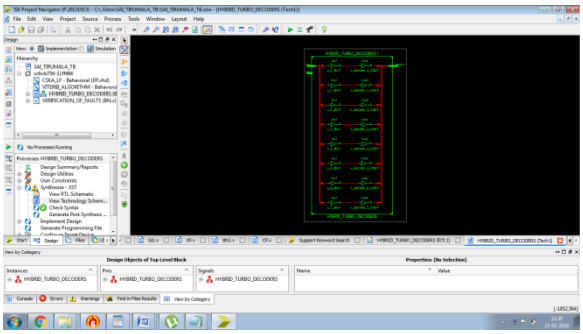

FIG 6: TECHNOLOGY SCHEMATIC

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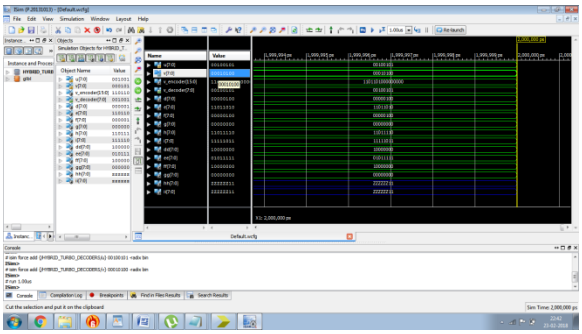

FIG 7: OUTPUT WAVEFORM

V.CONCLUSION

The most important aspects regarding the FPGA implementation of a turbo decoder for LTE systems were presented in this paper. Turbo decoders are used for error detection and error correction for distance communication. Turbo codes, the described channel coding strategy in LTE, suffers from a low-decoding throughput because of its iterative decoding algorithm. A MAP based turbo decoder has been implemented which increases the throughput.

This paper also proposes the adoption of an advanced interleaver, which reduces delay in decoding process and hence has less latency. Hence Turbo code is better in terms of performance, low latency, and computational complexity than other codes.

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