International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 04
February 2018

Design a High Speed Carry Skip Adder with Ladner Fischer Technique

Avvaru.Vijay Kumar & K.Ramesh Babu.
[1]M.Tech scholar, Dept of E.C.E, Sai Tirumala NVR Engineering College, Narasaraopet.
[2]Associate Professor, Dept of E.C.E, Sai Tirumala NVR Engineering College, Narasaraopet.

ABSTRACT:*A carry skip adder (CSKA) structure is presented which has lower power consumption with a higher speed. The performance of the conventional CSKA is improved by achieving the speed enhancement by applying concatenation and incrementation schemes. The existed structure utilizes AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) compound gates for the skip logic. A parallel-prefix adder provides the best performance in VLSI design. However, performance of Ladner-Fischer adder through black cell takes huge memory. So, gray cell can be replaced by black cell which gives the Efficiency in Ladner-Fischer Adder. The proposed system contains three stages of operations they are pre-processing stage, carry generation stage, post-processing stage. The pre-processing stage focuses on propagate and generate, carry generation stage focuses on carry generation and post-processing stage focuses on final result. In ripple carry adder each bit is waited for the previous bit addition operation. In efficient Ladner - Fischer adder, addition operation does not wait for previous bit addition operation and modification is done at gate level for improving the speed and to decreases the memory used.*

KEY WORDS: Ripple carry adder, Efficient Ladner–Fischer adder, Black cell, Gray cell

I.INTRODUCTION

Addition operation is the main operation in digital signal processing and control systems. The fast and accuracy of a processor or system is based on the performance of adder. In DSP processors and general purpose processors the addition operations are taken from simple ripple carry adder.

In ripple carry adder, each bit full adder operation consists of sum and carry, that carry will be given to next bit full adder operation, this process is continuous until the Nth bit operation. The N-1th bit full adder operation carry will be given to the Nth bit full adder operation present in the ripple carry adder.

For 16-bit ripple carry adder, the first bit carry is given to second bit full adder, second bit carry is given to the third bit full adder, similarly the operation is continue till fifteenth bit carry is given to sixteenth bit full adder. The addition operation is performed from least significant bit to most significant bit in ripple carry adder.

II.EXISTED SYSTEM

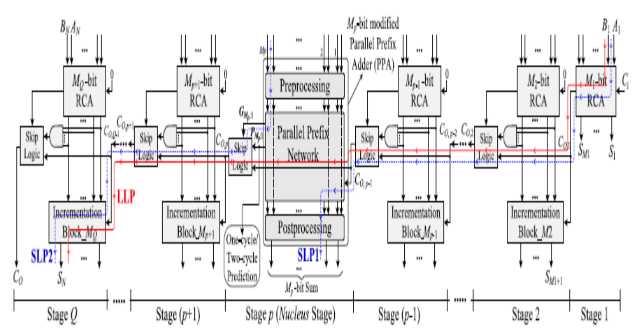

Fig. 1 Structure of the existed hybrid variable latency CSKA

The existed structure is based on combination of the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, it is denoted by CI-CSKA. It provides us with the ability to utilize simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, it becomes complemented when the carry propagates through the skip logics. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the existed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

III.PROPOSED LADNER-FISCHER ADDER

The proposed Ladner-Fischer adder is flexible to speed up the binary addition and the structure looks like tree structure for the high performance of arithmetic operations.

In ripple carry adders each bit have to wait for the last bit operation. In parallel prefix adders instead of waiting for the carry propagation of the first addition, the idea here is to overlap the carry propagation of the first addition with the computation in the second addition, and so forth, since repetitive additions will be performed by a multioperand adder.

Research on binary operation elements and motivation gives development of devices. Field programmable gate arrays [FPGA's] are most popular in recent years because they improve the speed of microprocessor based on applications like mobile DSP and telecommunication. The construction of efficient Ladner-Fischer adder contains three stages. They are pre-processing stage, carry generation stage, post-processing stage.

A. Pre-Processing Stage

In the pre-processing stage, generate and propagate are from each pair of inputs. The propagate perform "XOR" operation of input bits and generate operation "AND" operation of input bits. The propagate (Pi) and generate (Gi) are shown in below equations 1 and 2.

$$P_i = A_i \text{ XOR } B_i - - - - \quad (1)$$

$$G_i = A_i \text{ AND } B_i - - - - \quad (2)$$

B. Carry Generation Stage

In this stage, carry is generated for each bit called as carry generate (Cg). The carry propagate and carry generate is generated for the further operation but final cell present in the each bit operation gives carry. The last bit carry will help to produce sum of the next bit simultaneously till the last bit. The carry generate and carry propagate are given in below equations 3 and 4.

$$C_p = P_1 \text{ AND } P_0 - - - - - - - \quad (3)$$

$$C_g = G_1 \text{ OR } (P_1 \text{ AND } G_0) - - \quad (4)$$

The above carry propagate Cp and carry generation Cg in equations 3 & 4 is black cell and the below shown carry generation in equation 5 is gray cell. The carry propagate is generated for the further operation but

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 04
February 2018

final cell present in the each bit operation gives carry. The last bit carry will help to produce sum of the next bit simultaneously till the last bit. This carry is used for the next bit sum operation, the carry generate is given in below equations 5.

$$C_g = G_1 \text{OR} (P_1 \text{ AND } G_0) - - \quad (5)$$

C. Post-processing stage

It is the last stage of an efficient Ladner-Fischer adder, the carry of a first bit is XORed with the next bit of propagates then the output is produced as sum and it is shown in equation 6.

$$S_i = P_i \text{ AND } C_{i-1} - - - - - \quad (6)$$

It is used for two sixteen bit addition operations and each bit carry is undergoes post-processing stage with propagate, provides the final sum. The first input bits operated in pre-processing stage and it will produce propagate and generate. These propagates and generates undergoes carry generation stage produces carry generates and carry propagates, these undergoes post-processing stage and gives final sum. The step by step process of efficient Ladner-Fischer adder is shown in Fig 2.

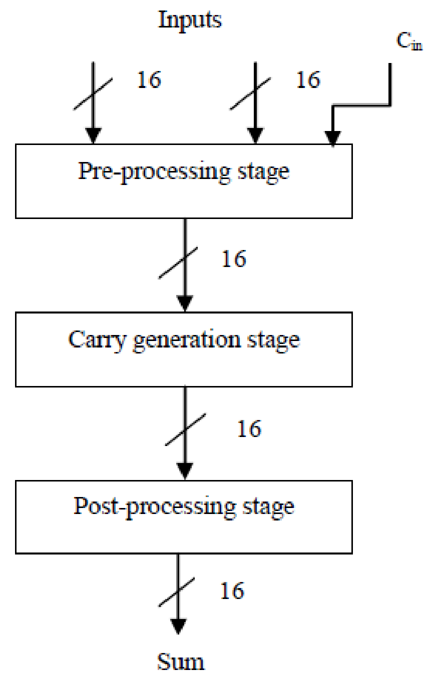

Fig 2: Flow chart for Efficient Ladner-Fischer adder.

In Efficient Ladner-Fischer adder, black cell operates three gates and gray cell operates two gates. The gray cell reduces the delay and memory because it operates only two gates. The proposed adder is design with the both black and gray cells. By using gray cell operations at the last stage of proposed adder gives a enormous dropping delay and memory used.

The proposed adder is shown in fig 3 which increases the speed and decreases the memory for the operation of 8-bit addition. The input bits Ai and Bi concentrates on generate and propagate by XOR and AND operations. These propagates and generates undergoes the operations of black cell and gray cell and produces the carry Ci. That carry is XORed with the propagate of next bit, which gives sum.

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 04
February 2018

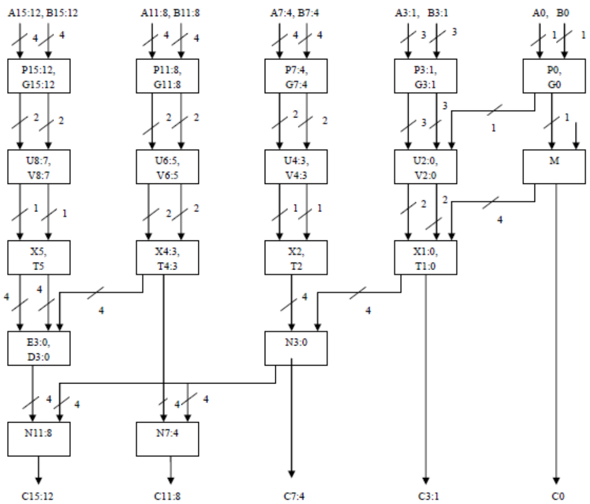

Fig 3: 16-Bit Efficient Ladner-Fischer Adder

The logical circuit is utilizing multiple adders to find the sum of N-bit numbers. Each addition operation has a carry input (Cin) which is the previous bit carry output (Cout).

The Efficient Ladner-Fischer Adder design takes less number of gates. Generally each black cell consists of two AND gates, one OR gate and gray cell consists of one AND gate, one OR gate. The last stage design with the gate level logic with the gray cell reduces delay and memory.

IV.RESULTS

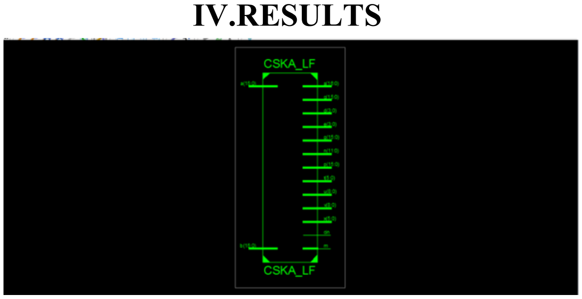

Fig 4. RTL Schematic

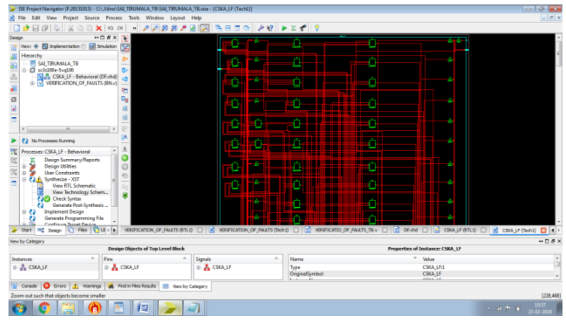

Fig. 5.Technology Schematic

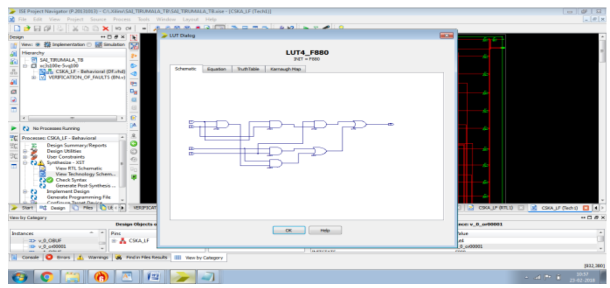

FIG 6. Look Up Table (LUT)

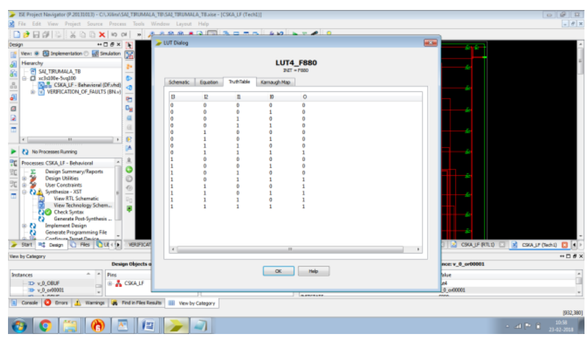

Fig 7.Truth table

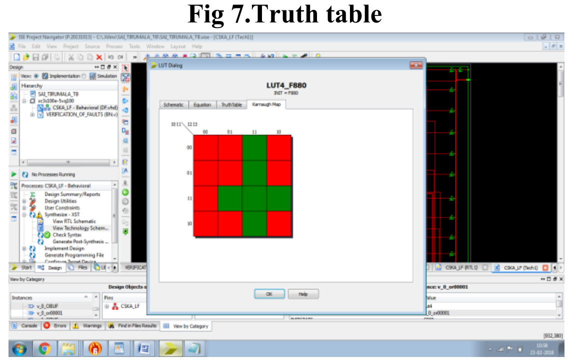

Fig 8. K MAP

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 04
February 2018

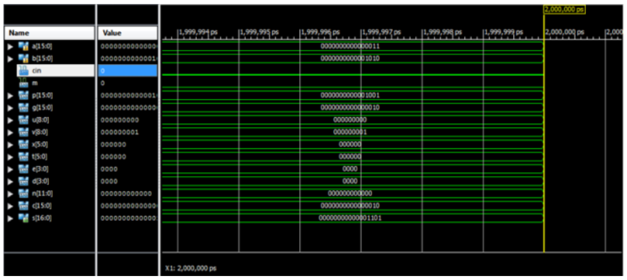

Fig 9. Output Waveform

V.CONCLUSION

In this paper, a new approach is implemented to design an efficient Ladner-Fischer adder which concentrates on gate levels to improve the speed and decreases the memory. It is like tree structure and cells in the carry generation stage are decreased for speed up the binary addition. In proposed adder addition operation offers a great advantage in reducing the delay.

VI.REFERENCES

[1]. Alioto. M and Palumbo.G, "A simple strategy for optimized design of one-level carry-skip adders,"(2003) IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 50, no. 1, pp. 141–148,.

[2]. Chang. C.-H, Gu.J, and M. Zhang, "A review of 0.18 µm full adder performances for tree structured arithmetic circuits," (2005)IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686– 695.

[3]. Chirca.K et al., "A static low-power, highperformance 32-bit carry skip adder,"(2004) in Proc. Euromicro Symp. Digit. Syst. Design (DSD), pp. 615–619.

[4]. Dreslinski .R. G, Wieckowski.M, Blaauw. D , Sylvester D., and Mudge. T, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," (2010) Proc. IEEE, vol. 98, no. 2, pp. 253–266,.

[5]. Harris. T, taxonomy of parallel prefix networks," (2003) in Proc. IEEE Conf. Rec. 37th Asilomar Conf. Signals, Syst., Comput., vol. 2, pp. 2213–2217.

[6]. He .Y, and Chang. C.-H, "A power-delay efficient hybrid carrylookahead/ carry-select based redundant binary to two's complement converter,"(2008) IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 1,pp. 336–346.

[7]. Jia.S et al., "Static CMOS implementation of logarithmic skip adder," (2003) in Proc. IEEE Conf. Electron Devices Solid-State Circuits, ,pp. 509–512.

[8]. Jain. S, et al., "A 280 mV-to-1.2 V wide-operatingrange IA-32 processor in 32 nm CMOS," (2012)in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), pp. 66–68.

[9]. Koren.I, Computer Arithmetic Algorithms.(2002) Natick, MA, USA: A K Peters.

[10]. Markovic. D, Wang. C. C, Alarcon. L. P, Liu. T.-T, and Rabaey. J. M,"Ultralow-power design in nearthreshold region,"(2010) Proc. IEEE, vol. 98, no. 2, pp. 237–252.

[11]. Mathew. S. K, Anders. M. A, Bloechel .B, Nguyen.T, Krishnamurthy. R. K, and Borkar. S, "A 4-GHz 300- mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS,"(2005) IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 44–51.

[12]. Oklobdzija.V.G, Zeydel.B.R,. Dao.H.Q, Mathew.S, and Krishnamurthy.R, "Comparison of highperformance VLSI adders in the energy-delay space,"(2005) IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 754–758.

[13]. Ramkumar.B and Kittur.H.M, "Low-power and area-efficient carry select adder,"(2012) IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20,no. 2, pp. 371–375.

[14]. Suzuki.H, Jeong.W, and Roy.K, "Low power adder with adaptive supply

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 04
February 2018

voltage,"(2003) in Proc. 21st Int. Conf. Comput. Design, pp. 103–106.

[15]. Zlatanovici .R, Kao.S, and Nikolic.B, "Energy–delay optimization of 64-bit carry-lookahead adders with a 240 ps 90 nm CMOS design example," (2009) IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 569– 583.

[16]. Milad Bahadori, Mehdi Kamal, Ali Afzali-Kusha, Senior Member, IEEE, and Massoud Pedram, Fellow, IEEE "high-speed and energyefficient carry skip adder operating under a wide range of supply voltage levels"1063-8210 © 2015

[17]. P.Chaitanya kumari1, R.Nagendra2 "Design of 32 bit Parallel Prefix Adders "IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-ISSN: 2278-2834,p- ISSN: 2278-8735. Volume 6, Issue 1 (May. - Jun. 2013),

[18]. Damarla Paradhasaradhi*, Prof. K. Anusudha ' An Area Efficient Enhanced SQRT Carry Select Adder D Paradhasaradhi et al Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013, pp.876-880

[19]. S. K. Mathew, M. A. Anders, B. Bloechel, T. Nguyen,R. K. Krishnamurthy, and S. Borkar, "A 4-GHz 300-mW 64-bitinteger execution ALU with dual supply voltages in 90-nm CMOS," IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 44–51, Jan. 2005.

[20]. V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, andR. Krishnamurthy, "Comparison of high-performance VLSI adders inthe energydelay space," IEEE Trans. Very Large Scale Integr. (VLSI)Syst., vol. 13, no. 6, pp. 754–758, Jun. 2005

AVVARU VIJAY KUMAR Completed his B.Tech in EVM College of Engineering and Technolgy and pursuing M TECH in Sai Tirumala NVR Engineering College.

K.RAMESH BABU Completed his M.Tech. He has 9 years of Teaching experience And at present he is working as Associate Professor in Sai Tirumala NVR Engineering College.