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Power Quality Improvement by Using Less Number of Switches and Reduced Switching Losses with Asymmetric Cascaded H - Bridge Multi-Level Inverter

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ABSTRACT:
Cascaded H-Bridge converter has recently been utilized in different high-power applications due to its modular and simple structure. In order to have a balanced operation after a fault occurrence in this converter, it is necessary to detect the switch fault and its location. In this project, a fast power switch fault detection method is presented to identify the fault and its location. Only one voltage measurement per phase is required by this method, and the fault detection is faster compared to the existing methods. Moreover, it is easy for implementation on an FPGA device, due to the use of simple math, relational and state machine blocks. The proposed method is verified by computer simulations.

Key words :- Power switch fault detection; Open switch fault; Multilevel converter ; Cascaded H-bridge converter Insulated Gate Bipolar Transistor (IGBT).

I.INTRODUCTION

Multilevel converters have been used in recent years in a large number of power electronics applications. They have lots of benefits over the conventional two-level converters that make them interesting choices especially in high-power applications. In these converters, each switching device has to with stand only a portion of the total voltage. Therefore by using several devices, the converter can work with higher voltages compared to the conventional ones. Also these converters produce lower harmonics. Several types of multilevel converters are proposed and used. The most popular structures are the diode clamped [1], flying capacitor [2] and the Cascaded H-Bridge (CHB) converters [3-8].However, having a large number of devices increases significantly the risk of a failure in one of the power converters witches. Therefore it is important to detect and compensate faults occurrence in these converters. Several methods are proposed for the post-fault operation of multilevel converter [9-17] providing the possibility of balanced operation of the converter even after a fault. The faster the fault is detected; the smaller will be its effect on the system performances.

MULTILEVEL CONVERTERS

Converters have attracted significant inter mist for medium/high power applications [1]–[3]. Among various multilevel converter topologies [4], the flying capacitor (FC) converter [5] offers some advantages over the neutral-point-clamped (NPC) converter [6], such as that capacitor volt-age balance can be achieved without producing low-frequency voltage ripples in the FCs, even in converters with a large number of levels.

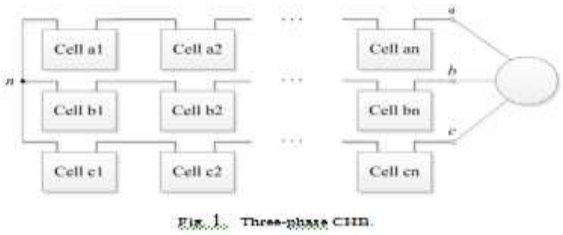

Fig1.1 three- phase CHB

FC CONVERTER AND PD-PWM

FUNDAMENTALS: Fig. 1 shows a phase-leg of an *n*-level FC converter, which integrates *n*–2 FCs. The subscript *x* is used for the phase identification *x*= {*a, b, c*}. The switch pairs in each phase-leg $s_{x1} - \bar{s}_{x1}$,$s_{x2} - \bar{s}_{x2}$,..., and$s_{xn-1} - \bar{s}_{xn-1}$operate in a complementary manner. During normal operation, the mean voltage values of the FCs, C_{x1} ,C_{x2} ,..., and C_{xn-2} , should be maintained

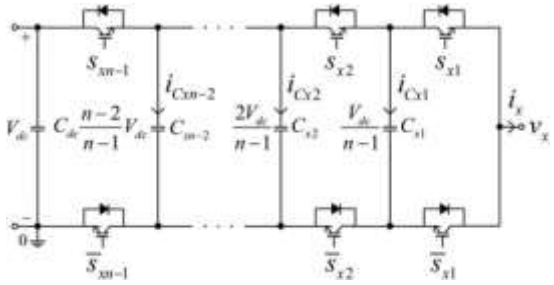

Fig.1.2 Phase-leg of a five-level FC Converter.

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At $V_{dc}/(n-1)$, $2V_{dc}/(n-1)$,..., and $(n-2)V_{dc}/(n-1)$, respectively, where V_{dc} is the dc-bus voltage. Consequently, the voltage across each switch is only $1/(n-1)$ of the dc-bus voltage. Each converter phase-leg can generate $n-1$ output voltage levels, i.e., 0, $V_{dc}/(n-1)$, $2V_{dc}/(n-1)$,..., $(n-2)/(n-1)V_{dc}$, and V_{dc} , with respect to the dc negative rail "0."

HISTORY OF MULTI-LEVEL INVERTERS

Conventional two-level topology is the most common inverter topology and has been used for many years in industry. The term "two-level" is derived from the number of output voltage levels the inverter can generate. If the DC link voltage of a two-level inverter is assumed to be , its output voltage has the values { and }, or { / and /}. This family of inverters typically takes advantage of simple structure and control strategy. A three-phase two-level inverter contains six applications. The primary disadvantage of two-level inverters is that they usually operate in higher switching frequencies, consequently increasing the total loss of the system. Moreover, the output waveform of a two-level inverter contains a large number of harmonics, resulting in the use of more expensive output filters.

TYPES OF TOPOLOGYS

DIODE-CLAMPED (DC) TOPOLOGY

The diode-clamped (DC), also called neutral-point clamped (NPC), topology is based on the utilization of a number of diodes in order to block small DC sources. The configuration of a single-phase 3-level and 5-level diode-clamped inverter is shown in Figure 2.2.

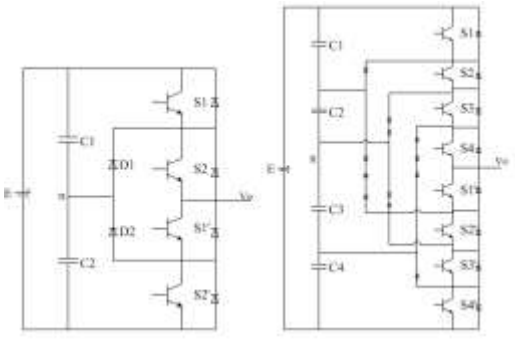

Figure 2.1 Single-phase 3-level and 5-level DC topology

The DC topology can easily be extended to a generic n-level configuration. In a 3-level diode-clamped inverter, the DC bus voltage is divided by capacitor banks into two equal steps. Operation of the inverter is simple. The name of the DC topology originates from the fact that the voltage between two switches is clamped through the clamping diodes. When switches are(s1,s2) *on* and are($s1's2'$) *off*, output voltage of the inverter is equal to the voltage of , which is equal to /. Likewise, when switches (s1,s2) are *off* and($s1's2'$) are *on*, output voltage of the inverter is equal to the voltage of , which is equal to-E/2. When are *on* and are *off*, output voltage of the inverter is equal to 0.

In a 5-level diode-clamped inverter, the DC bus voltage is split into four equal voltage steps. In this case, the number of diodes required to clamp the voltage changes point by point. Each diode is sized to provide voltage blocking for the voltage across one capacitor. For instance,D1 is represented only by one diode, while D1'is represented by three diodes equal toD1 , which are in series because it must block voltage across capacitors c2, c3, and c4, meaning that it is allowed to use one diode with higher blocking capability or three diodes in series with equal blocking capability toD1 . Considering the diode reverse voltage for an n-level inverter, calculated by vr=E/n-1 , Operation of 3- and 5-level NPC topology is shown in Table 2.1 and 2.2, respectively.

Switches				Output Voltage
S1	S2	S1'	S2'	Vo
1	1	0	0	$+E/2$
0	1	1	0	0
0	0	1	1	$-E/2$
1	0	0	1	N/A

Table 2.1 Switching table for the 3-level DC topology

Switches								Output Voltage
S1	S2	S3	S4	S1'	S2'	S3'	S4'	Vo
1	1	1	1	0	0	0	0	+E/2
0	1	1	1	1	0	0	0	+E/4
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-E/4
0	0	0	0	1	1	1	1	-E/2

Table 2.2 Switching table for the 5-level DC topology

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In Table 2.1 and 2.2, the on-state and off-state of the switches is shown by 1 and 0 , respectively. Any shortcut should be avoided in each of the switching states, meaning that all switches cannot be turned on simultaneously. In addition si, and si ‘, where is the number of the switches, should be switched in a complementary way. For instance, when s1is *on*, s1’should be *off* and vice versa. This has to happen for all the other switches.

FLYING CAPACITOR (FC) TOPOLOGY

This topology is similar to diode-clamped topology in which diodes are replaced by capacitors in order to maintain voltage levels across DC link capacitors. Figure 2.3 shows the structure of a single-phase 3-level and 5-level flying-capacitor inverter. The topology has a ladder structure of DC dice capacitors, in which, the voltage on each capacitor differs from voltage of the next capacitor. FC topology can easily be extended to higher levels. Voltage across each capacitor is given by:

vc=E/n-1

This voltage is the reverse voltage drop each switch can withstand when all capacitors are fully charged. These capacitors are known as clamping capacitors because their function of them is similar to the clamping diodes in diode-clamped topology because they maintain the voltage drop between the buses to which they are connected.

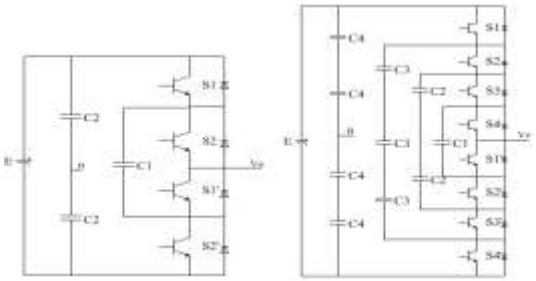

Figure 2.2 Single-phase 3-level and 5-level FC topology

OTHER MULTI-LEVEL TOPOLOGIES

Introduction of the first multi-level topologies dates back to almost three decades ago. However, new concepts of multi-level topologies have emerged in recent years. In addition to basic multi-level topologies introduced in Section 2.2, numerous other multi-level topologies originate from the fundamental topologies.

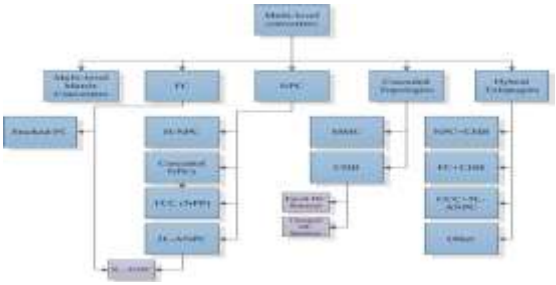

Figure 2.4 Classification of multi-level voltage source converters

PULSE WIDTH MODULATION AND TOTAL HARMONIC DISTORTION

The energy that a switching power converter delivers to a motor is controlled by Pulse Width Modulated (PWM) signals, applied to the gates of the power transistors. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. There is one pulse of fixed magnitude in every PWM period. However, the width of the pulses changes from period to period according to a modulating signal.

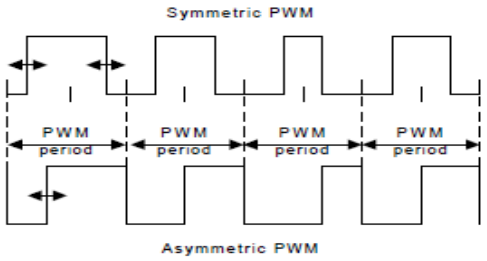

Fig 4.1 two types of PWM signals

TOTAL HARMONIC DISTORTION: Harmonic problems are almost always introduced by the consumers’ equipment and installation practices. Harmonic distortion is caused by the high use of non-linear load equipment such as computer power supplies, electronic ballasts, compact fluorescent lamps and variable speed drives etc, which create high current flow with harmonic frequency components. The limiting rating for most electrical circuit elements is determined by the amount of heat that can be dissipated to avoid overheating of bus bars, circuit breakers, neutral conductors, transformer windings or generator alternators.

Definition: THD is defined as the RMS value of the waveform remaining when the fundamental is removed.

A perfect sine wave is 100%, the fundamental is the system frequency of 50 or 60Hz. Harmonic distortion is caused by the introduction of waveforms at frequencies in multiplies of the fundamental i.e.: 3rd harmonic is 3x the fundamental frequency / 150Hz. Total harmonic distortion is a easurement of the sum value of the waveform that is distorted.

Power Measurement

Despite the use of good quality test meter instrumentation, high current flow can often remain undetected or under estimated by as much 40%. This severe underestimation causes overly high running temperatures of equipment and nuisance tripping. This is simply because the average reading test meters commonly used by maintenance technicians, are not designed to accurately measure distorted currents, and can only provide indication of the condition of the supply at the time of checking. Power quality conditions change continuously and only instruments offering true RMS measurement of distorted waveforms and neutral currents can provide the correct measurements to accurately determine the ratings of cables, bus bars and circuit breakers.

Neutral Currents

High harmonic environments can produce unexpected and dangerous neutral currents. In a balanced system, the fundamental currents will cancel out, but, triple- N's will add, so harmonic currents at the 3rd, 9th, 15th etc. will flow in the neutral. Traditional 3 phase system meters are only able to calculate the vector of line to neutral current measurements, which may not register the true reading. Integra 1530, 1560 and 1580 offer a 3 phase 4 wire versions with a neutral 4th CT allowing true neutral current measurement and protection in high harmonic environments.

Harmonic Profiles

There is much discussion over the practical harmonic range of a measurement instrument; However study of the harmonic profiles of typically installed equipment can guide the system designer to the practical solution. A typical harmonic profile graph will show a logarithmic decay as the harmonic frequency increases. It is necessary to establish the upper level at which the harmonic content is negligible.

For Example:

A laptop switch mode power supply causes approximately 25% of 3rd harmonic, 19% of 5th harmonic, 10% of 7th harmonic and 5% of 9th harmonic etc. Therefore it can be seen that almost all the harmonic content in an IT dominated load will be below the 15th harmonic. In a 3 phase load incorporating 6 pulse bridge technologies as is common in many variable speed drives, UPS systems and DC converters, similar profiles will be observed but extending to the 25th and 27th harmonic. It can therefore be deduced

That in the majority of industrial and commercial applications an instrument measuring up to the 31st harmonic is ideal.

The Costs

Harmonic currents add to the fundamental load current and can affect revenue billing by introducing errors into kilowatt hour metering systems, which will directly increase the net billable kilowatt demand and kilowatt hour consumption charges.

The commercial effects of harmonic distortion to power quality are dramatically shorter equipment lifetimes, reduced energy efficiency and a susceptibility to nuisance tripping. The costs of supply interruption are high, however caused, resulting in data corruption, disruption of process manufacturing and failure of telecommunications facilities etc.

FAULT LOCATION IDENTIFICATION

After fault detection, it is necessary to detect the fault locations well. Here, a simple yet effective method is used based on the fact that when the command of the faulty switch goes back to zero, the voltage error will also disappear, because the converter will act normally again, The third comparison and moving sum unit detect the fault removal, and signal it to the fault detection state machine (FDSM). As it is visible in Fig. 4,when the error voltage is less than C v and larger than -Cv format least Ct samples, one can be sure that there is no fault in the system, and the Fault Jemoved input of the FDSM will become equal to l.

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The FDSM is shown in Fig. 4.3.If a fault is already detected, one of the Fault""positive or Fault negative states in FDSM are active, and the SM is wait U;-g for the Fault removal signal (Fault removed) to arrive, When this signal arrives, it is only necessary to investigate in which cell(s) a switching is occurred in the previous Ct samples. This is done with the help of Dip and Din signals, For each cell, these signals basically show if that in the last Ct sampling a switching is commanded that increase or decrease the cell's output voltage. Fig, 6 shows the Dip and Din generation for one cell. Basically a switching in S1 or S4 will tend to increase the output voltage by VDC while a switching in S2 or S3 will decrease it by VDC ' If the error has been positive and the fault removal signal arrives, it can be concluded that a decreasing switching has been occurred, which corresponds to one Din signal going high. Based on the Din signals, the next state in the FDSM can be detected. For a negative error similar reasoning applies. The FDSM stays in the faulty states (FauI Un_Ci , i E {1: N}) upon entering them, as long as a reset signal is not applied. Finally, the Faul Un_Ci outputs go high when the corresponding state is active. These outputs may be used in the fault tolerant scheme, to reconfigure the structure and control appropriately. In Fig. 4.5, their information is combined to determine the faulty cell's number. It is worth mentioning that after reconfiguration, the FDSM can be reset, and fault detection will be again possible for other switches, as long as the necessary changes in the calculation of the estimated voltage are applied. One special condition is particularly interesting, when two switching's have occurred in two legs during the last Ct sampling periods, because it is important to detect which one has been responsible for fault removal. In another words, it is important that in the observation window, only one Dip and Din are present, otherwise the FDST cannot decide between two Dip or Din signals. Fig.7 shows an example of such condition for a Phase Shifted PWM (PSPWM). Referring to Fig.3, it can be verified that when a carrier becomes larger than the modulation signal, voltage of the corresponding cell will experience a +VDC change (rising level) and vice versa. The modulation signal frequency is several times smaller than the carrier frequency, therefore it can be visually confirmed in Fig.7 that the minimum time between two +VDC or two-VDC.

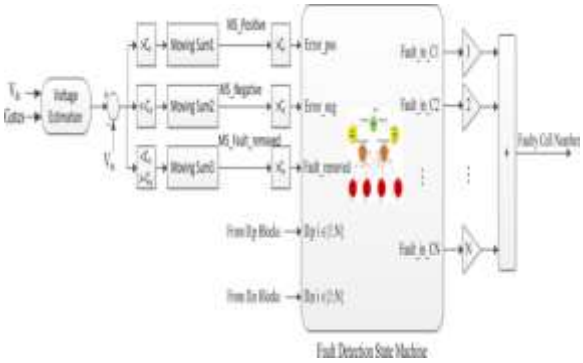
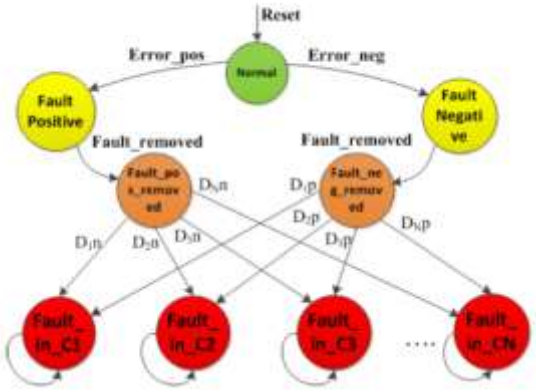
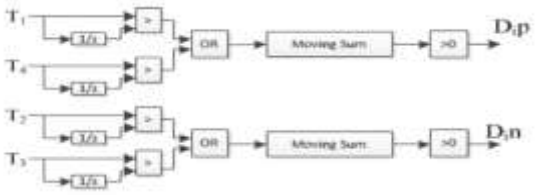


Fig: 4.3 Proposed fault detection scheme for CHB converter



Fault detection State machine



Generation of Dip and Din signals

SIMULATIONS AND EXPERIMENTAL RESULTS:

Simulations are carried out to evaluate the effectiveness of the proposed method. Simulations are performed in the MATLAB/Simulink environment. A five-cell (II-level) three-phase CHB converter is simulated. DC-link voltages of the cells are equal to 1700 V. The fundamental switching frequency is equal to 1000 Hz, resulting in a 2 * n * i = 2 * 5 * 1000 = 10 (kHz) equivalent switching frequency. We consider an open-loop control of the converter and using PSPWM, it generates a sinusoidal voltage at the converter's output. A fault is introduced in switch S 1 of cell 2 at t=O.035s.

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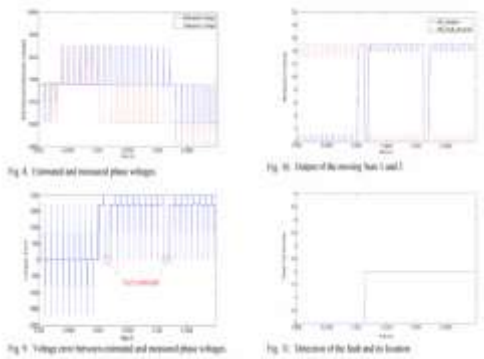
The fault detection algorithm operates with a 500 kHz clock. As soon as the estimated and measured voltages are different ,based on the sign of the voltage error, the MS positive or MS _negative (ref. Fig. 4) signals will start to increase, and when one of them becomes greater than 12, the fault is detected and one of the Fault positive or Fault _negative states will become active.



Here, the estimated and measured voltages of the faulty phase are shown in Fig. 8. The voltage error is shown in Fig. 9. As it was expected, a fault in S 1 has resulted in a +VDC error in phase voltage. It is also shown in this figure that in certain periods of time, the voltage error disappears. This is due to a decreasing switching command, and is used for identification of the fault's location .Outputs of the Moving Sum I and Moving Sum 3 blocks are shown in Fig. 5.5 When it passes Ct= 12, a fault can be declared, and the FDSM goes to the Fault positive state. MS_ Fault removed signal starts to increase when the converter is acting normal or when the voltage error is smaller than its limits. It can be seen that during normal operation of the converter, this signal has a usually high value, but immediately after the fault occurrence at t=0.035, it goes down to zero. However, when the fault is removed due to switching in the faulty cell, this signal goes high again. Fig. 11 shows the moment that the FDSM has reached its final stage, as well as the final result. Fault location is correctly detected. Also the fault detection has been very fast. The fault is detected in less than 2001lS.Fig. 12 shows the details of the identification of fault location.

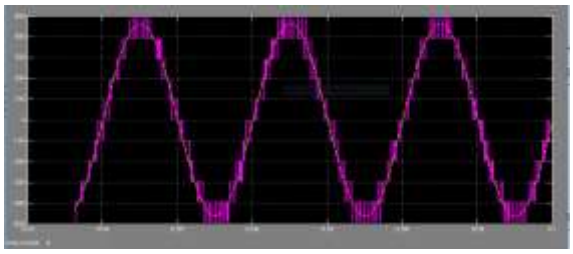


Fig 5.7 output of the moving suml and sum 3

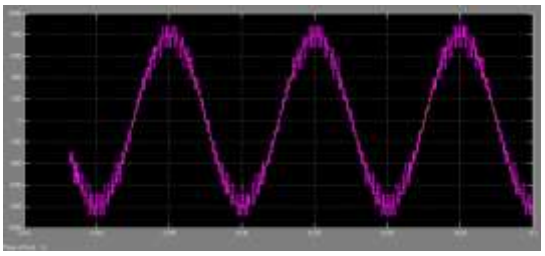


Fig 5.8 output of the moving sum 2 and sum 4

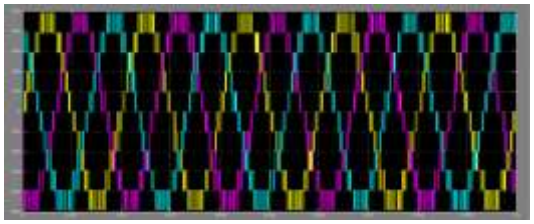


Fig 5.9 output wave form of 3-phase cascaded H-bridge multilevel inverter

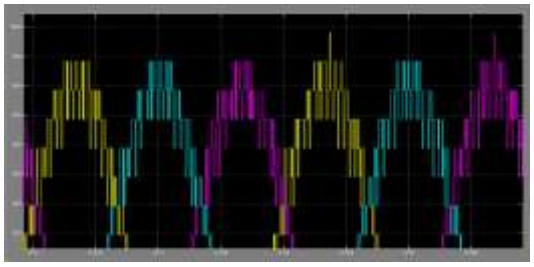


Fig 5.10 3 phase outputs of the moving sum 1 and sum 3

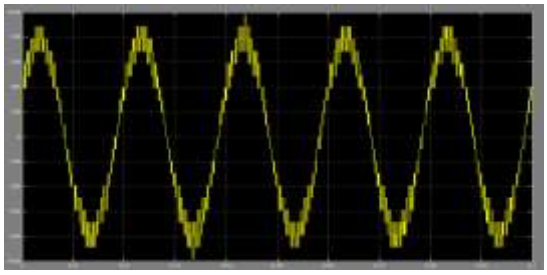


Fig 5.11 output waveform of cascaded H- bridge multi level inverter

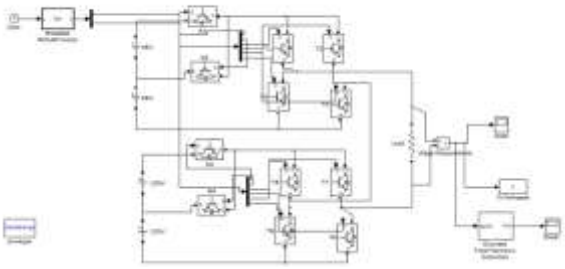


Fig 5.12 simulation diagram Asymmetric cascaded H-bridge multi level inverter

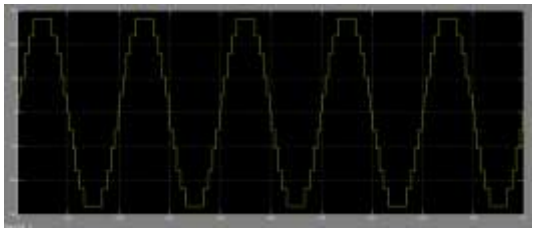


Fig 5.13 Output of Asymmetric cascaded H-bridge

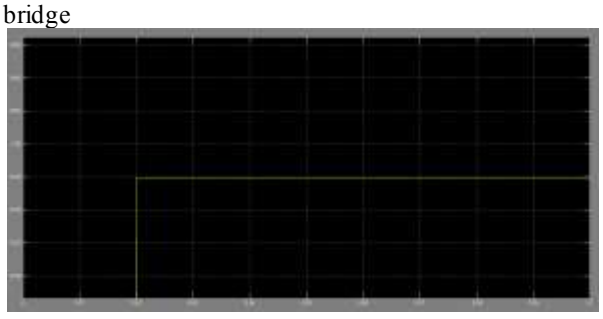


Fig: 5.14 Detection of the fault and its location.

CONCLUSION

In this Project, a very fast method for detection of open-switch faults in cascaded H-bridge converters is proposed. This method only needs one voltage measurement per phase, and is fast and robust for the detection of semiconductor open-switch fault and its location. The proposed method detects the fault by comparing the estimated and measured phase voltages of the converter. Fault location is found based on the fact that when the faulty switch command is equal to zero, converter will act normal again. Only simple math, relational and state machine blocks are used and therefore the implementation of this approach on a digital target like FPGA will be easy. The detection time will be at maximum equal to one switching period and can be as low as a few tens of microseconds. Simulation results show the high performance of the proposed method.

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