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Closed Loop Control of PV fed High Voltage Gain DC-DC converter with Two-Input Boost-Stages

Gujju Nooratham Reddy & M.V.S Prem Sagar
M.Tech student scholar Department of Electrical & Electronics Engineering BABA Institute of Technology and Sciences Visakhapatnam, A.P, India.
E-mail:gujju.gnr@gmail.com
Assistant Professor Department of Electrical & Electronics Engineering BABA Institute of Technology and Sciences Visakhapatnam, A.P, India.
E-mail:ajay3359@gmail.com

Abstract-*DC-DC converter is a device which produces a dc output voltage when a dc input is given. If output voltage needed is higher than input voltage we go for boost converter. The conventional boost converter can be used for step up applications because of low conduction loss, simple structure and low cost. However, it is not suitable for high step-up applications. Generally conventional boost converters have been used to obtain higher output voltage than the input voltage. When these boost converters are operated for high ratios it leads to high voltage and current stress on the switch. Hence an interleaving technique of boost converter has been presented. This method of approach can be used in high power applications to produce high voltage gain when compared to the conventional boost converter. A simple dc-dc boost converter are unable to provide high step-up voltage gains due to the effect of power switches, rectifier diodes, and the equivalent series resistance of inductor and capacitors. In this paper proposes new dc-dc converter to achieve high voltage gain without an extremely high duty ratio. In the proposed converters, two inductors with the same level of inductance are charged in parallel during the switch –on period and are discharged in series during the switch-off period. In this converter mainly proposed converter. That is used for PV system. To achieve high-voltage conversion ratios, a new family of high-voltage-gain dc–dc power electronic converters has been introduced. The proposed converter can be used to draw power from two independent dc sources as a multiport converter or one source in an interleaved manner. They draw continuous input current from both the input sources with low current ripple which is required in many applications, e.g., solar. Several diode-capacitor stages are cascaded together to boost up the voltage which limits the voltage stresses on the switches, diodes, and capacitors.*

II. Topology Introduction and Modes of Operation

The proposed converter is inspired from a Dickson charge pump [20]. Diode-capacitor VM stages are integrated with two boost stages at the input. The VM stages are used to help the boost stage achieve a higher overall voltage gain. The voltage conversion ratio depends on the number of VM stages and the switch duty ratios of the input boost stages. Fig.1 shows the proposed converter with four VM stages. For simplicity and better understanding, the operation of the converter with four multiplier stages has been explained here. Similar analysis can be expanded for a converter with N stages.

For normal operation of the proposed converter, there should be some overlapping time when both the switches are ON and also one of the switches should be ON at any given time (see Fig.2). Therefore, the converter has three modes of operation. The proposed converter can operate when the switch duty ratios are small and there is no overlap time between the conduction of the switches. However, this mode of operation is not of interest as it leads to smaller voltage gains.

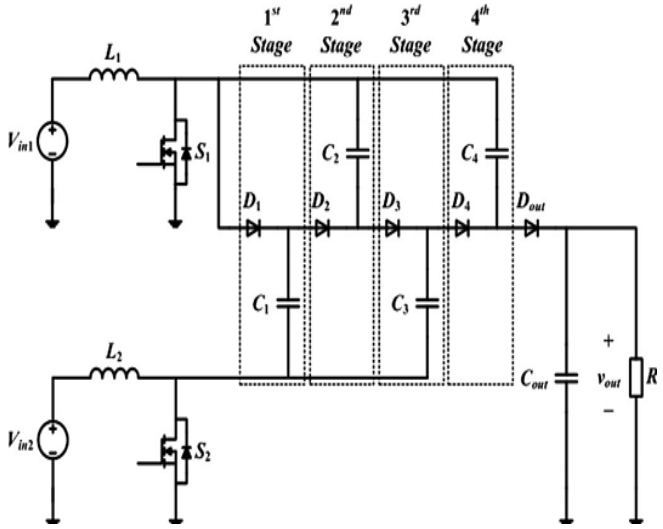

Fig.1. Proposed high-voltage-gain dc–dc converter with four VM stages.

A. Mode-I

In this mode, both switches S1 and S2 are ON. Both the inductors are charged from their input sources Vin_1 and Vin_2. The current in both the inductors rise linearly. The diodes in different VM stages are reverse biased and do not conduct. The VM capacitor voltages remain unchanged and the output diode Dout is reverse biased (see Fig.3); thus, the load is supplied by the output capacitor Cout.

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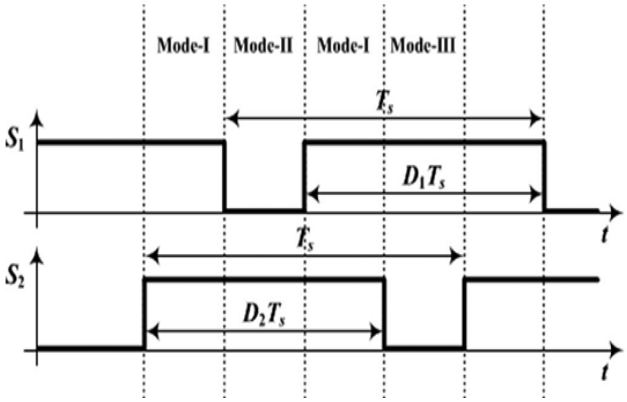

Fig.2. Switching signals for the input boost stage for the proposed converter.

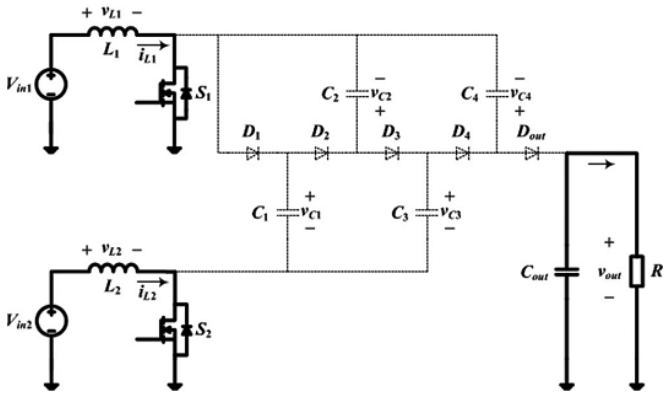

Fig.3. Mode-I of operation for the proposed converter with four VM stages.

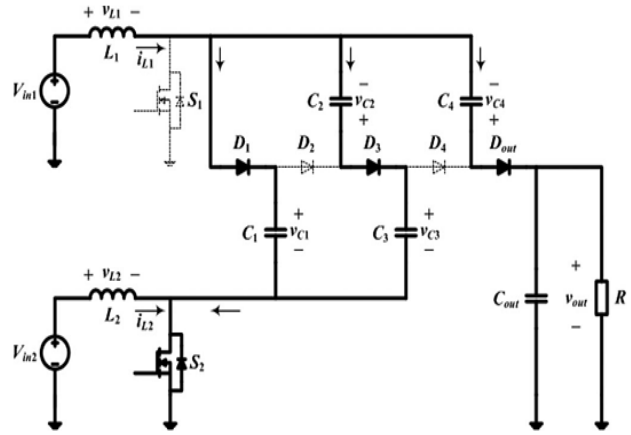

Fig.4. Mode-II of operation for the proposed converter with four VM stages.

B. Mode-II

In this mode, switch S1 is OFF and S2 is ON (see Fig.4). All the odd numbered diodes are forward biased and the inductor current IL1 flows through the VM capacitors charging the odd numbered capacitors (C1,C3,...) and discharging the even numbered capacitors (C2,C4,...). If the number of VM stages is odd, then the output diode Dout is reverse biased and the load is supplied by the output capacitor. However, if the number of VM stages is even, then the output diode is forward biased charging the output capacitor and supplying the load.

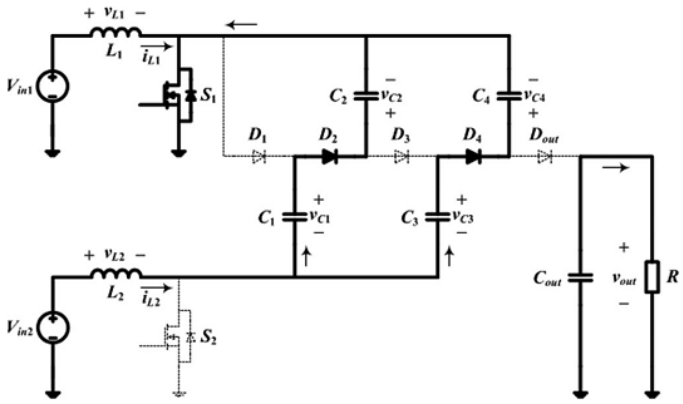

Fig.5. Mode-III of operation for the proposed converter with four VM stages.

In the particular case considered here, since there are four VM stages, the output diode is forward biased.

C. Mode-III

In this mode, switch $S_1$is ON and S2 is OFF (see Fig.5). Now, the even numbered diodes are forward biased and the inductor current IL_2 flows through the VM capacitors charging the even numbered capacitors and discharging the odd numbered capacitors. If the number of VM stages is odd, then the output diode D_{out} is forward biased charging the output capacitor and supplying the load. However, if the number of VM stages is even, then the output diode is reverse biased and the load is supplied by the output capacitor.

III. Voltage Gain of the Converter

The charge is transferred progressively from input to the output by charging the VM stage capacitors. For a converter with four stages of VM (see Fig.1), the voltage gain can be derived from the volt-sec balance of the boost inductors. For L_1, one can write

$$\langle v_{L1} \rangle = 0 \tag{1}$$

Therefore, from Fig.4, it can be observed that the capacitor voltages can be written in terms of upper boost switching node voltage as

$$V_{C1} = V_{C3} - V_{C2} = V_{\text{out}} - V_{C4} = \frac{V_{\text{in1}}}{(1-d_1)} \tag{2}$$

Where d1 is the switching duty cycle for S_1. Similarly, from the volt-sec balance of the lower leg boost inductor L_2, one can write the capacitor voltages (see Fig.5) in terms of lower boost switching node voltage as

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$$V_{C2} - V_{C1} = V_{C4} - V_{C3} = \frac{V_{in2}}{(1-d_2)} \quad (3)$$

Where d_2 is the switching duty cycle for S_2.

From (2) and (3), the capacitor voltages for the proposed converter with four VM stages can be derived as

$$V_{C1} = \frac{V_{in1}}{(1-d_1)} \quad (4)$$

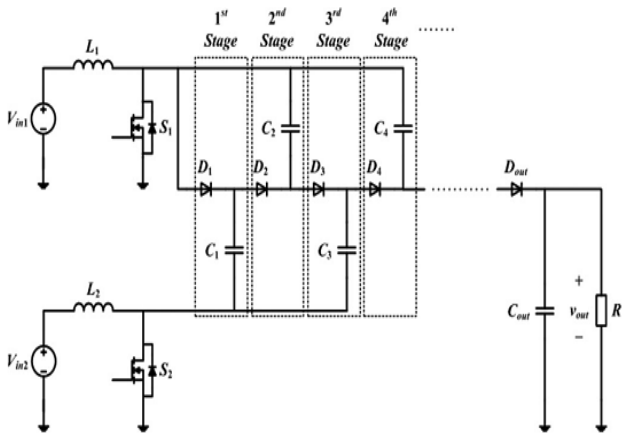

Fig.6. Proposed converter with N number of VM stages.

$$V_{C2} = \frac{V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)}$$

$$V_{C3} = \frac{2V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)}$$

$$V_{C4} = \frac{2V_{in1}}{(1-d_1)} + \frac{2V_{in2}}{(1-d_2)} \quad (5)$$

The output voltage is derived from (2), which is given by

$$V_{out} = V_{C4} + \frac{V_{in1}}{(1-d_1)} = \frac{3V_{in1}}{(1-d_1)} + \frac{2V_{in2}}{(1-d_2)} \quad (6)$$

Similar analysis can be extended to a converter with N number of VM stages (see Fig.6). Thus, the VM stage capacitor voltages are given by

$$V_{Cn} = \left(\frac{n+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{n-1}{2}\right)\frac{V_{in2}}{(1-d_2)}$$

if n is odd &n ≤ N,

$$V_{Cn} = \left(\frac{n}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{n}{2}\right)\frac{V_{in2}}{(1-d_2)}$$

if n is even & n ≤ N.

(7)

The output voltage equation of the converter with N number of VM stages depends on whether N is odd or even and is given by

$$V_{out} = V_{CN} + \frac{V_{in2}}{(1-d_2)} \quad \text{if } N \text{ is odd}$$

$$= \left(\frac{N+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N+1}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad (8)$$

$$V_{out} = V_{CN} + \frac{V_{in1}}{(1-d_1)} \quad \text{if N is even}$$

$$= \left(\frac{N+2}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad (9)$$

When the converter operates in an interleaved manner with single input source, if d_1 and d_2 are also chosen to be identical, i.e., $d_1 = d_2 = d$, then the output voltage is given by

$$V_{out} = (N+1)\frac{V_{in}}{(1-d)} \quad (10)$$

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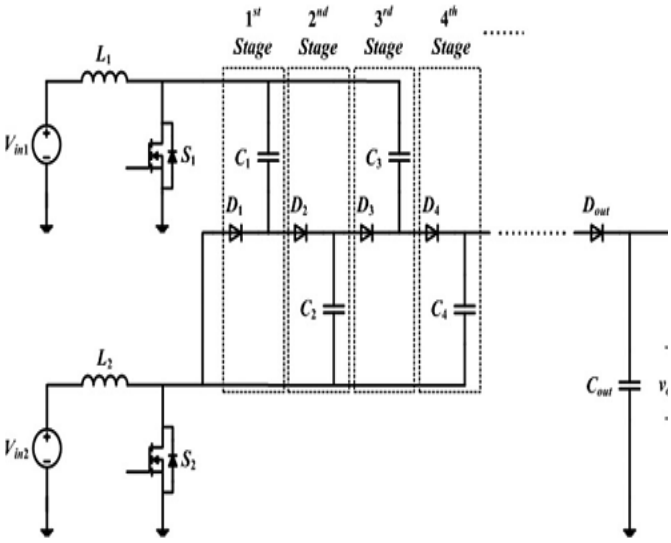

Fig.7. Alternative to the proposed converter with N number of VM stages

In [21], an interleaved boost power factor corrected converter with voltage-doubler characteristics is introduced. It can be observed that it is a special case of the proposed converter with a single VM stage (N = 1).

It is worth noting that there is an alternative to the proposed converter (see Fig.7) where diode D1 of the first VM stage is connected to the lower boost switching node and capacitor C1 is connected to the upper boost switching node (compare with Fig.6).

The output voltage equation for this alternative topology is given by

$$V_{\text{out}} = \left(\frac{N+1}{2}\right)\frac{V_{\text{in1}}}{(1-d_1)} + \left(\frac{N+1}{2}\right)\frac{V_{\text{in2}}}{(1-d_2)} \quad \text{if } N \text{ is odd} \tag{11}$$

$$V_{\text{out}} = \left(\frac{N}{2}\right)\frac{V_{\text{in1}}}{(1-d_1)} + \left(\frac{N+2}{2}\right)\frac{V_{\text{in2}}}{(1-d_2)} \quad \text{if } N \text{ is even.} \tag{12}$$

For N = 1, if one combines the topology depicted in Fig.6 with its alternative (see Fig. 7), then the resulting converter in Fig.8 is similar to the multiphase converter introduced in [22].

In general, when both topologies with N number of VM stages are combined, then the resulting converter is shown in Fig.9. When N is odd, then from (3.7) and (3.10), the voltage gain of the combined topology is given by

$$V_{\text{out}} = \left(\frac{N+1}{2}\right)\frac{V_{\text{in1}}}{(1-d_1)} + \left(\frac{N+1}{2}\right)\frac{V_{\text{in2}}}{(1-d_2)} \quad \text{if } N \text{ is odd.} \tag{13}$$

In this case, the original topology and its alternative each process half of the output power. In other words, the average currents of Dout1 and Dout2 are equal.

When N is even, the output voltage of the combined topology would be either (3.8) or (3.11) and will be dictated by the topology that provides a higher output voltage. Both legs (see Fig.9) would compete with each other and only one of the output diodes (Dout1 and Dout2) would process the entire power while the other will be reverse biased. When N is even, putting the converters in parallel only makes sense if there is only one source used and $d_1 = d_2$. In that case both (3.8) and (3.11) determine the output voltage.

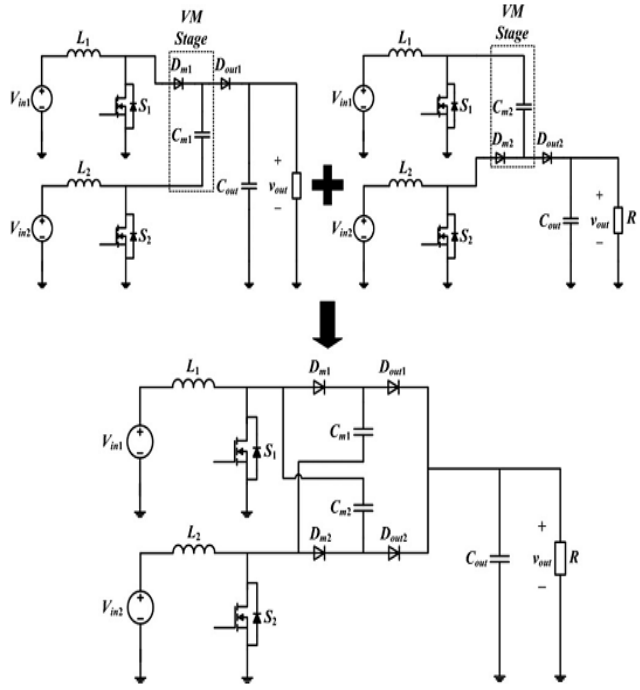

Fig.8. Combined topology with single VM stage.

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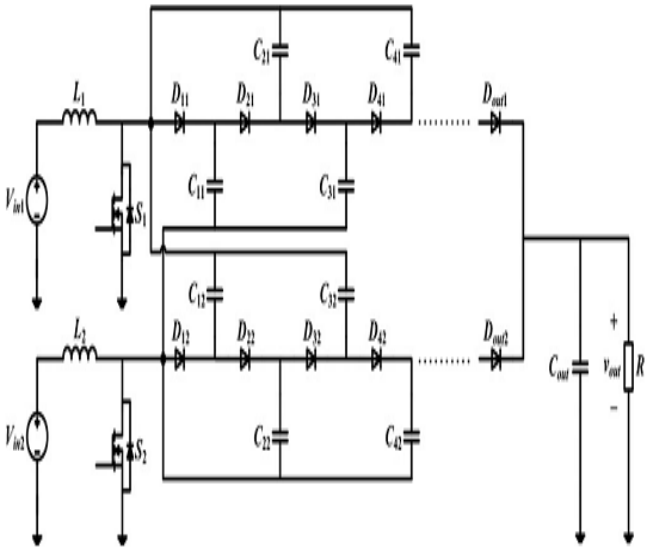

Fig.9. Combined topology with N number of VM stages.

$$V_{\text{out}} = (N+1)\frac{V_{\text{in}}}{(1-d)} \quad \text{if } N \text{ is even} \tag{14}$$

For the combined topology with a single input source and identical duty ratios d1 and d2, i.e., d1 = d2 = d, both the boost stages will always have symmetrical inductor and switch currents irrespective of the number of VM stages.

IV. MATLAB/SIMULINK RESULTS:

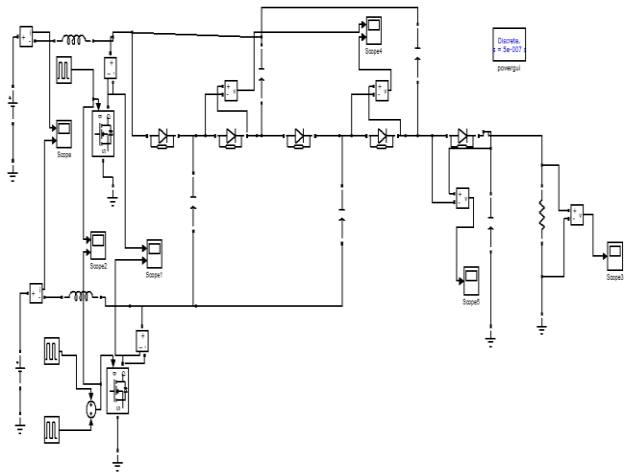

Fig.10. Matlab/simulink Model for Proposed with Two Input Boost Stages

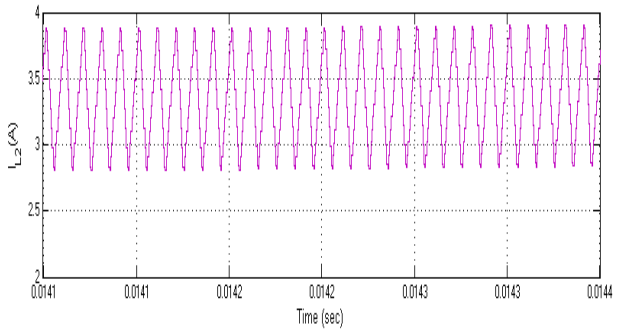

Fig.11. Inductor Current (I_{L2})

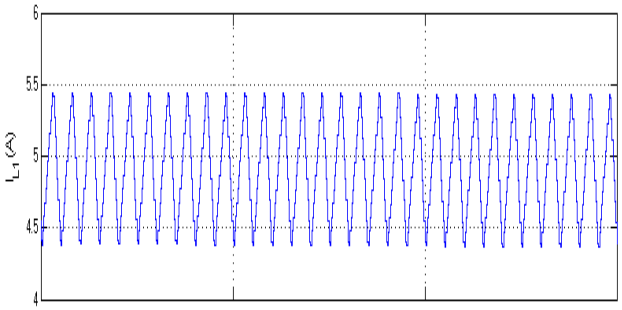

Fig.12. Inductor Current (I_{L1})

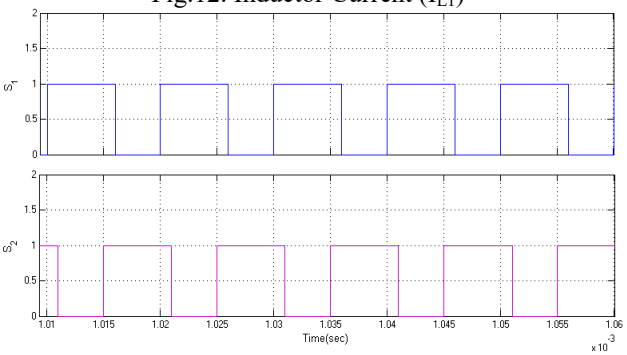

Fig.13. Switch Gating Pulses S_1, S_2

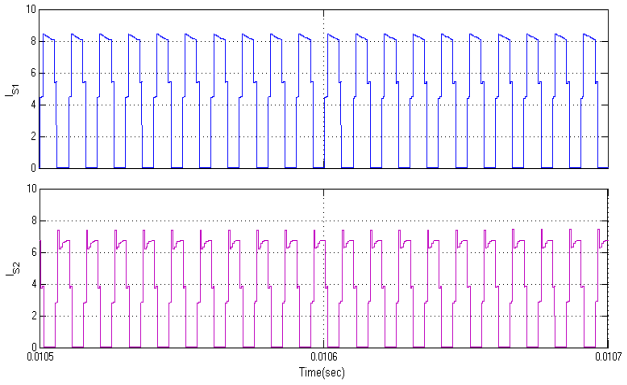

Fig.14. Switching Currents I_{S1}, I_{S2}

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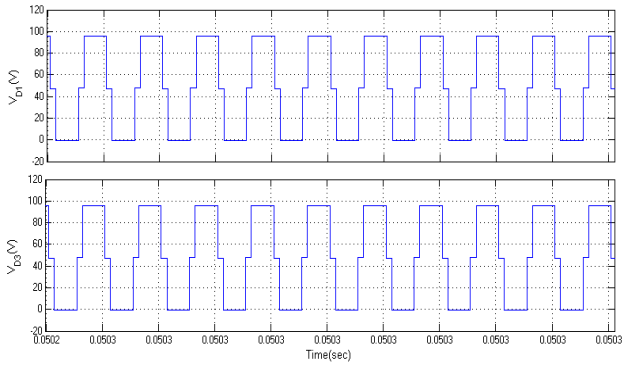

Fig.15. Diode Voltages V_{D1}, V_{D3}

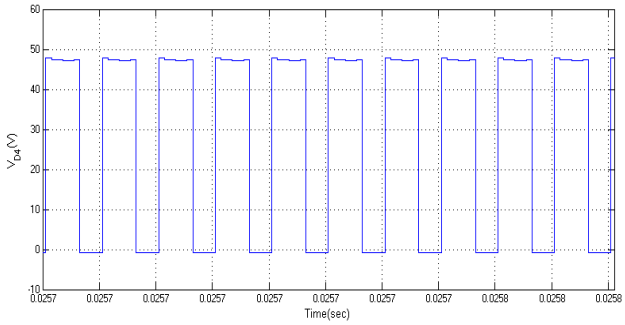

Fig.16. Diode Voltage V_{D4}

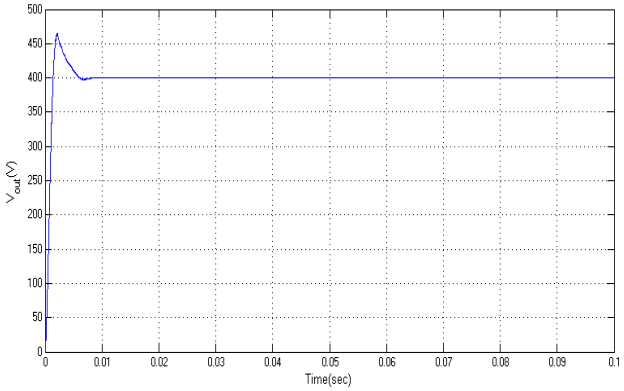

Fig..17. Output Boost Voltage V_0.

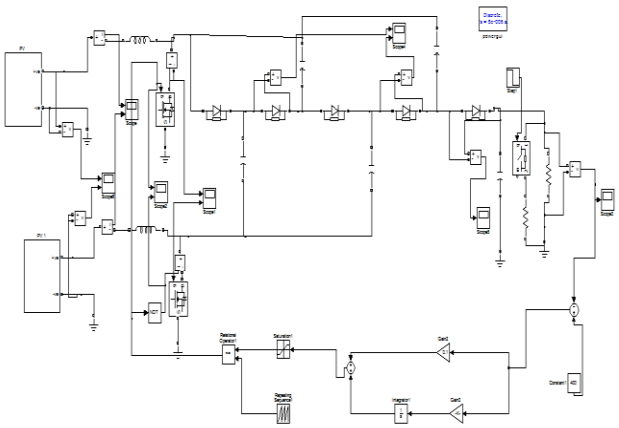

Fig.18. Matlab/simulink Model of Proposed converter with PV Fed Closed loop operation.

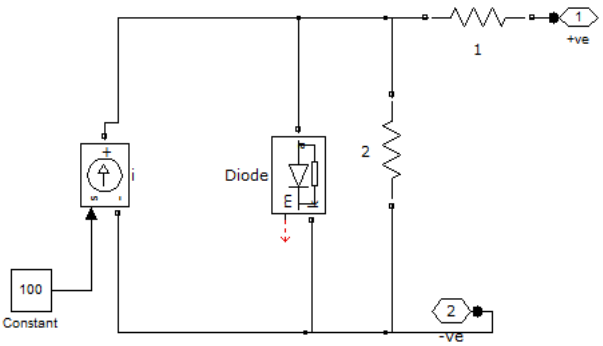

Fig.19. Matlab/simulink Model for PV System.

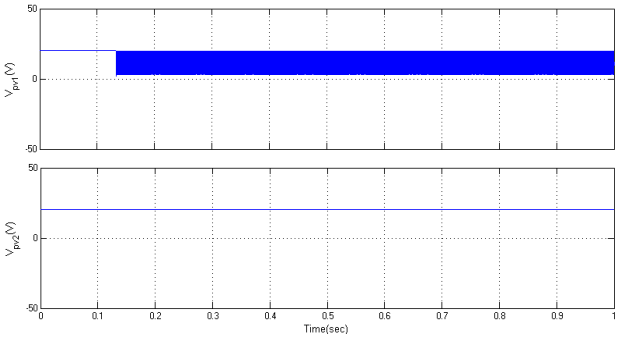

Fig.20. Source Voltages V_{PV1}, V_{PV2}

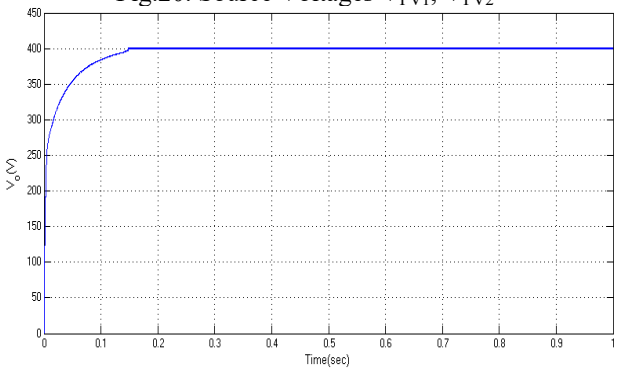

Fig.21. Output Voltage.

V. CONCLUSION

In this paper, a family of novel high-voltage-gain dc–dc converters with two boost stages at the input has been proposed. The proposed converter is based on diode–capacitor VM stages and the voltage gain is increased by increasing the number of VM stages. It can draw power from two input sources like a multiport converter or operate in an interleaved manner when connected to a single source. One of the advantages of the proposed converter is that since it is a multiport converter with high voltage gain, it has the flexibility to be connected to independent sources while allowing power

sharing, MPPT algorithms etc., to be implemented independently at each input port. Furthermore, an alternative topology of the proposed converter has been presented and combining them both would result in a new converter topology. The proposed converter can be used for solar applications where each panel can be individually linked to the 400-V dc bus.

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