Performance Study of Robust Router using VHDL

[1]Ch.Surendra, [2] A.Phanindra Babu

[1]M.Tech Research Scholar, Priyadarshini Institute of Technology & Science, Chintalapudi
[2]Assistant Professor, Priyadarshini Institute of Technology & Science, Chintalapudi

Abstract: *The swell in the numeral of cores that can be incorporated on a distinct chip has forced the designer to use computer system concepts for design of System on Chip (SoC).The supplementary is of multiple protocols being used in the diligence at present. For larger networks, where a direct mapped loom is not viable due to FPGA reserve limitations, a virtualized time multiplexed loom was used. Compared to the provided software reference execution, our direct-mapped loom achieves three orders of enormity expedite, while our virtualized time multiplexed loom achieves one to two orders of enormity expedite, depending on the set-up and router design. This paper is based on the hardware coding which will give a great impact on the latency issue as the hardware itself will be designed according to the need. In this article our endeavor is to afford a flexible networking router by means of Verilog code, being generated by code in our design in the so we call this as the self-independent router called as the VLSI Based router. This paper focus upon the actual implementation of Network Router and verifies the functionality of the three port router for system on chip using the newest authentication methodologies, Hardware authentication Languages and EDA utensils and thrive the IP for blend an execution. This manuscript thus is going to be a radical enhancement in the province of networking.*

Keywords--Network-on-Chip; Simulation Router; FIFO; FSM; Register blocks

I. INTRODUCTION

New developments are necessary in every field, especially in technology, to improve quality of life. As we know this is the era of research and there is research in every field of life. In electronic, more emphasis is on how to reduce the chip area, its cost and how to develop a product in short interval of time. Integrating a complete system on a single chip is known as “System on Chip”. A lot of work has been done in this field. A regular increase in the number of transistors on a single chip has opened new fields and makes it possible to develop more complex systems on a single chip. Due to the increased complexity, there was a need of introducing a platform which makes it easy to integrate new component on a single chip with reduced complexity. In the last few years, a platform has been introduced name as Network on Chip (NOC). Our approach here is to design a variable hardware router code by using Verilog and the same

to be implemented for the SOC (System OnChip) level router. In this paper we are making a VLSI design for the implementation at the synthesizable level the same can be further enhanced to SOC level .Due to the increase of numbers of transistors on a single chip, it is possible to develop more complex systems on a single silicon chip. The whole system is integrated in the using components which are called IP cores. These IP cores are directly connected to communicate with each other.

These IP cores can be reused in different systems. These cores can be processors, I/O controllers, memory blocks, DSPs,video controller and many others. Increase in number of cores will increase interconnects complexity on the chip. This project helps one to understand the complete functional verification process of complex ASICs an SoC's and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and urbane EDA tools, for the high quality verification. In research work, goals are of great importance. Appropriate goals become cause of good research. The goal in this hypothesis is to design router architecture for junction based source routing. Junction based source routing needs two kind of router design: one for normal router and other for junction router. In the options it was decided that we will intend a single router which works as normal router as well as junction router.

II. SESTYM-ON- CHIP(SOC) CONCEPT

System-on-chip has been a nebulous term that mystically holds out a lot of excitement, and has been gaining momentum in the electronics industry. While the potential is huge, the complexities are several, and countering these to offer successful designs is a true engineering challenge. These trends are ample evidence that SoCs are growing in importance in the semiconductor industry. The reasons are not far to look: SoCs make available, on a single piece of silicon, the embedded IP and high system-level integration required for performance demanding applications today. This enables semiconductor manufacturers to cost-effectively meet specific system requirements while delivering competitive time-to-market advantage. Paradoxically, if the opportunities look promising, the challenges are no less daunting. While opportunities come in the form of drastic reduction in the overall cycle time of the system with superior performance levels, challenges are in the form of deep sub-micron complexities, faster timing closure requirements, verification challenges and the need for an extensive portfolio for pre-verified IP components. How then does one adopt efficient methodologies and processes, and what are the strategies of effective SoC designs? At Wipro Technologies, we translated a decade of ASIC and VLSIdesign experience into a proven design methodology flow for complex SoCs. SoC designs typically exhort several man-hours of skilled engineering resources. In catering to a competitive market with shortened product cycle times, it is important to offer tangible reductions in design cycle time. Two key aspects

III. FUNCTIONALITY OF A ROUTER

A router is a device that forwards data packets between computer networks. This creates an overlay internetwork, as a router is connected to two or more data lines from different networks. When a data packet comes in one of the lines, the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table or routing policy, it directs the packet to the next network on its journey. Routers perform the "traffic directing" functions on the Internet. A data packet is typically forwarded from one router to another through the networks that constitute the internetwork until it reaches its destination node.

The most familiar type of routers are home and small office routers that simply pass data, such as web pages, email, IM,and videos between the home computers and the Internet. An example of a router would be the owner's cable or DSL router, which connects to the Internet through an ISP. More sophisticated routers, such as enterprise routers, connect large business or ISP networks up to the powerful core routers that forward data at high speed along the optical fiber lines of the Internet backbone.

Though routers are typically dedicated hardware devices, use of software-based routers has grown increasingly common. What defines a router is not its shape, color, size or manufacturer, but its job function of routing data packets between computers. A cable modem which routes data between your PC and your ISP can be considered a router. In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing). In this scenario, the computer that is connected to the Internet is acting as the router for the second computer to obtain its Internet connection. Going a step up from ICS,we have a category of hardware routers that are used to perform the same basic task as ICS, albeit with more features and functions. Often called broadband or Internet connection sharing routers, these routers allow you to share one Internet connection computers. Routing is the process of selecting best paths in a network. In the past, the term routing was also used to mean forwarding network traffic among networks. However this latter function is much better described as simply forwarding. Routing is performed for many kinds of networks, including the telephone network (circuit switching), electronic data networks (such as the Internet), and transportation networks. This article is concerned primarily with routing in electronic data networks using packet switching technology. In packet switching networks, routing directs packet forwarding (the transit of logically addressed network packets from their source toward their ultimate destination) through intermediate nodes.Intermediate nodes is typically network hardware devices such as routers, bridges, gateways, firewalls, or switches. In many instances, an ISP will allow you to use a router and connect multiple computers to a single Internet connection and pay a nominal fee for each additional computer sharing the connection. This is when home users will want to look at smaller routers, often called broadband routers that enable two or more computers to share an Internet connection.

Within a business or organization, you may need to connect multiple computers to the Internet, but also want to connect multiple private networks Not all routers are created equal since their job will differ slightly from network to network. General-purpose computers can also forward packets and perform routing, though they are not specialized hardware and may suffer from limited performance. The routing process usually directs forwarding on the basis of routing tables which maintain a record of the routes to various network destinations. Thus, constructing routing tables, which are held in the router's memory, is very important for efficient routing.

Most routing algorithms use only one network path at a time. Multipath routing techniques enable the use of multiple alternative paths. In case of overlapping/equal routes, the following elements are considered in order to decide which routes get installed into the routing table (sorted by priority): Prefix-Length: where longer subnet masks are preferred (independent of whether it is within a routing protocol or over different routing protocol) Metric: where a lower metric/cost is preferred (only valid within one and the same routing protocol) Administrative distance: where a lower distance is preferred (only valid between different routing protocols)

IV. PRINCIPLES OF ROUTER DESIGN

Specified the compact contest limit and the short implementation window we adopted a set of design principles to spend the on hand time as proficiently as possible. This document provides specifications for the Router is a packet base protocol. Router drives the incoming packet which comes from the enter port to output ports based on the address contained in the packet. The router is a ” Network Router” has a one input port from which the packet enters. It has three amount produced ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame confirms sequence. Packet width is 8 bits and the length of the packet can be between 1 bytes to 33 bytes. Packet header contains three fields DA and length. Goal address (DA) of the packet is of 8 bits. The switch drives the packet to personal ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the objective address of the packet matches the port address, then switch drives the envelope to the output port, Length of the data is of 8 bits and from 0 to 33.Length is exact in terms of bytes. Data should be in terms of bytes and can take anything.

Outline check sequence contains the security check of the packet. It is calculated over the subtitle and data. The communication on network on chip is carried away from home by means of router, so meant for implement better NOC , the router should be efficiently design. This router chains three similar connections at he same time. It uses store and forward type of flow control in count to FSM Controller deterministic steering which improves the act of router.

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If the destination address of the packet matches the port address, then switch drives the packet to the output port,Length of the data is of 8 bits and from 0 to 62

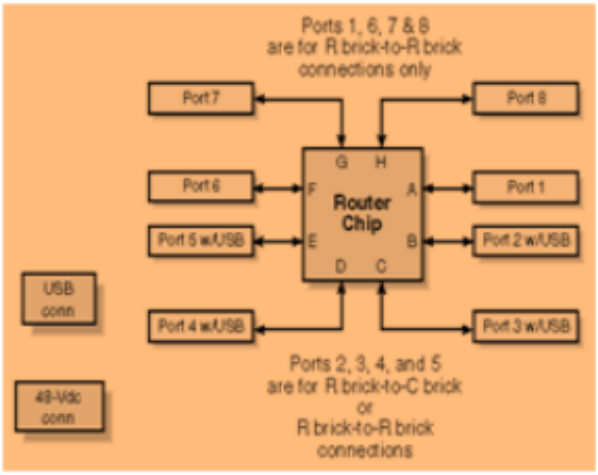

Fig 1. Three Port Router

The register has a positive edge clock, an active high clock enable and an active high asynchronous reset. The output of the register is the input of the demultiplexer. The data input to the register is transferred to the output port at the positive edge of the clock if and only if the enable is 1 and the reset is 0. If the reset is 1, then the output port of the register is set to zeros. If the enable is 0, then the output port keeps its current value. Since ROUTER is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocols do not use a clock pulse, but the data must be timed very accurately. Since ROUTER has a clock signal, the clock can vary without disrupting the data. The data rate will simply change along with the changes in the clock rate. The Three Router Design is done by using of the three blocks .the blocks are 8-Bit Register, Router controller and output block. The router controller is design by using FSM design and the output block consists of three the FSM controller gives the err and suspended_data_in signals .This functions are discussed clearly.

V. OUTPUTS

Simulation refers to the verification of a design, its function and performance. It is the process of applying stimuli to a model over time and producing corresponding responses from a model. The simulation is performed in XILINX ISE 10.1 software. A test bench is also written to test the routing pattern from various data packets. If a single slave device is used, the RE pin may be fixed to logic low if the slave permits it.Some slaves require the falling edge (high→low transition) of the slave select to initiate an action such as the mobile operators, which starts conversion on said transition. With multiple slave devices, an independent RE signal is required from the master for each slave device

Fig 2. Simulation of Router

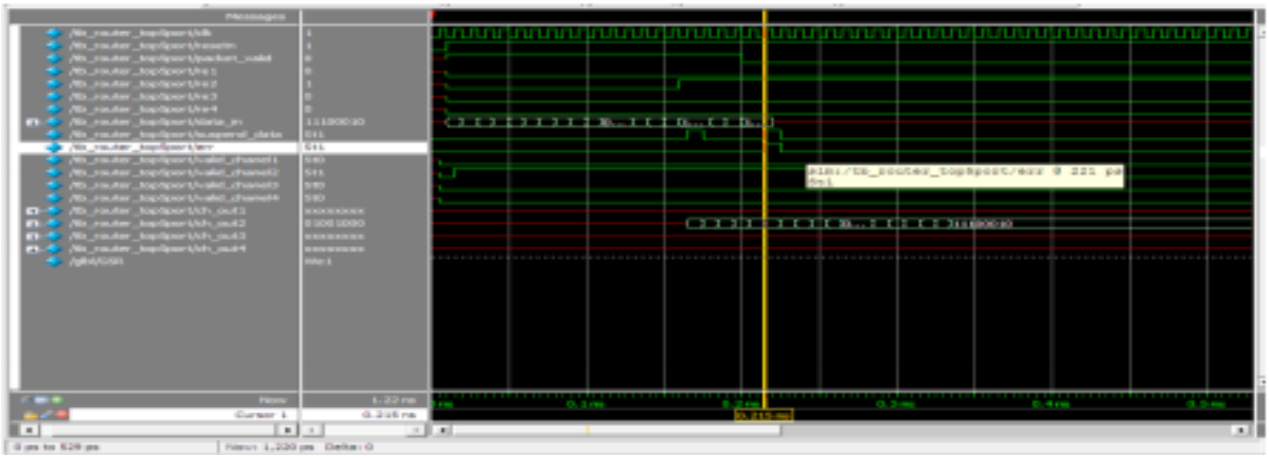

Fig 3 Simulation Results of Protocol

Data_in[1:7] = input =deferent data packets

Data_in[0] = 11111001

Output : Ch_out1 = 8'bXXXXXXXX

Ch_out2 = data_in,

Ch_out3 = 8'bXXXXXXXX.

Ch_out4 = 8'bXXXXXXXX.

After 80ns again applying inputs immediately output obtained, because of no delay elements.

Data_in[1:7] = input =deferent data packets

Data_in[0] = 11111000

Output : Ch_out1 = data_in,

Ch_out2 = 8'bXXXXXXXX,

Ch_out3 = 8'bXXXXXXXX,

Ch_out4 = 8'bXXXXXXXX.

VI. CONCLUSION

A three port router using simple decoding logic is proposed in this paper. The synthesis and simulation of the proposed router is verified through VHDL codes using XILINX ISE 10.1 software. In this ROUTER project I demonstrated the functionality of ROUTER with the most modern Design methodology i.e., Verilog and System verilog and observed the convention coverage and functional coverage of ROUTER by using cover points ,cross and different test cases(like constrained, weighted and bound for test cases).By using these test cases I improved the functional coverage of ROUTER. In this

The simulation facilitates clear indulgent of routing pattern and the functionality of a five port router for a network on chip.In future, we intend to work on improving the scheduling algorithm used in the router for better performance.

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