Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications

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Abstract

The (DSRC) dedicated short-range communication is an intelligent transportation system to push an emerging technique in our daily life. DSRC standards generally adopt FM0 and enhancing the signal reliability, Manchester codes to reach dc-balance. Nevertheless, the VLSI architecture for both coding-diversity between the Manchester codes limits the potential to design a fully reused. in this paper the FM0, to overcome this limitation (SOLS) similarity-oriented logic simplification technique is proposed. SOLS technique increases the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. this paper evaluated the performance of post layout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-µm 1P6M CMOS technology . The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 µm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

Index Terms—Dedicated short-range communication (DSRC), FM0, Manchester, VLSI.

INTRODUCTION

The dedicated short-range communication (DSRC) is a protocol for one- or two-way medium range communication especially for intelligent transportation systems. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the messagesending and broadcasting among automobiles for safety issues and public information announcement the safety issues include blind-spot, intersection warning, intercars distance, and collision-alarm. The automobile-to-roadside

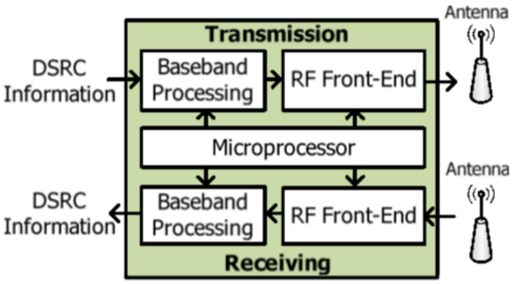


Fig. 1. System architecture of DSRC transceiver.

focuses on the intelligent transportation service, such as electronic toll collection (ETC) system. With ETC, the tollcollecting is electrically accomplished with the contactless IC-card platform. Moreover, the ETC can be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry. The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna. The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table I. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequencyof 5.8 and 5.9 GHz. The modulationmethods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zeromean for robustness issue, and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance.The purposes of FM0 and Manchester codes can provide the transmitted

signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink. The VLSI architectures of FM0 and Manchester encoders are reviewed as follows.

Review of VLSI

Architectures for FM0 Encoder and Manchester Encoder The literature proposes a VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct

Manchester encoder. It is implemented by 0.35-µm CMOS technology and its operation frequency is 1 GHz. The literature further replaces the architecture of switch in by the nMOS device. It is realized in 90-nm CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. This design is realized in 0.35-µm CMOS technology and the maximum operation frequency is 200 MHz. The literature also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator [8] . Its maximum operation frequency is about 192 MHz. Furthermore, [9] combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

B. Features of This Paper

However, the coding-diversitybetween both seriously limits the potential to design a VLSI architecture that can be fully reused with each other. This paper proposes a VLSI architecture design using similarity-oriented logic simplification (SOLS) technique. The SOLS consists of two core methods: area-compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource

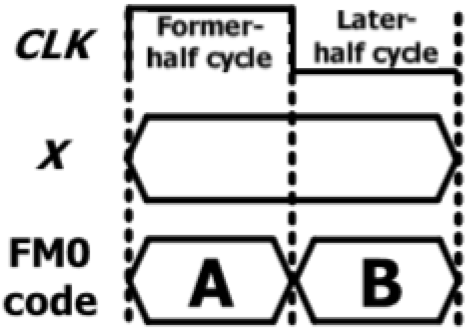


Fig. 2. Codeword structure of FM0.

to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture. With SOLS technique, this paper constructs a fully reused VLSI architecture of Manchester and

FM0 encodings for DSRC applications. The experiment results reveal that this design achieves an efficient performance compared with sophisticated works.

C. Organization

The remainder of this paper is organized as follows. Section II describes the coding principles of FM0 and Manchester codes. Section III gives a limitation analysis on hardware utilization of FM0 and Manchester encoders. This section shows the difficulty to design a fully reused VLSI architecture for FM0 and Manchester encoders

CODING PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

In the following discussion, the clock signal and the input data are abbreviated as CLK, and X, respectively. With the above parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

A. FM0 Encoding As shown in Fig. 2, for each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK, B. The coding principle of FM0 is listed as the following three rules. 1) If X is the logic-0, the FM0 code must exhibit a transition between A and B. 2) If X is the logic-1, no transition is allowed between A and B. 3) The transition is allocated among each FM0 code no matter what the X is. A FM0 coding example is shown in Fig. 3. At cycle 1, the X is logic-0; therefore, a transition occurs on its FM0 code, accordingto rule 1. For simplicity, this transition is initially set from logic-0 to -1. Accordingto rule 3, a transition is allocated

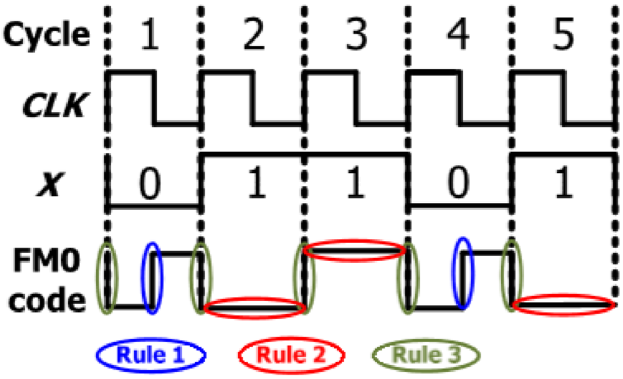


Fig. 3. Illustration of FM0 coding example.

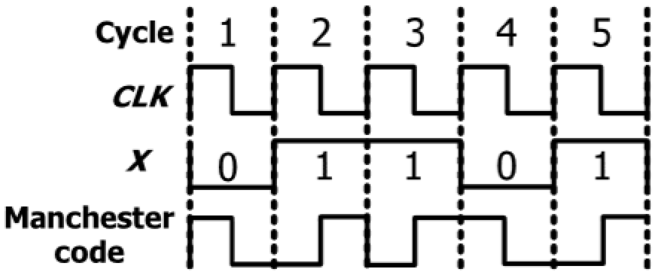


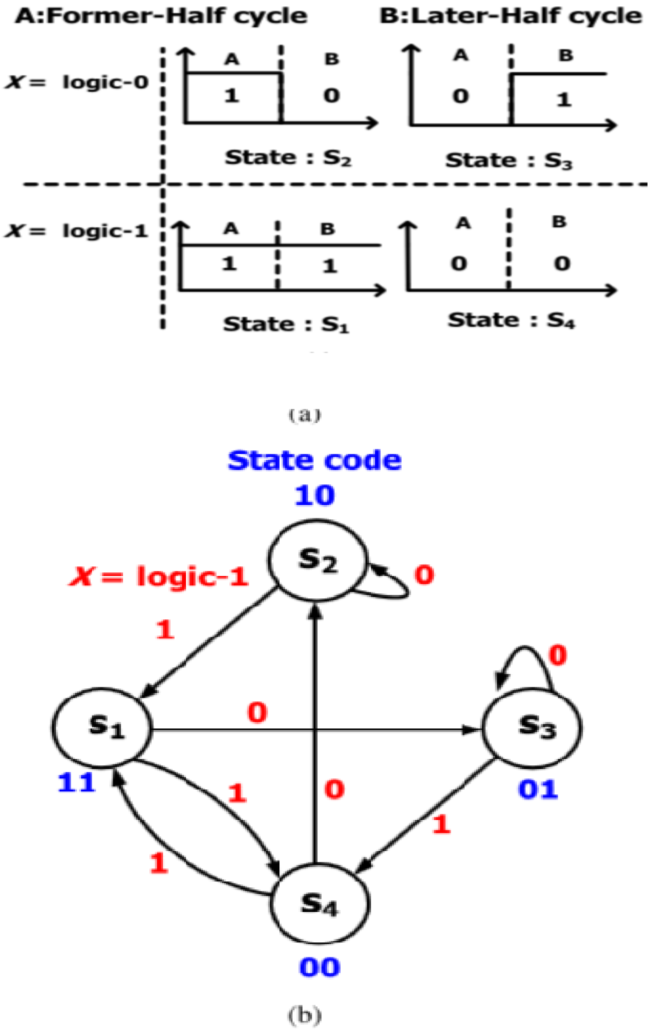
Fig. 4. Illustration of Manchester coding example.

among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

B. Manchester Encoding The Manchester coding example is shown in Fig. 4. The Manchester code is derived from X ⊕ CLK. (1) The Manchester encoding is realized with a XOR operation for CLK and X. The clock always has a transition within one cycle, and so does the Manchester code no matter what the X is.

LIMITATION ANALYSIS ON HARDWARE UTILIZATION OF FM0 ENCODER AND MANCHESTER ENCODER

To make an analysis on hardware utilization of FM0 and Manchester encoders, the hardware architectures of both are conducted first. As mentioned earlier, the hardware architecture of Manchester encoding is as simple as a XOR operation. However, the conduction of hardware architecture for FM0 is not as simple as that of Manchester. How to construct the hardware architecture of FM0 encoding should start with the FSM of FM0 first. As shown in Fig. 5(a), the FSM of FM0 code is classified into four states. A state code is individually assigned to each state, andeach state code consists of A and B, as shown in Fig. 2. According to the coding principle of FM0, the FSM of FM0 is shown in Fig. 5(b). Suppose the initial state is S1, and its state code is 11 for A and B, respectively. If the X is logic-0, the state-transition must follow both rules 1 and 3. The only one next-state that can satisfy both rules for



(a)

(b)

Fig. 5. Illustration of FSM for FM0. (a) States definition. (b) FSM of FM0. the X of logic-0 is S3. If theX is logic-1,

the state-transition must follow both rules 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also conduct the transition table of each state, as shown in Table II. A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t −1) and the B(t −1), respectively. With this transition table, the Boolean function A(t) and B(t) are given as □ $A(t)= B(t-1)$(2) $B(t)= X \oplus B(t-1)$. (3) With both A(t) and B(t), the Boolean function of FM0 code is denoted as CLK A(t)+CLK B(t). (4) With (1) and (4), the hardware architectures of FM0 and Manchester encoders are shown in Fig. 6. The top part is the hardware architecture of FM0 encoder, and the bottom part is the hardware architecture of Manchester encoder. As listed in (1), the Manchester encoder is as simple as a XOR operation for X and CLK. Nevertheless, the FM0 encoding depends not only on the X but also on the previous-state of the FM0 code. The DFFA and DFFB store the state code of the FM0 code. The MUX−1 is to switchA(t) and B(t) through the selection of CLK signal. Both A(t) and B(t) are realized by(2)and(3),respectively.Thedeterminationo fwhichcoding is adopted depends on the Mode selection of the MUX−2, where the Mode = 0 is for FM0 code, and the Mode = 1 is for Manchester code. To evaluate the hardware utilization, the hardware utilization rate (HUR) is defined as HUR= Active components Total components ×100%. (5) The component is defined as the hardware to perform a specific logic function, such as AND, OR, NOT, and flipflop. The active components mean the components that work for FM0 or Manchester encoding. The total components are the number of components in the entire hardware architecture no matter what encoding method is adopted. The HURf FM0 and Manchester encodings is listed in Table III. Forbothencodingmethods,the total componentsare 7, including MUX−2 to indicate which coding method is activated. For FM0 encoding, the active components are 6, and its HUR is 85.71%. For Manchester encoding, the active components are 2, comprising XOR−2 and MUX −2, and its HUR is as low as 28.57%. On average, this hardware architecture has a poor HUR of 57.14%, and almost half of total components are wasted. The transistor count of the hardware architecture without SOLS techniqueis 98, where86transistors are forFM0 encoding and 26 transistors are for Manchester coding. On average, only 56 transistors can be reused, and this is consistent with its HUR. The coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture.

VLSI ARCHITECTURE DESIGN OF FM0 ENCODER AND MANCHESTER ENCODER USING SOLS TECHNIQUE

The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester encodings. The SOLS technique is classified into two parts: area-compact retiming and balance logic-operation sharing. Each part is individually described as follows. Finally, the performance evaluation of the SOLS technique is given.

A. Area-Compact Retiming The FM0 logic in Fig. 6 is simply shown in Fig. 7(a). The logic for A(t) and the logic for B(t) are the Boolean functions to derive A(t) and B(t), where theX is omitted for a concise representation. For FM0, the state code of each state is stored into DFFA and DFFB. According to (2) and (3), the transition of state code only depends on B(t −1) instead of both A(t −1) and B(t −1). Thus, the FM0 encoding just requires a single 1-bit flip-flop to store the B(t−1). If the DFFA is directly removed, a nonsynchronizationbetween A(t) and B(t) causes the logicfault of FM0 code. To avoid this logic-fault, the DFFB is relocated right after the MUX−1, as shown in Fig. 7(b), where the DFFB is assumed to be positive-edge triggered. At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. In Fig. 7(a), the Q of DFFB is directly updated from the logic of B(t) with 1-cycle latency. In Fig. 7(b), when the CLK is logic-0, the B(t) is passed through MUX−1 to theD of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. As shown in Fig. 8, the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. Suppose the logic components of FM0 encoder are realized with the logic-family of static CMOS, and the total transistor count is shown in Table IV. The transistor count of the FM0 encoding architecture without area-compact retiming is 72, and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

B. Balance Logic-Operation Sharing As mentioned previously, the Manchester encoding can be derived from X ⊕ CLK, and it is also equivalent to X ⊕ CLK = X CLK + X CLK. (6) This can be realized by the multiplexer, as shown in Fig. 9(a). It is quite similar to the Boolean function of FM0 encoding in (4). By comparing with (4) and (6), the FM0 and Manchester logics have a common point of the multiplexerlike logic with the selection of CLK. As shown in Fig. 9(b), the concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t), respectively. The logic for A(t)/X is shown in Fig. 10. TheA(t) can be derived from an inverter of B(t − 1), andX is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of B(t −1) and X. The Mode indicates either FM0 or Manchester encoding is adopted. The similar concept can be also applied to the logic for B(t)/X, as shown in Fig. 11(a). Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The X can be also interpreted as the X ⊕0, and thereby the XOR operation can be shared with Manchester and FM0 encodings. As a result, the logic for B(t)/X is where the multiplexer is responsibleto switch the operandsof B(t−1) and logic-0.This architecture shares the XOR for both B(t) and X, and thereby increases the HUR. Furthermore, the multiplexer in can be functionally integrated into the relocated DFFB from area-compact technique, as shown in Fig. 11(c). The CLR is the clear signal to reset the content of DFFB to logic-0. The DFFB can be set to zero by activating CLR for Manchester encoding. When the FM0 code is adopted, the CLR is disabled, and the B(t−1) can be derived from DFFB. Hence, the multiplexer in can be totally saved, and its function can be completely integrated into the relocated DFFB. The proposed VLSI architecture of FM0/Manchester encoding using SOLS technique is The logic for A(t)/X includes the MUX−2 andan inverter.Instead, the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX−2 is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX−1, possibly causing the logic-fault on coding. To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/X is The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved.

C. Timing Analysis The logic functions of SOLS technique can be realized by various logic families. Each logic family optimizes one or more electrical performance, such as area, power, or speed, from circuit topology perspective instead of architecture perspective. The proposed SOLS technique is developed from architecture perspective to achieve 100% HUR. Among the logic families, both static CMOS circuit and transmissiongate logic are widely applied in digital circuit owing to their superior integration in process manufacturing. Hence, the timing analysis is given under these two kinds of logic families for a more general purpose. Although the SOLS technique enables the VLSI architecture to be fully shared for Manchester and FM0 encoders, their critical paths are not identical. For Manchester encoding, the delay time is given as TMan =max{TMUX,TXNOR}+TMUX +TINV (7) where TMan denotes the delay time of Manchester encoding. The TMUX, TXNOR, andTINV represent the delay time of the multiplexer, the XNOR gate, and the inverter, respectively. The DFFB is always kept at logic-0 in Manchester encoding; therefore, it is excluded from TMan. This delay path is also incorporated into that of FM0 encoding. Moreover, the FM0 encoding applies the DFFB to store the sate code, and thereby the delay time of DFFB is further considered as TFM0 = TMan +TDFF

(8) where the TFM0 is the delay time of FM0 encoding, and the TDFF stands for the delay time of DFFB. The delay time of Manchester encoding is smaller than that of FM0 encoding. Thus, the operation frequency of Manchester encoding is faster than that of the FM0 encoding in the proposed VLSI architecture.From the abovetiming analysis, the TMan notonly dominates the timing of Manchester encoding, but also affects that of FM0 encoding. Hence, the logic components inside TMan should be carefullyconsideredin their implementation.If these logic componentsare totally designed with static CMOS, the TMan is seriously limited owing to too many transistors in the critical path of Manchester encoding. More detail on this part is described as follows. For simplicity, both rise and fall times of static CMOS circuit are assumed to be identical. The fall time is adopted to denote the propagation delay with Elmore delay estimation. The static CMOS topologiesof two-input multiplexerand twoinput XNOR are respectively. The pull-down network of two-input multiplexer includes M1, M2, M3, andM4. TheM1 and M2 are in parallel, and so are M3 and M4. Indeed, this connection can improve the discharging capability. However, the transistor sizing still considers the worst case where the discharging path is constructed by only two transistors in series. The propagation delay of the static CMOS two-input multiplexer is given as TMUX−SC = TINV +CAR+CB2R (9) where the second and third terms are predicted by Elmore delay estimation. The R stands for the equivalent resistor of each transistor in pull-down network. The CA aggregates the junction capacitances of M1, M2, M3, andM4. TheCB gathers the junction capacitances of M3, M4, M5, andM6. Similarly, the propagation delay of static CMOS two-input XNOR is given as TXNOR−SC = TINV +CC R+CD2R. (10) Compared with (9), the CA is greater than CC since the CA incorporates more junction area than CC, and theCB approximates to CD. Thus, the TMUX−SC is greater than TXNOR−SC for static CMOS, the series of MUX−1 and MUX−2 dominates Manchester encoding path and leads to a total propagation delay as 2TMUX−SC =2(TINV +CAR+CB2R). (11) To further reduce the transistor count in Manchester encodingpath, the transmission-gatelogicis consideredin the circuit designs of MUX−1, MUX−2 andXNOR. The transmission gate logic of two-input multiplexer and two-input XNOR are shown in Fig. 14(a) and (b),

respectively. The propagation delay of transmission-gate two-input multiplexer is given as TMUX−TG = R□ CE (12) where the CE aggregates the junction capacitances of M1, M2, M3, andM4. TheR stands for the equivalent resistances of M1 and M2 in parallel, or M3 and M4 in parallel. Similarly, the propagation delay of transmission-gate two-input XNOR is given as TXNOR−TG =TINV + R□ CF (13) where the CF gathers the junction capacitances of M1, M2, M3, andM4. The TXNOR−TG causes slightly longer propagation delay than TMUX−TGfor transmission-gate logic, the series of XNOR and MUX−2 dominates Manchester encoding path and leads to a total propagation delay as TXNOR−TG +TMUX−TG = TINV+ R CE + R CF. (14) For a concise comparison with (11), the assumptions are given as follows. The CB, CD, CE, andCF consistently incorporate the junction capacitances of two nMOS and two pMOS. All these four capacitors can be assumed as CB = CD = CE = CF. For static CMOS circuit, both two-input multiplexer and two-input XNOR have two nMOS in series. The width of these two nMOS in series is enlarged by two times to achieve a balance fall-time, and the RN is reduced down to RN/2. A transmission gate consisting of a pMOS and an nMOS in parallel has its equivalent resistor of RP//RN. To obtain a balance signal path, RP is approximated to RN by enlarging the width of pMOS by two to three times depending on the process technology. Hence, the equivalent resistor of a transmission gate is RP//RN RN//RN = RN/2. The equivalent resistor of an nMOS in two-input multiplexer or two-input XNOR is identical to that of a transmission gate. Thus, the assumption is given as R = R = RN/2. With above assumptions, the propagation delay of transmission-gate logic is less than that of static CMOS. Applying the transmission gate logic can compact the transistor count to reduce the

D. Performance Evaluation of the SOLS Technique The evaluation of the SOLS technique is shown in Table V. With SOLS technique, the total components are reduced from seven down to five. Without SOLS technique, the FM0 and Manchester encodings are performed on individual hardware architecture with a poor HUR of 57.14%, as previously shown in Table III. With SOLS technique, the total transistor count is reduced from 98 to 44, and every transistor is fully reused in either FM0 or Manchester encoding. The SOLS technique eliminates this limitation on HUR by two core techniques: area-compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. The SOLS technique improves the HUR from 57.14% to 100%, whether the FM0 or Manchester code is adopted. Thus, the SOLS technique provides a fully reused VLSI architecture for FM0 and Manchester encodings with the HUR of 100%.

EXPERIMENT RESULTS AND DISCUSSION

A. Experiment Environment This paper is compared with the existing articles. These articles are implemented in two kinds of design-flows. The literatures [4] and [5] are realized with full-custom and the literatures are designed with FPGA. To give an objective evaluation, the proposed VLSI architecture is realized with both design-flows, as listed in Table VI. The design flow of the full-customis Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-µm 1P6M CMOS technology, and the Xilinx development board is adopted for the FPGA design-flow. The performance of full-custom design flow is from postlayout simulation, and its layout view is shown in Fig. 15. The performances of [4], [5], and [7]–[9] are listed in Table VII. Note that [6] is excluded since it further involves Miller encoding, which is out of the scope of this performance evaluation. The CMOS technologies of these works include 0.35 µm, 90 nm, which are not identical to 0.18 µm adopted in this paper. To normalize the process parameters due to different CMOS technologies, the CMOS process scaling of the constant field theorem is applied. The normalization equations are given as follows [12]: ⎧ ⎪ ⎪ ⎪ ⎪ ⎨ ⎪ ⎪ ⎪ ⎪ ⎩ f0.18 µm = f0.35 µm/90 nm ×α P0.18 µm = P0.35 µm/90 nm × 1 α A0.18 µm = A0.35 µm/90 nm× 1 α2 (15) where the f0.18µm, P0.18µm, andA0.18µm represent the normalized operation frequency, power, and area for 0.18-µm CMOS process. The α is a scaling factor defined as α = ⎧ ⎪ ⎪ ⎨ ⎪ ⎪ ⎩ 0.35 µm 0.18 µm ;from 0.35 µm to 0.18µm 90 nm 0.18 µm ;from 90 nm to 0.18µm. (16) B. Comparison With Sophisticated Articles This paper adopts the proposed SOLS technique to construct a fully reused VLSI architecture for both FM0 and Manchester

CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: areacompact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-µm1P6MCMOS technologywith anoutstandingdeviceefficiency. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 µm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

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