International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 07
March 2018

Implementation of Reversible Vedic Multipliers for High Speed applications

Thota Sri Gouri Priyanka & Y .Kanaka Raju
[1]M-Tech,Department Of Ece, Nova College Of Engineering And Technology
[2]Assistant Professor, Department Of Ece, Nova College Of Engineering And Technology

ABSTRACT :

Multiplier design is always a challenging task; how many ever novel designs are proposed, the user needs demands much more optimized ones. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation is drastically reduced by the use of Reversible logic. The reversible Urdhva Tiryakbhayam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. In this paper we aim to enhance the performance of the previous design. The Total Reversible Logic Implementation Cost (TRLIC) is used as an aid to evaluate the proposed design. This multiplier can be efficiently adopted in designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications.

Keywords— Quantum Computing, Reversible Logic Gate, Urdhva Tiryakbhayam, Optimized Design, TRLIC.

Introduction:

Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations [2]. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories [1] or Sutras

needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved. With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. Vedic mathematics can be aptly employed here to perform multiplication. Another important area which any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a tradeoff between the power dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. Thus during the design of any reversible circuit the delay is the only criteria that has to be taken care of. In [12] a reversible Urdhva Tiryakbhayam Multiplier had been proposed. This paper is an extension of the previous work which tries to optimize the circuit proposed in [12]. The paper is organized as follows: The section II gives the basics of reversible logic along with the literature review. Section III explains the Urdhva Tiryakbhayam algorithm. The section IV describes the modifications of the previous design in order to evolve the optimized design. Section V compares the proposed design with the other non Vedic multipliers as well as the previous Vedic multiplier design and draws a conclusion claiming. the versatility of Reversible Urdhva Tiryakbhayam multiplier.

Thus, integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation. The multiplier architecture is based on Urdhva Tiryagbhyam

[4] (vertical and cross - wise algorithm) sutra. An illustration of Urdhva Tiryagbhyam sutra is shown in Fig 1.

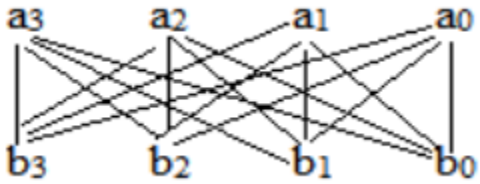


Fig 1 Illustration of Urdhva Tiryagbhyam Sutra

The 4x4 multiplication has been done in a single line in Urdhva Tiryagbhyam sutra[1] , whereas in shift and add (conventional) method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier.

ADDERS are a key building block in multipliers [5] and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect [6]. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions.

To improve the performance of the adder structures at low supply voltage levels, some methods have been proposed in [6]. In [6], an adaptive clock stretching operation has been suggested. The method is based on the observation that the critical paths in adder units are rarely activated.

Therefore, the slack time between the critical paths and the off-critical paths may be used to reduce the supply voltage. When the critical timing paths in the adder are activated, the structure uses two clock cycles to complete the operation. This way the power consumption reduces considerably at the cost of rather small throughput degradation. In [7], the efficiency of this method for reducing the power consumption of the RCA structure has been demonstrated.

II.ADDER DESIGN

The structure is based on combining the concatenation and the incrementation schemes [8] with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer . Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which

imposes a higher wiring capacitance (in the noncritical paths).

Now, we describe the internal structure of the proposed CI-CSKA shown in Fig 3 in more detail. The adder contains two *N* bits inputs, *A* and *B*, and *Q* stages [9]. Each stage consists of an RCA block with the size of *Mj (j* = 1, . . . , *Q)*. In this structure, the carry input of all the RCA blocks, except for the first block which is *Ci* , is zero (concatenation of the RCA blocks). Therefore, all the blocks execute their jobs simultaneously. In this structure, when the first block computes the summation of its corresponding input bits (i.e., *SM*1, . . . , *S*1*)*, and *C*1, the other blocks simultaneously compute the intermediate results [i.e., {*ZK j*+ *Mj* , . . . , *ZK j*+2, *ZK j*+1} for *K j* = _*j*−1 *r*=1 *Mr (j* = 2, . . , *Q)*], and also *Cj* signals. In the proposed structure, the first stage has only one block, which is RCA. The stages 2 to *Q* consist of two blocks of RCA and incrementation. The incrementation block uses the Fig 3. Internal structure of the *j* th incrementation block, *K j* = _*j*−1 *r*=1 *Mr* (*j* = 2, . . . , *Q)*. Intermediate results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage. The internal structure of the incrementation block, which contains a chain of half-adders (HAs), is shown in Fig 4. In addition, note that, to reduce the delay considerably, for computing the carry output of the stage, the carry output of the incrementation block is not used. The skip logic [9] determines the carry output of the *j* th stage (*CO, j)* based on the intermediate results of the *j* th stage and the carry output of the previous stage (*CO, j*−1) as well as the carry output of the corresponding RCA block (*Cj)*.

MULTIPLICATION 4 X 4 (UT) MULTIPLIER UNIT using Compressors

$$P_0 = X_0Y_0$$

$$C_0P_1 = X_0Y_1 + X_1Y_0$$

$$C_1P_2 = X_0Y_2 + X_2Y_0 + X_1Y_1 + C_0$$

$$C_2P_3 = X_3Y_0 + X_0Y_3 + X_1Y_2 + X_2Y_1 + C_1$$

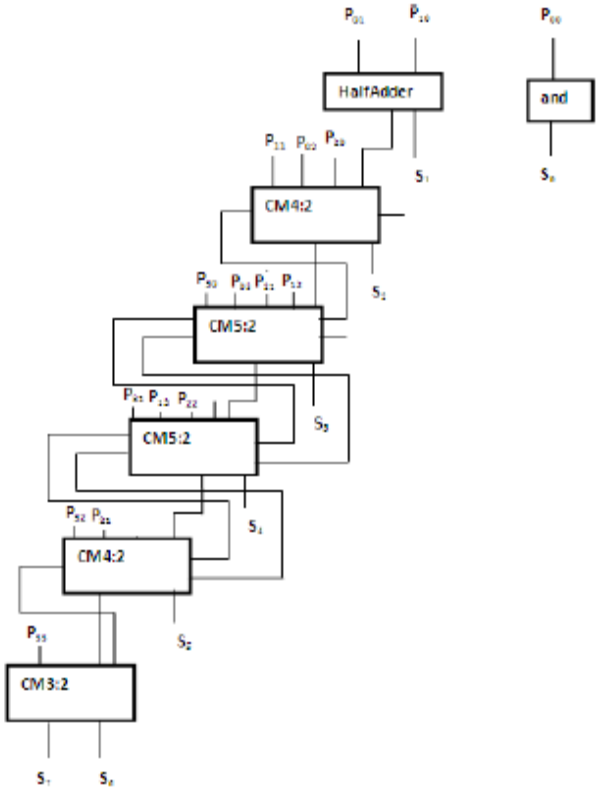
$$C_3P_4 = X_3Y_1 + X_1Y_3 + X_2Y_2 + C_2$$

$$C_4P_5 = X_3Y_2 + X_2Y_3 + C_3$$

$$V_7P_6 = X_3Y_3 + C_4$$

The 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 3.3.3. It consists of four 2X2 multipliers each of which produce four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder. The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in turn 5 bits each which need to be summed up.

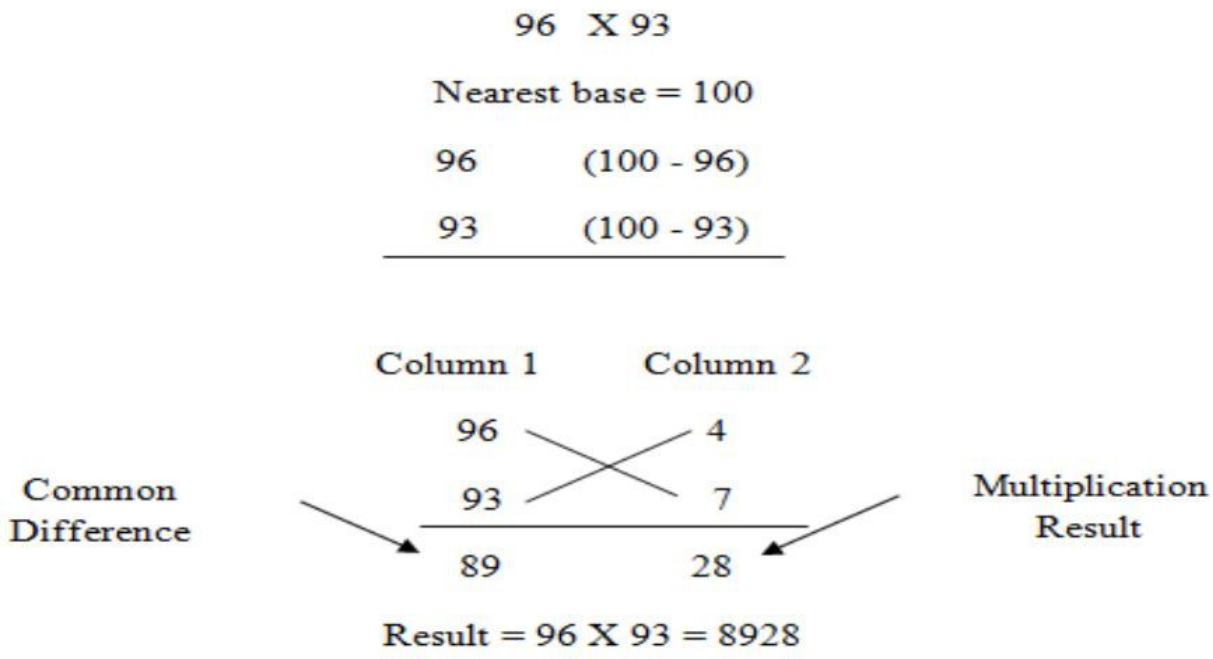
BLOCK DIAGRAM OF 4x4 UT MULTIPLIER



BLOCK DIAGRAM OF 4x4 UT MULTIPLIER

Nikhilam Sutra

Nikhilam Sutra literally means "all from 9 and last from 10". Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large. Since it finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, larger is the original number, lesser the complexity of the multiplication. We first illustrate this Sutra by considering the multiplication of two decimal numbers (96 * 93) where the chosen base is 100 which is nearest to and greater than both these two numbers.



Multiplication Using Nikhilam Sutra

The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (7*4 = 28). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of 12 Column 1 or vice versa, i.e., 96 – 7 = 89 or 93 - 4 = 89. The final result is obtained by concatenating RHS and LHS (Answer = 8928)

APPLICATIONS

- ☐ This multiplier may find applications in Fast Fourier Transforms (FFTs).
- ☐ Applications of DSP like imaging, software defined radios,wireless communications.
- ☐ To provide universal multiplication with low power high speed.
- ☐ Applications in system on chip design as technology scales.
- ☐ In public key cryptography like RSA encryption and decryption.
- ☐ Nanocomputing
- ☐ Bio Molecular Computations
- ☐ Laptop/Handheld/Wearable Computers
- ☐ Spacecraft
- ☐ Implanted Medical Devices
- ☐ Wallet “smart cards”
- ☐ “ Smart tags” on inventory

ADVANTAGES:

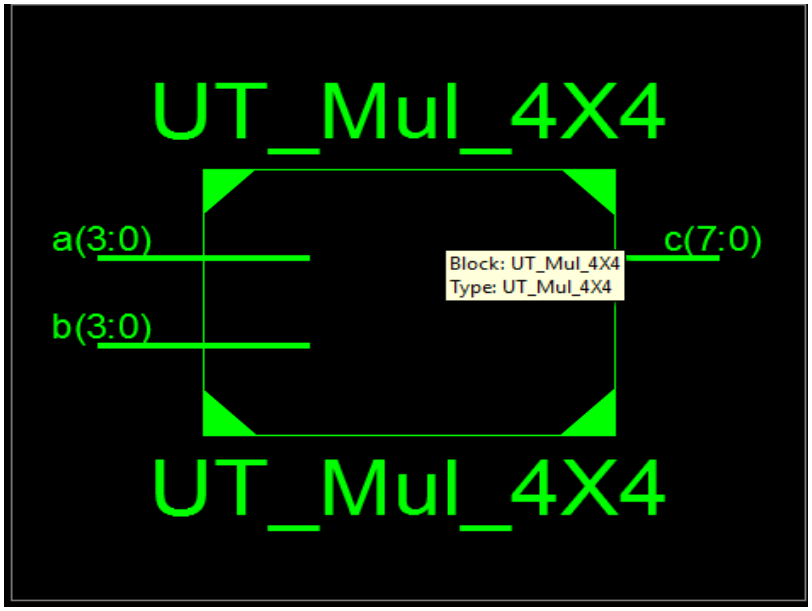
Vedic multiplier is faster than array multiplier and Booth multiplier. As the number of bits increases from 8x8 bits to 16x16 bits, the timing delay is greatly reduced for

Vedic multiplier as compared to other multipliers. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures. Delay in Vedic multiplier for 16 x 16 bit number is 32 ns while the delay in Booth and Array multiplier are 37 ns and 43 ns respectively [12]. Thus this multiplier shows the highest speed among conventional multipliers. It has thisadvantage than others to prefer a best multiplier

Architecture of Vedic multiplier based on speednspecification is designed here for following criteria

- Increase the Speed of the system
- To acquire good efficiency of the system
- Reduce the time delay as well as path delay in the multiplier
- The combinational path delay of Vedic multipliern obtained after compared with normal multipliers and found that the proposed Vedic multiplier.

RTL SCHEMATIC DIGRAM:



4x4 vedic multiplier PIN diagram

Conclusion:

In This Paper Presents The Urdhva Tiryakbhayam Vedic Multiplier Realized Using Compressors And New Architecture Compressors Are Presented. These Compressors Performance Is Evaluated On Vedic Multiplier In Terms Of Speed Or Delay. Vedic Multiplier Speeds Operation And Using Modified Compressors Reduces Power And Delay.

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