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Proposal of a Novel Test Application Strategy for Optimum Power Utilization and Achieving Minimum Number of Transitions

Prof.Dr.G.Manoj Someswar[1], Babu Rajesh[2]

1. Research Supervisor, Dr.APJ Abdul Kalam Technical University, Lucknow, U.P., India

2. Research Scholar, Dr.APJ Abdul Kalam Technical University, Lucknow, U.P., India

Abstract

Testing low power very large scale integrated (VLSI) circuits in the recent times has become a critical problem area due to yield and reliability problems. This research work lays emphasis on reducing power dissipation during test application at logic level and register-transfer level (RTL) of abstraction of the VLSI design flow. In the initial stage, this research work addresses power reduction techniques in scan sequential circuits at the logic level of abstraction.

Implementation of a new best primary input change (BPIC) technique based on a novel test application strategy has been proposed. The technique increases the correlation between successive states during shifting in test vectors and shifting out test responses by changing the primary inputs such that the smallest number of transitions is achieved. The new technique is test set dependent and it is applicable to small to medium sized full and partial scan sequential circuits. Since the proposed test application strategy depends only on controlling primary input change time, power is reduced with no penalty in test area, performance, test efficiency, test application time or volume of test data. Furthermore, it is indicated that partial scan does not provide only the commonly known benefits such as less test area overhead and test application time, but also less power dissipation during test application when compared to full scan. With a view to promote for power savings in large scan sequential circuits, a new test set independent multiple scan chain-based technique which employs a new design for test (DFT) architecture and a novel test application strategy has been indicated in this research work. The technique has been validated using benchmark examples and it has been shown that power is reduced with low computational time, low overhead in test area and volume of test data and with no penalty in test application time, test efficiency, or performance. The second part of this dissertation addresses power reduction techniques for testing low power VLSI circuits using built-in self-test (BIST) at RTL. First, it is important to overcome the shortcomings

associated with traditional BIST methodologies. It is shown how a new BIST methodology for RTL data paths using a novel concept called test compatibility classes (TCC) overcomes high test application time, BIST area overhead, performance degradation, volume of test data, fault-escape probability, and complexity of the testable design space exploration. Secondly, power reduction in BIST RTL data paths is achieved by analyzing the effect of test synthesis and test scheduling on power dissipation during test application and by employing new power conscious test synthesis and test scheduling algorithms. Thirdly, the innovative BIST methodology has been validated using benchmark examples. Also, the research work states that when the power conscious test synthesis along with the test scheduling is combined with novel test compatibility classes and in this proposed research work, simultaneous reduction in test application time and power dissipation is achieved with low overhead in computational time.

Keywords*: *Testing low power very large scale integrated (VLSI), Register-transfer level (RTL), Test compatibility classes (TCC), Built-in self-test (BIST), Best primary input change (BPIC) Linear feedback shift register (LFSR)

cuits with no penalty in area overhead, test application time, test efficiency, performance, or volume of test data. However, the computation of the best primary input change (BPIC) time introduced research paper is dependent on the size and the value of the test vectors in the test set. Therefore, integrating the proposed best primary input change time with scan cell and test vector ordering leads to discrete, degenerate and highly irregular design space, and hence high computational time, which limits the applicability of the new BPIC test application strategy only to small to medium sized scan sequential circuits?[1] This chapter introduces a new test set independent technique based on multiple scan chains and shows how with low overhead in test area and volume of test data, and with no penalty in test application time, test efficiency, or performance, considerable savings in power dissipation during test application in large scan sequential circuits can be achieved in low computational time. Further, the extra test hardware required by the proposed technique employing multiple scan chains can be specified at the logic level and synthesised with the rest of the circuit. This makes the proposed multiple scan chains-based power minimisation technique easily embeddable in the existing VLSI design flow as described previously in Figure 1.

The rest of the chapter is organised as follows. Outlines the shortcomings of the previously proposed approaches for power minimisation in large scan sequential circuits and gives the motivation and the objectives of the proposed technique. In a brief review of standard test terminology and power dissipation concepts used throughout the chapter are presented. Section introduces a new technique for power minimisation in large scan sequential circuits based on multiple scan chains including the proposed DFT architecture, scan cell classification, clock tree power minimisation and extension to scan BIST methodology. Partitioning scan

cells in multiple scan chains based on their classification, and a new test application strategy based on the DFT architecture described in the previous section are introduced in research paper. Experimental results and a comparative study of the proposed BPIC and the multiple scan chain-based technique are presented.

Motivation and Objectives

The aim of this chapter is to reduce power dissipation in large scan sequential circuits. Despite their benefits in lowering power dissipation during test application, the previously described techniques, and the new BPIC test application strategy, also described in, are inefficient for large scan sequential circuits due to one or more of the following problems:

a. test area overhead associated with detection logic required to find non-essential vectors (i.e. vectors which do not contribute to an increase in fault cover-age).

b. performance degradation associated with modified scan cell design.

c. large test application time required to achieve significant power savings.

d. clock tree power dissipation is tackled by clock gating only for nonessential test vectors.

e. high number of extra test vectors emerges as a problem to testers which need to change to support the large volume of test data.

f. computational time may be prohibitively large hindering the exploration for large sequential circuits.

The aim of this chapter is to introduce a new technique for power minimisation during test application in large scan sequential circuits based on a novel DFT architecture which eliminates all the above mentioned problems (a) - (f). The proposed DFT architecture is based on partitioning scan cells into multiple scan chains which reduces the clock tree power dissipation and does not have performance penalty. A new test application strategy for the proposed DFT architecture which applies a single extra test vector while shifting out test responses for each scan chain is presented. The multiple scan chain-based approach for power minimisation which is test set independent, is applicable to both non-compact and compact test sets leading to low test application time. It is shown that with low overhead in test area and volume of test data, and with no penalty in test application time, test efficiency, or performance, high savings in power dissipation during test application in large scan sequential circuits are achieved in low computational time.

Background and Definitions

A brief review of standard test terminology used throughout this chapter is presented. The *controlling* value for a gate is a single input value that uniquely determines the output to a known value independent of the other inputs to the gate. For example, the controlling value for OR gate is 1, and for AND gate is 0. If the value of an input is the complement of the controlling value, then the input has a *non controlling* value. A path is a

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set of connected gates and wires. A path is defined by a single input wire and a single output wire per gate. A signal is an *on-input* if it is on the target path. A signal is an *off-input* (*side input*) if it is an input to a gate which is on a target path but is not an on-input. If two faults can be detected by a single test vector,

they are *compatible faults*. Consequently, two faults are *incompatible*, if they cannot be detected by a single test vector. A test vector from a given test set is an *essential* test vector, if it detects at least one fault that is not detected by any other test vector in this test set. A test vector is *non-essential* with respect to a given test set if all the faults detected by it are also detected by other test vectors in the given test set. A test set independent approach for power minimisation depends only on circuit structure and savings are guaranteed regardless of the size and the value of the test vectors in the test set. This is unlike the test set dependent approaches, where power minimisation depends on the size and the value of the test vectors in the test set, as introduced.[3]

Power Minimisation in Scan Sequential Circuits Based on Multiple Scan Chains

In this section a new technique for power minimisation in large scan sequential circuits based on multiple scan chains is introduced. Overviews the proposed DFT architecture for power minimisation. It defines compatible, incompatible, and independent scan cells and their importance for partitioning scan cells into multiple scan chains. It gives an important theoretical result showing the advantage of the proposed DFT architecture from the clock tree power dissipation standpoint, and describes how the proposed multiple scan chains can be extended to scan BIST methodology.[4]

Proposed Design for Testability Architecture Using Multiple Scan Chains

The proposed DFT architecture using multiple scan chains SC_0: : :$SC_{k\ 1}$is illustrated in Figure 4.1. The scan input *Scan In* is routed to all scan chains while the scan output *Scan Out* is selected from the output of each scan chain. Scan chains SC_0: : :$SC_{k\ 1}$are operated using non-overlapping enable signals for clocks CLK_0: : :$CLK_{k\ 1}$. Non-overlapping enable signals gate the system clock *CLK* using a scan control register where the number of cells equals the number of scan chains. This implies that scan chains SC_0: : :$SC_{k\ 1}$are enabled one by one during each scan cycle. While shifting out test responses through scan chain SC_i, only the bit position *i* of scan control register is set to 1 while the other positions are set 0. This is easily implemented by shifting the value of 1 through scan control register using the extra scan clock *SCLK*. Before starting the first scan cycle, the initial vector 10: : :00 is set up in the scan control register using the scan input *Scan In*. Thereafter, for each scan cycle, the 10: : :00 value is propagated circularly through the scan control register. It should be noted that when the circuit under test is in the test mode all the faults in the

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extra logic are observable through *Scan Out* line using the test data which is shifted through the k scan chains and control data shifted through the scan control register. Therefore, the extra test hardware, including the selection logic shown in Figure 1, has no penalty on test efficiency. During the normal operation of the circuit CLK_0: : :$CLK_{k\ 1}$are active at the same time, since when normal/test signal $N=T$ is 1 the outputs of the extra OR gates are 1 and CLK is not gated by the scan control register.

To provide a brief overview of the test application strategy for the proposed DFT architecture, while shifting out test responses present in scan cells within scan chain SC_i, primary inputs are set to extra test vector EV_i which eliminates the spurious transitions that originate from scan cells within scan chain SC_i. The number of clock cycles required to shift in the present state (pseudo input) part of each test vector equals the number of scan cells and the test response is loaded in a single clock cycle. This implies that there are no extra clock cycles for each test vector applied to the circuit under test and hence no penalty on test application time. Note that the proposed DFT architecture has no penalty on performance, since extra test hardware is not inserted on critical paths. Further, the extra test hardware required by the scan control register and selection logic can be specified at the logic level and synthesised with the rest of the circuit which makes the proposed DFT architecture easily embeddable in the existing VLSI design flow. It should be noted that the proposed DFT[5] architecture introduced for full scan sequential circuits is equally applicable to partial scan sequential circuits. Since the number of scan cells in a partial scan sequential circuit is approximately 10% of the total number of state elements it is more appropriate to illustrate the applicability of the proposed architecture on large full scan sequential circuits. However, as the complexity of state of the art digital circuits increases it is expected that in the foreseeable future partial scan sequential circuits with very high number of scan cells will appear. In such cases, the technique proposed in this chapter *is applicable with no modifications to partial scan sequential circuits*. What makes the proposed multiple scan chain-based DFT architecture particularly suitable for large scan sequential circuits is that partitioning scan cells into multiple scan chains is test set independent, and it depends only on the circuit size and structure unlike the solutions described in the previous Chapter 3 which strongly rely on the size of the test set and hence are applicable only to small to medium sized scan sequential circuits.

The algorithm for partitioning scan cells into multiple scan chains and the new test application strategy using multiple scan chains and extra test vectors shown in Figure 1, are described later. Before describing generation of multiple scan chains, scan cells need to be classified into three broad classes as described in the following.

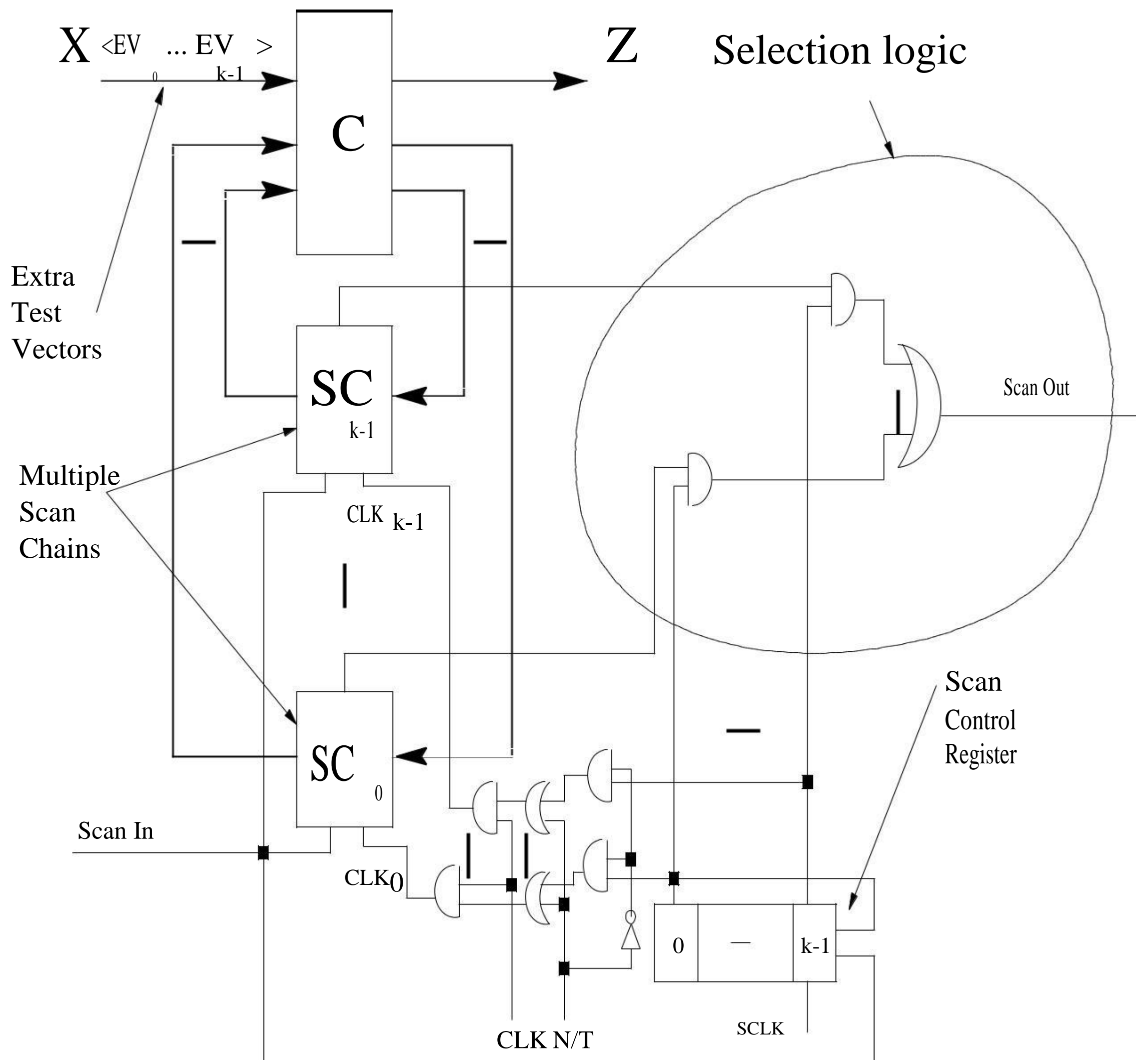

Figure 1: Proposed DFT architecture based on multiple scan chains.

Compatible, Incompatible, and Independent Scan Cells

In order to partition scan cells into multiple scan chains, they need first to be classified into three broad classes: compatible, incompatible, and independent scan cells. It should be noted that scan cell classification is not done explicitly by enumeration or exhaustive search, but it is done implicitly by the multiple scan chains partitioning algorithm as explained later in Figure9. The proposed classification is important for computing extra test vectors associated with each scan chain that eliminate spurious transitions which were defined. For the sake of completeness, Definition 1

Definition 1 A spurious transition during test application in scan sequential circuits is a transition which occurs in the combinational part of the circuit under test while shifting out the test response and shifting in the present state part of the next test vector.[6] These transitions do not have any influence on test efficiency since the values at the input and output of the combinational part are not useful test data. Now the compatible and incompatible scan cells are introduced.

Definition 2 Two scan cells S_i and S_j are *compatible* if all primary inputs x_k are as-signed values c_k that eliminate the spurious transitions which originate from both S_i and S_j . The values c_k of primary inputs x_k constitute the *extra test vector* which eliminates spurious transitions originating from both S_i and S_j.[7]

Note that the sole purpose of extra test vectors is to reduce the spurious transitions during test application and has no effect on fault coverage which is determined by the original test set. The application of extra test vectors defines a novel test application strategy for power minimisation which is detailed. Further, since a single extra test vector is used for each scan chain regardless of values loaded in scan cells then the volume of extra test data is dependent only on the number of scan chains and not on the number of scan cells and/or the size of the original test set.

Definition 3 Two scan cells S_i and S_j are *incompatible* if at least one primary input x_k that is assigned value i_k to eliminate the spurious transitions which originate from S_i will propagate the transitions which originate from S_j . Two incompatible scan cells cannot be assigned to the same scan chain since there is no extra test vector that can eliminate spurious transitions which originate from both of them.

The following example illustrates compatible and incompatible scan cells.

Example 1 Consider the circuit shown in Figure 2. The fx_0;x_1;x_2g are primary in-puts, fS_0;S_1;S_2;S_3;S_4;S_5g are scan cells, fy_0;y_1;y_2;y_3;y_4;y_5g are present state lines, and fz_0;z_1;z_2;z_3;z_4;z_5g are circuit outputs. To eliminate spurious transitions at gate z_0 while shifting out test responses through scan cell S_0, primary input x_0 must be assigned the con-trolling value 0 of gate z_0. Similarly, to eliminate spurious transitions that originate from scan cell S_1, primary input x_0 must be assigned the controlling value 1 of gate z_1. Different values must be assigned to x_0 to eliminate spurious transitions which originate from scan cells S_0 and S_1. Therefore scan cells S_0 and S_1 are incompatible and are assigned to different scan chains SC_0 = fS_0g and SC_1 = fS_1g. On the other hand, by assigning x_1 to the controlling value 0 of gates z_2 and z_3 the spurious transitions which originate from both scan cells S_2 and S_3 are eliminated. Thus, by introducing S_2 and S_3 into SC_0 and applying for example extra test vector $x_0x_1x_2$ = f000g while shifting out test responses from SC_0 = fS_0;S_2;S_3g no spurious transitions will occur at gates z_0, z_2 and z_3. Similarly, scan cells S_4 and S_5 are compatible since assigning 1 to the primary input x_2 eliminates spurious transitions at gates z_4 and z_5. By introducing S_4 and S_5 into SC_1 and applying extra test vector $x_0x_1x_2$ = f111g while shifting out test responses from SC_1 = fS_1;S_4;S_5g no spurious transitions will occur at gates z_1, z_4

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and z_5. It should be noted that there is a strict interrelation between extra test vector value $x_0x_1x_2$ = f000g and scan chain SC_0 = fS_0;S_2;S_3g, and $x_0x_1x_2$ = f111g and scan chain SC_1 = fS_1;S_4;S_5g. While for the sake of simplicity, the

extra test vectors $x_0x_1x_2$ = f000g and $x_0x_1x_2$ = f111g were de-scribed explicitly in this particular example, the extra test vectors and hence the multiple scan chains, are derived implicitly by the partitioning algorithm as explained later in Figure 9. Finally, note that output signals z_3 of scan chain SC_0 and z_5 of SC_1 are fed into the selection logic of the proposed DFT architecture from Figure.1. The previous example has assumed a simple circuit where *all* the spurious transitions are eliminated by partitioning scan cells in two scan chains SC_0 and SC_1. However, some of the spurious transitions cannot be eliminated as described in the following example.[7]

Example 2 Consider the circuit shown in Figure 3. The spurious transitions which originate in scan cells S_0 and S_1 cannot be eliminated at gate t_0 since both inputs are present state lines. However, by assigning x_0 and/or x_1 to the controlling value 0 of gate t_1 the spurious transitions will be eliminated at gate t_1. Scan cells S_0 and S_1 are compatible since same primary input values eliminate the spurious transitions of gate t_1.

Example 3 has illustrated that some of the spurious transitions cannot be eliminated since all the gate inputs depend on present state lines. Computing primary input values that eliminate spurious transitions (extra test vectors introduced in Definition 2) can be viewed as an ATPG problem to a *reduced circuit* with a *specified fault list* which are detailed in the algorithms presented. The following Example 3 briefly illustrates the generation of the *reduced circuit* required to compute extra test vectors.

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ScanIn

S 0 y 0 Z 0

X 0

y 1

S 1 z 1

S 2 y 2 z 2

x 1

y 3 z 3

S 3

ScanOut

Selection Logic

S 4 y 4 z 4

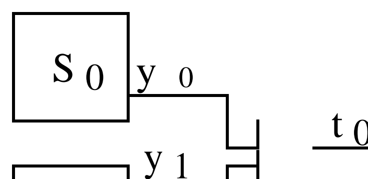
x 2

Z 5

y 5

S 5

Figure 2: Example 1 circuit illustrating compatible and incompatible scan cells



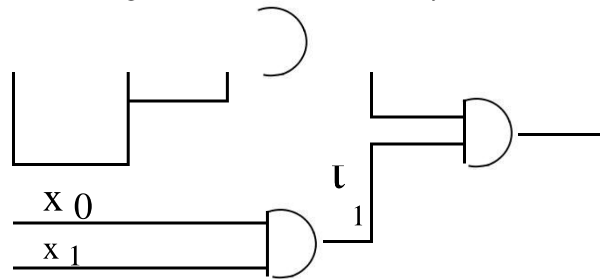


Figure 3: Example 2 circuit illustrating spurious transitions which cannot be eliminated on t_0.

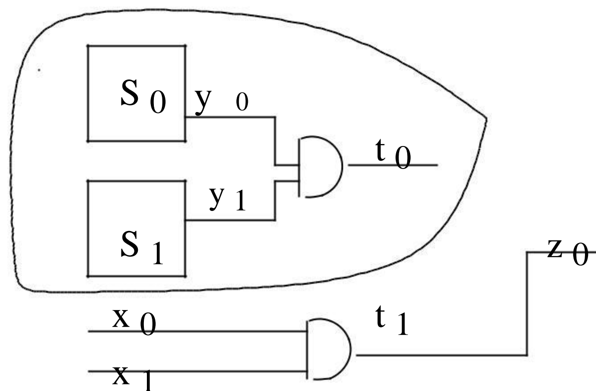


Figure 4: Reduced circuit of the example circuit from Figure 3 illustrating the steps required to compute extra test vectors

Example 4 For the circuit shown in Figure 3 the reduced circuit is generated as follows using the part (a) of the algorithm shown in Figure 9. Initially the signal t_1 at the input of gate z_0 is identified to eliminate spurious transitions that originate from scan cells S_0 and S_1. Then scan cells S_0 and S_1, and the AND gate t_0 are excluded from the reduced circuit as shown in Figure 4. Furthermore, gate z_0 is modified to a buffer (signals t_1 and z_0 are identical). The targeted fault in the reduced circuit is t_1 stuck-at 1 (*sa* 1) which eliminates the spurious transitions at gate z_0 in the original circuit. Finally, the extra test vectors (Definition 2) that eliminate the spurious transitions during test application are computed x_0x_1 = f0X ;X 0g.

A particular case of scan cells are self-incompatible scan cells which are defined as follows.

Definition 4 A scan cell S_i is *self-incompatible* if at least one primary input x_k that is assigned value i_k to eliminate the spurious transitions which originate from S_i on one fan out path will propagate the transitions which originate from S_j on a different fan out path. Now a new question which arises is whether the spurious transitions which originate from self-incompatible scan cells can be eliminated? In order to provide an answer consider the following example.

Example 5 Consider the circuit of Figure 5 where fx_0;x_1g are primary inputs, S_0 is scan cell, y_0 is present state line, and ft_0;t_1;t_2g are circuit lines. To eliminate spurious transitions at gate t_0

while shifting out test responses through scan cell S_0, primary input x_0 must be assigned the controlling value 1 of gate t_0. However, to eliminate spurious at gate t_1, primary input x_0 must be assigned the controlling value 0 of gate t_1. Different values must be assigned to x_0 to eliminate spurious transitions which originate from the same scan cell S_0 and hence scan cell S_0 is self-incompatible. However if primary input x_1 is assigned the controlling value 0 of gate t_2 the spurious transitions which originate in S_0 and propagate on path fS_0;t_1;t_2g will be eliminated.[9] Therefore by assigning extra test vector x_0x_1 = f10g, the spurious transitions propagating on both paths fS_0;t_0g and fS_0;t_1;t_2g will be eliminated. This leads to the conclusion that most of the spurious transitions originating in self-incompatible scan cells can be eliminated by examining the fan out paths of self-incompatible scan cells and assigning a single extra test vector while shifting out the test responses. However, the single extra test vector is at the expense of a small number of spurious transitions that cannot be eliminated as in the case of transitions on line t_1 in the simple circuit of Figure5.

The previous example has shown that following a careful examination of fan out branches of self-incompatible scan cells, most of the spurious transitions originating in self- incompatible scan cells can be eliminated using a single value for the extra test vector. Finally, independent scan cells are introduced.[8]

Definition 5 A scan cells S_i is *independent* if all the gates on all the paths which originate from S_i do not have at least one side input which can be justified by primary inputs.

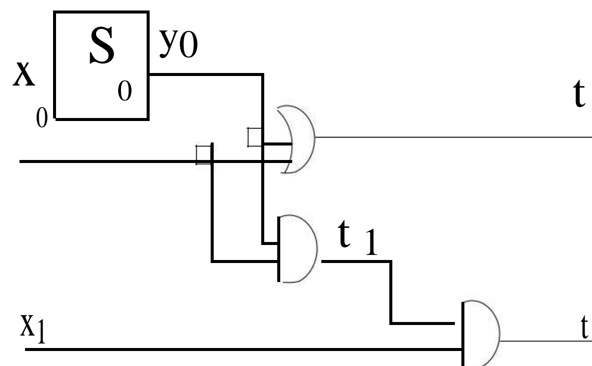


Figure 5: Example 4 circuit illustrating self-incompatible scan cells

The independent scan cells are grouped in the extra scan chain (ESC) for which no extra test vector can be computed and hence the spurious transitions cannot eliminated. The following example illustrates independent scan cells.

Example 5 Consider the circuit shown in Figure 6. Output z_0 depends only on scan cells S_0 and S_1, and the next state $y^0_4$of scan cell S_4 depends only on scan cells S_0, S_1, S_2 and S_3. There are no side inputs of

gates t_0 and t_1 that can be justified by primary inputs such that spurious transitions originated from S_0, S_1, S_2 and S_3 are eliminated. Therefore scan cells S_0, S_1, S_2 and S_3 are independent.

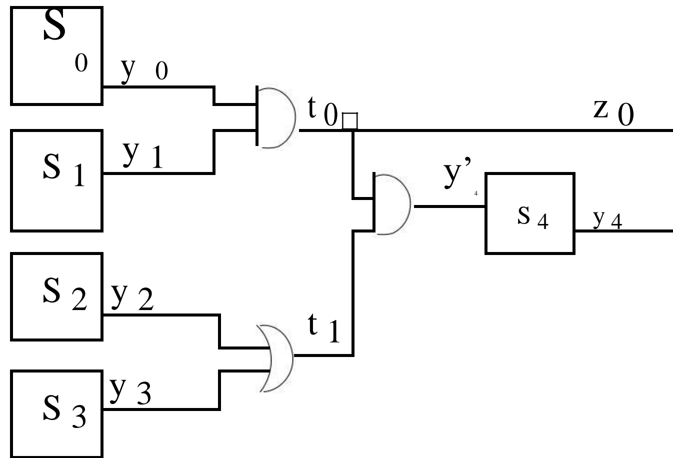


Figure 6: Example 5 circuit illustrating independent scan cells.

Power Dissipated by the Buffered Clock Tree

Previous research has established that power dissipated in the clock tree is typically one third of the total power dissipation and hence it is necessary to minimise power dissipated in the clock tree not only during functional operation but also during test application. Unlike previous approaches which do not consider power dissipated by the buffered clock tree or gate the clock tree *only* for non-essential test vectors from a large test set, the proposed DFT architecture using multiple scan chains (Figure 1) reduces clock tree power for *all* the test vectors of a very small test set where each test vector is essential (i.e. detects at least one fault). This is explained by the following theorem which gives an upper bound on power reduction.[10]

Theorem 1 Consider k scan chains in the DFT architecture of Figure 1 then the power reduction of the buffered clock tree over the standard full scan architecture is upper bounded by $(k-1)/k$.

Proof: Let $\{m_0, \ldots, m_{k-1}\}$ be the size of each scan chain and $\sum_{i=0}^{k-1} m_i = m$, where m is the total number of scan cells. Since for large dies the clock power dissipation changes from square-root dependence on the number of scan cells to a linear dependence power dissipated by each scan chain SC_i can be approximated to $\lambda \; m_i$ where λ is dependent on clock frequency, supply voltage and wire lengths. The power dissipated while shifting test responses over an entire scan cycle (m clock cycles) for the proposed architecture

is $P_{MSC} = \lambda \sum_{i=0}^{k-1} m_i^2$ since over m_i clock cycles only the buffered clock tree feeding SC_i is active. On the other hand power dissipated in the traditional full scan architecture is

$$P_{FULL} = \lambda \; m^2 = \lambda \left(\sum_{i=0}^{k-1} m_i\right) \left(\sum_{i=0}^{k-1} m_i\right).$$ Therefore the reduction in power dissipation is

i=0 i=0

$$Red = (P_{FULL} \quad P_{MSC}) = P_{FULL} = 1 \quad (\lambda \sum_{i=0}^{k-1} m_i^2) = (\lambda \quad (\sum_{i=0}^{k-1} m_i) \quad (\sum_{i=0}^{k-1} m_i)).$$

Following Cauchy-Schwarz inequality where

$$(\sum_{i=0}^{k-1} m_i) \quad (\sum_{i=0}^{k-1} m_i) \quad kfi \quad (\sum_{i=0}^{k-1} m_i^2)$$

the power reduction is upper bounded by $Red ffi$ 1 1=k = (k

1)=k

The previous theorem shows that power reduction of up to $(k\ 1)=k$ can be achieved in the buffered clock tree, with maximum reduction achieved when scan chains have an equal number of scan cells. It should be noted that by gating the clock of each scan chain not only average power reduction is achieved but also savings in peak power are guaranteed since while shifting out test responses only a single buffered clock tree is active.

Extension of the Proposed DFT Architecture Based on Multiple Scan Chains to Scan BIST Methodology

So far the proposed DFT architecture based on multiple scan chains introduced. It was applied to full scan sequential circuits using external automatic test equipment ATE (Figure1). This can be summarised in Figure 7 where the extra test vectors for scan chains SC_0 and $SC_{k\ 1}$ are highlighted. Further, it is shown that the test response $Y_{m\ 1}^{i}$, which is the test response in the first scan cell from scan chain $SC_{k\ 1}$, has yet to be shifted after the test responses from scan chains SC_0; : : : ;$SC_{k\ 2}$ were already shifted out.

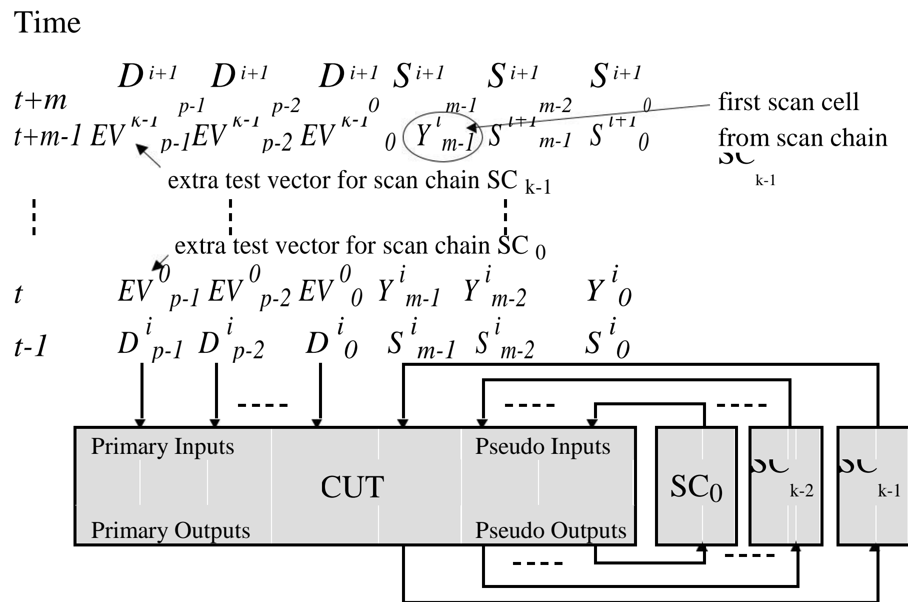


Figure 7: Summary of the proposed DFT architecture based on multiple scan chains when employing standard scan DFT using external ATE

However, the proposed DFT architecture based on multiple scan chains is not applicable only to standard scan sequential circuits using external ATE [11]. In the following the minor modifications which need to be considered when using scan BIST methodology (Figure 1 is given. Figure 8 shows that the serial output of the linear feedback shift register (LFSR) is fed directly into the scan chain which makes the primary inputs directly controllable while shifting out test responses from each scan chain. Therefore, extra test vectors associated with each scan chain can be applied to primary inputs while shifting in the present state part of the next test vector associated with each scan chain. Scan cells are partitioned into multiple scan chains and extra test vectors are calculated in the same way as for scan sequential circuits as described in the following. This will lead to a lower area overhead associated with scan BIST methodology (Figure 5) at the expense of higher interference from ATE which needs to store the primary input part of each test vector and the extra test vector associated with each scan chain.

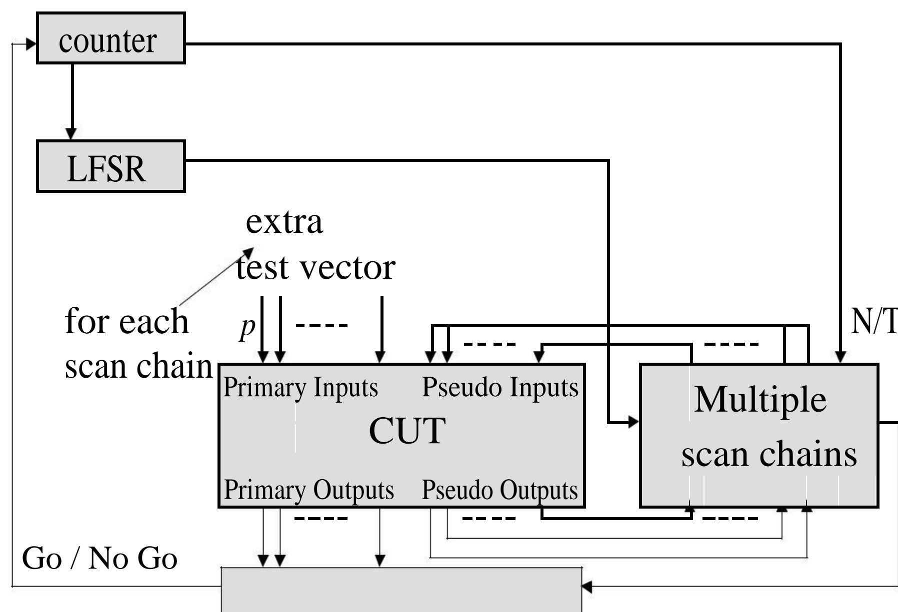


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Figure 8: Extension of the proposed DFT architecture based on multiple scan chains to scan BIST methodology

Multiple Scan Chains Generation and New Test Application Strategy

Having described the new DFT architecture based on multiple scan chains and scan cell classification from power dissipation standpoint, now algorithms for multiple scan chain generation are introduced. In partitioning scan cells into multiple scan chains based on their classification is given. Then, in new test application strategy based on the DFT architecture described, is introduced.[12]

Partitioning Scan Cells into Multiple Scan Chains

Multiple Scan Chain Partitioning (*MSC-PARTITIONING*) algorithms identifies compatible scan cells introduced by Definition 2, groups them in scan chains and computes an extra test vector for each scan chain. Figure9 gives the flow of the pro-posed *MSC-PARTITIONING* algorithm which is divided in five parts identified in boxes marked from (a) to (e). In order to facilitate the elimination of spurious transitions by computing an extra test vector for each scan chain the initial circuit **C** needs to be trans-formed to a reduced circuit **C'** (box (a)). A by-product of the reduction procedure is a specified fault list **L** (box (b)) which is targeted by an ATPG process on the reduced circuit **C'** (box (c)).[14] It is interesting to note that within the context of this section, ATPG is *not used* to detect the stuck-at faults of the initial circuit **C**, but it is *used* to compute extra test vectors which when applied to primary inputs while shifting out test responses will mask the circuit activity and hence lead to reduction in power dissipation (Figure 1). Associated with each fault stuck-at non-controlling value nc_i on wire $F\ S_i$ ($F\ S_i$ *sa* nc_i) in the specified fault list **L** is a set of scan cells whose spurious transitions will be eliminated in the original circuit **C** by applying extra test vector EV_i which detects $F\ S_i$ *sa* nc_i in the reduced circuit **C'**. There-fore based on fault compatibility in the reduced circuit **C'**, scan cell classification in the original circuit **C** is done implicitly which leads to several partitions of the initial single scan chain (box (d)). However, some scan cells may be self-incompatible (Definition 4) which leads to iterations through the ATPG process with a respecified fault list (box (e)) until no self-incompatible scan cells are left. At the end of the *MSC-PARTITIONING* algorithm the multiple scan chains f SC_0; : : : ;$SC_{k\ 1}$;$E\ SC$g and extra test f EV_0; : : : ;$EV_{k\ 1}$g will be used by the novel test application strategy described. In the following each part of the *MSC-PARTITIONING* algorithm is explained in detail.[13]

In the first part of the *MSC-PARTITIONING* of Figure 9 the initial circuit C is transformed into a reduced circuit C' as described in *CIRCUIT-REDUCTION* algorithm of Figure 10. The algorithm also identifies the *freezing signals* which are the signals that depend on primary inputs and should be set to the controlling value as side inputs to the gates which eliminate transitions that originate from scan cells as described in the following parts. Two lists of *eliminated gates* and *modified gates* contain the gates which

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ought to be eliminated and modified respectively in the reduced circuit C'. Initially *eliminated gates* is set to all the scan cells whereas the *modified gates* is void (lines 1-2). The circuit is traversed in breadth first search order using two lists *current frontier* and *new frontier*. While *current frontier* is set initially to all the scan cells of C (line 3), the *new frontier* initially is void (line 4). In the inner loop (lines 6-13) for all the gates neighbours of the current frontier it is checked where input gates already belong to *eliminated gates* (i.e. depend on scan cells). If this is the case then the currently evaluated gate is introduced into *eliminated gates*, removed from *modified gates* (if applicable) and introduced to *new frontier*.[15] If at least one input does not belong to *eliminated gates* then the currently evaluated gate is introduced to *modified gates*. In the outer loop (lines 5-16) while current frontier is not void (i.e. no more gates need to be eliminated) the inner loop proceeds further. At the end of each iteration of the outer loop *current frontier* and *new frontier* are updated (lines 14 and 15). Finally, using the *eliminated gates* and *modified gates* the initial circuit C is modified to the reduced circuit C' (lines 16 and 17) as follows: gates that belong to *eliminated gates* (depend only on scan cells) are excluded; gates that belong to *modified gates* (depend on both scan cells and primary inputs) are modified to gates with input signals dependent only on primary inputs (in the case of gates with two inputs of which one is a freezing signal, the gate is modified to a buffer);[16] all the freezing signals identified in the first step are set as primary outputs in the reduced circuit. Freezing signals f $F\ S_0$; : : : ;$F\ S_{p\ 1}$g, which are the outputs of the gates present in the *modified gates*, are determined simultaneously with identifying independent scan cells (Definition 5). The independent scan cells are grouped into the extra scan chain (ESC) which consists of scan cells whose spurious transitions cannot be eliminated by computing an extra test vector. The algorithm returns not only the reduced circuit C' but also the list of freezing signals that will be used in the following part of the *MSC-PARTITIONING of Figure 9.*

a   Reduce
initial circuit C to
reduced circuit C'

Specify fault list L
for C'

b

ATPG for C' using
fault list L; derive
c   extra test vectors

Classify scan cells   Respecify fault list

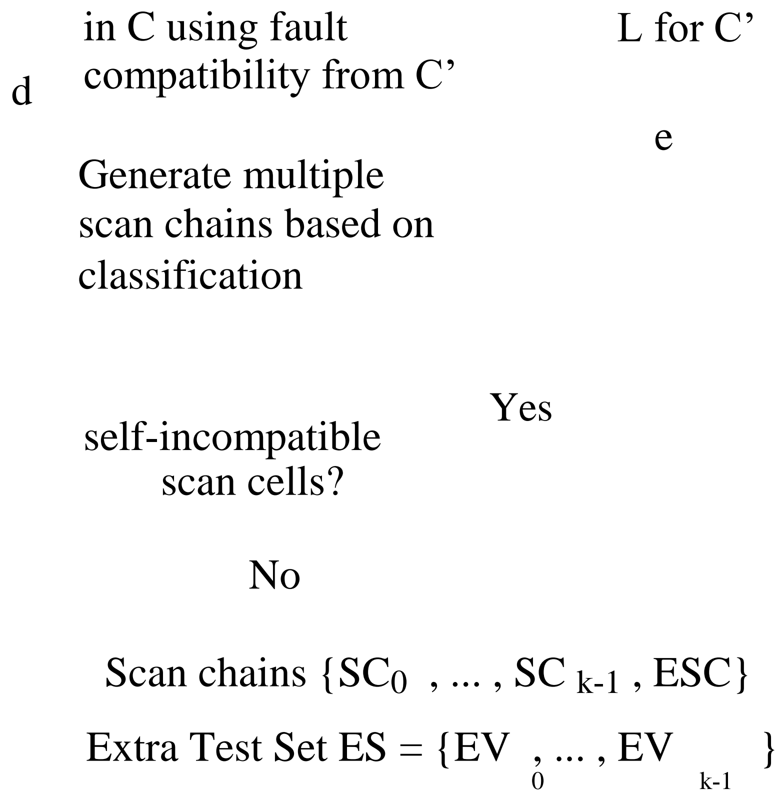

Figure 9: Proposed algorithm for partitioning scan cells in multiple scan chains

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In the second part a specified fault list L is created which will be provided together with the reduced circuitC' to an ATPG tool. Specified fault listL comprises freezing signals F S_i targeting the stuck-at the non-controlling value sa nc_i of the gate g_i from modified gates list of algorithm CIRCUIT-REDUCTION of Figure 10. It is important to note that each fault F S_i sa nc_i has attached a list of scan cells f S_{i0} ; : : : ;$S_{im\ 1}$ g whose spurious transitions in the initial circuit C are eliminated when setting gateF S_i to its controlling value. The list of scan cells is required during generation of scan chains in part d() of the MSC-PARTITIONING algorithm.[17]

*In the third part, having generated the reduced circuit*C' and the specified fault list L, any state of the art combinational ATPG tool can be used to generate test vectors for the faults fromL for C'. Test vectors for the faults fromL are the extra test vectors required to eliminate spurious transitions while shifting test responses in the initial circuitC as described in partd(). Since the freezing signals are primary outputs inC' as described in parta() then L contains faults only on primary outputs. This will clearly speed up the ATPG process since only backward justification and no forward propagation is required. Moreover, the specified fault list is significantly smaller than the entire fault set which will further reduce ATPG computational time for computing extra test vectors. It should be noted that some faults fromL are redundant which implies that no extra test vector can be computed to stop the propagation of the spurious transitions from scan cells associated with the respective fault.[18] However, this scan cells are treated as self-incompatible and handled by re-specifying the fault list as described in the last parte)of(the *MSC-PARTITIONING of Figure 4.9.*

Given the extra test set with a list of faults from L detected by each extra test vector EV_i, scan cell

classification according to definitions is done as follows. If two faults F S_i sa nc_i and F S_j sa nc_j from L are incompatible (i.e. they are not detected by the same extra test vector) then each element of the two lists of scan cells associated with the two faults f S_{i0} ; : : : ;$S_{im\ 1}$ g and f S_{j0} ; : : : ;$S_{jq\ 1}$ g respectively, are incompatible (otherwise they are compatible). This leads to grouping all the scan cells, associated with faults detectable by single extra test vector, into a single scan chain. However, this may lead to self-incompatible scan cells (Definition 4) when different extra test vectors eliminate spurious transitions from the same scan cell. Consequently, while there are self-incompatible the MSC-PARTITIONING algorithm will iterate through parts (e), (c), (d) as explained next.

ALGORITHM: **CIRCUIT-REDUCTION**
INPUT: CircuitC
OUTPUT: Reduced CircuitC'
Freezing Signalsf $F\ S_0$; : : : ;$F\ S_{p\ 1}$g

1 *eliminated_gates* = *f* S_0; : : : ;S_m *1g*
2 *modified_ gates* = Ø
3 *current_frontier* = *f* S_0; : : : ;S_m *1g*
4 *new_frontier* = Ø
5 **while** (*current_frontier* =6 Ø) f
6 **for all** g_x *2 neighbours(current_frontier)*
7 **if** (*all inputs of* g_x *2 eliminated _gates) f*
8 *add* g_x *to eliminated _gates*
9 *remove* g_x *from modified _gates*
10 *add* g_x *to new-frontier*
11 *g*
12 **else**
13 **add** g_x *to modified_gates*
14 *current_frontier* = *new_frontier*
15 *new_frontier* = Ø
16 *g*
17 *generate reduced circuit* **C' as follows f**
18 **eliminate** *all the gates* g_x *2 eliminated_gates*
19 *modify all the gates* g_y *2 modified gates*
20 *g*
21 *freezing signals f F* S_0; : : : ;*F* S_p *1g are output signals of f* g_0; : : : ;g_p *1g* = *modified_gates*
22 *f* S_{e0} ; : : : ;$S_{em\ 1}$ g for which no freezing signal exists are introduced in the extra scan chain **ESC**
23 return Reduced CircuitC'
Freezing signalsf *F* S_0; : : : ;*F* S_p *1g*

Figure 10: Proposed algorithm for circuit reduction for extra test vector computation

In the case that there are self-incompatible scan cells after the generation of multiple scan chains then the problem needs to be addressed as it was briefly explained in example 4. The faults F S_i sa nc_i which have attached self-incompatible scan cells are removed from fault list L and new faults are specified on the lines in the fan out paths ofF S_i. Thus, the respecified fault list L will be provided back to the ATPG process for computing extra test vectors (partc))which(will be followed by new multiple scan chain generation based on fault compatibility (part (d)). This iterative process continues until there are no self-incompatible scan cells left.

The MSC-PARTITIONING algorithm of Figure 9 returns the scan chains of compatible scan cells, the extra scan chain ESC and the extra test set of extra test vectors used to define a new test application strategy, as explained in the following. It should be noted that scan cells are partitioned into multiple scan

chains and extra test vectors are computed without any knowledge of the test set to be applied to achieve the required fault coverage.[19] Therefore, computational time for circuit reduction depends only on the circuit size and structure (number of scan cells and circuit depth) and not on the size of the test set, which makes the proposed solution test set independent and applicable to large scan sequential circuits within low computational time. This is also due to the fact that although ATPG, used for detecting compatible faults in the reduced circuit, is NP-hard, efficient heuristics have been developed that could easily be integrated in the MSC-PARTITIONING algorithm. Note that the low computational time for large scan sequential circuits is achieved with small overhead in test area and test data which is also dependent only on the number of scan chains determined by the proposed MSC-PARTITIONING algorithm.

New Test Application Strategy Using Multiple Scan Chains and Extra Test Vectors

Having partitioned the scan cells into multiple scan chains with an extra test vector for each scan chain, this section introduces a new test application strategy for power minimisation during test application in scan sequential circuits. *Node transition count NTC* = å N_G *fi* C_{load} is used as quantitative measure for power dissipation throughout the section. N_G is the total number of gate output transitions (0 ! 1 and 1 ! 0) and it is assumed that load capacitance for each gate is equal to the number of fan outs (Equation 1).

Multiple Scan Chain Test Application (*MSC-TEST APPLICATION*) algorithm computes the *NT C* during the entire test application period for the given test set S, circuit C, multiple scan chains f SC_0; : : : ;SC_k $_1$;ESCg, and extra test set ES = f EV_0; : : : ;$EV_{k\ 1}$g. Figure 11 gives the pseudo code of the proposed *MSC-TEST APPLICATION* algorithm. The value of NTC is 0 at the beginning of the algorithm and it is gradually increased as the entire test set is traversed. The outer loop represents the traversal of all the test vectors V_i, with i = 0; : : : ;n 1, from test set S. Shifting out test responses through all the scan chains are then considered in the inner loop. For each scan chain SC_j , circuit C is simulated by applying the extra test vector EV_j to primary inputs and $NT\ C_{i;j}$ is added to NTC . $NT\ C_{i;j}$ stands for node transition count while shifting in present state part of test vector V_i through scan chain SC_j and applying extra test vector EV_j to the primary inputs. After shifting out the test responses though each scan chain SC_j the primary input part of test vector V_i is applied to primary inputs and $NT\ C_{i;E\ SC}$ is computed while shifting out test response through the extra scan chain ESC. Finally the entire test vector V_i

is applied to the circuit under test and $NT\ C_{i;LOAD}$ required to load the test response in the scan cells, is added to NTC . After the completion of the inner loop, the outer loop continues until the entire test set is examined. The algorithm returns the value of NTC over the entire test application period. It should be noted that algorithms presented in this section are independent of test vector and scan cell order. Unlike the algorithms from whose computational time is prohibitively large hindering the exploration for large sequential circuits, the proposed *MSC-PARTITIONING* and *MSC-TEST APPLICATION* algorithms have low computational time and can handle large circuits as shown in the following.

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ALGORITHM: MSC-TEST APPLICATION
INPUT: Test Set S=f V_0; : : : ;V_n 1g, Circuit C
Scan Chains f SC_0; : : : ;SC_k 1;ESCg
Extra Test Set ES = f EV_0; : : : ;EV_k 1g
OUTPUT: Node transition count NTC

1 NTC 0
2 for every V_i from S with i = 0; : : : ;n 1 f
3 for every SC_j with j = 0; : : : ;k 1 f
4 apply EV_j to primary inputs; EV_j is uniquely determined for every scan chain SC_j by the *MSC-PARTITIONING* algorithm of Figure 4.10
5 compute $NTC_{i;j}$ by simulating C when shifting in the present state part of test vector V_i through scan cells from SC_j
6 NTC NTC + $NTC_{i;j}$
7 g
8 compute $NTC_{i;ESC}$ by simulating C when shifting in the present state part of test vector V_i through independent scan cells from ESC
9 NTC NTC + $NTC_{i;ESC}$
10 apply primary part of V_i to primary inputs to get the circuit test response and compute $NTC_{i;LOAD}$
11 NTC NTC + $NTC_{i;LOAD}$
12 g
13 return NTC

Figure 11: Proposed test application strategy using multiple scan chains and extra test vectors

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Experimental Results

This section demonstrates through a set of benchmark examples that multiple scan chains combined with extra test vectors, as outlined in, yield savings in power dissipation during test application. The algorithms described in Section 4 were implemented on a 500 MHz Pentium III PC with 128 MB RAM running Linux and using GNU cc version. Shows the reduction in power dissipation at the expense of low overhead in test area and volume of test data, when the proposed multiple scan chains-based technique is employed for power minimisation. It provides a comparison with the BPIC test application strategy presented.

Experimental Results for Multiple Scan Chains-Based Power Minimisation

The average value of *NT C* reported throughout this section is calculated using the Equation 1 from under the assumption of the zero delay model. The use of the zero delay model is motivated by the observation that power dissipation under the zero delay model has a high correlation with power dissipation under the real delay model. Furthermore, due to elimination of spurious transitions the propagation of hazards and glitches is also eliminated leading to even greater reductions for power dissipation in the case of real delay model, as explained.

First column of Table 1 gives the number of scan cells of all full scan sequential circuits from ISCAS89 benchmark set. Second and third columns give the number of scan chains (SC) and the length of the extra scan chain (ESC) respectively computed using the *MSC-PARTITIONING* algorithm outlined. The number of scan chains varies from 2 as in the case of *s208* up to 7 as in the case of *s38584*. The small

number of scan chains implies that both area overhead required to control multiple scan chains and volume of test data overhead caused by extra test vectors are very low since they are proportional to the number of scan chains. For most of the examples the size of the extra scan chain (ESC length) is nil or very low. However, there are two extreme cases as in the case of *s13207* and *s38417* where the number of independent scan cells is very high leading to an increase in ESC length and hence insignificant penalty in power reduction.[20] Furthermore, the computational time is very low ($< 1s$) for small circuits. Moreover, for large circuits which are not handled by previous approached and the best primary input change (BPIC) time test application strategy proposed, as in the case of *s38584*, it takes $<3600s$ to achieve substantial reduction in average value of *NT C*. Table 2 shows the experimental results for all the circuits from ISCAS89 bench mark set using three different ATPG test tools, to further validate the advantages of the proposed test set independent technique.

circuit	Scan Cells	Scan Chains (SC)	ESC length	CPU time (s)
s208	8	2	0	1
s298	14	3	6	1
s344	15	4	4	1
s349	15	4	1	1
s382	21	3	6	1
s386	6	3	0	1
s400	21	3	6	1
s420	16	2	0	1
s444	21	4	6	1
s510	6	4	0	1
s526	21	4	6	1
s641	19	3	0	1
s713	19	3	0	1
s820	5	5	0	1
s832	5	3	0	1
s838	32	2	0	1
s953	29	3	23	1
s1196	18	4	2	1
s1238	18	4	2	1
s1423	74	5	3	2
s1488	6	3	0	3
s1494	6	4	0	3
s5378	179	5	33	49
s9234	211	6	20	201
s13207	638	5	330	472
s15850	534	6	62	596
s35932	1728	2	0	1903
s38417	1636	5	1079	8151
s38584	1426	7	7	3543

Table 1: Experimental results for ISCAS89 benchmark circuits in terms of number of scan chains, extra scan chain (ESC) length, and CPU time, when applying *MSC-PARTITIONING* algorithm

circuit	Test Vectors (TV)	traditional *NT C*	proposed *NT C*
s208	34	54.54	26.67
s298	33	103.56	39.23
s344	24	130.36	42.54
s349	22	131.90	52.59
s382	32	133.91	50.99
s386	74	81.31	63.75
s400	33	135.97	51.88
s420	73	111.69	54.46
s444	33	139.92	47.68
s510	60	123.89	64.38
s526	60	170.61	63.05
s641	58	166.32	60.03
s713	58	173.34	57.15
s820	110	137.52	111.08
s832	115	139.83	115.50
s838	148	227.46	108.24
s953	90	158.50	76.43
s1196	140	101.31	68.12
s1238	151	101.50	65.15
s1423	70	453.58	137.63
s1488	119	340.75	225.81
s1494	125	329.98	266.05
s5378	259	1772.07	527.87
s9234	366	3160.16	760.35
s13207	461	5949.81	2051.55
s15850	436	5260.90	942.07
s35932	65	11067.50	5440.19
s38417	904	15920.00	7159.88
s38584	658	12766.30	3914.41

(a) ATALANTA test set

Table 2: Comparison in *NT C* when using the proposed multiple scan chains and the traditional single scan chain

The first and second columns of Table 2(a) give the circuit name and the number of test vectors (TV) respectively generated using the ATALANTA test tool. Third column shows the initial average

circuit	Test Vectors (TV)	traditional *NT C*	proposed *NT C*
s208	65	55.82	25.93
s298	52	115.74	46.36
s344	62	131.58	48.03
s349	65	132.58	53.63
s382	72	145.63	51.81
s386	109	86.31	58.92
s400	98	107.24	43.82
s420	98	107.24	43.82
s444	77	150.01	49.74
s510	90	115.23	65.86
s526	107	186.24	67.38
s641	99	184.13	60.31
s713	100	196.92	59.92
s820	190	139.01	110.31
s832	200	138.07	114.29
s838	183	199.88	81.15
s953	138	169.70	76.37
s1196	227	105.37	68.37
s1238	240	107.46	66.11
s1423	135	509.96	150.41
s1488	196	347.17	227.33
s1494	191	353.12	237.43
s5378	358	1786.60	531.44
s9234	660	3123.35	754.58
s13207	709	5972.92	2056.18
s15850	643	5487.29	952.92
s35932	129	13039.30	6291.21
s38417	1458	15849.20	7136.23
s38584	989	12871.30	3912.55

(b) ATOM test set

Table 3: Comparison in *NT C* when using the proposed multiple scan chains and the traditional single scan chain

value of *NT C* (traditional *NT C*), which is the total value of *NT C* using the traditional single scan chain design [2] and ALAP test application strategy (Definition 3 in Chapter 3) divided by the total number of clock cycles over the entire test application period. The next column 4 shows the final average value of *NT C* (proposed *NT C*) when using the proposed multiple scan chains and extra test vectors (*MSC-TEST APPLICATION* algorithm.

circuit	Test Vectors (TV)	traditional *NT C*	proposed *NT C*
s208	27	54.94	24.07
s298	23	108.88	43.81
s344	13	124.77	46.69
s349	13	128.91	55.86
s382	25	148.40	55.54
s386	63	85.45	59.09
s400	43	100.60	40.11
s420	43	100.60	40.11
s444	24	156.59	51.87
s510	54	114.04	66.14
s526	49	183.15	67.95
s641	21	176.95	62.92
s713	21	192.82	63.50
s820	93	137.89	112.44
s832	94	138.61	115.29
s838	75	187.63	70.41
s953	76	169.09	76.02
s1196	113	105.47	68.83
s1238	121	103.88	65.24
s1423	20	507.21	150.82
s1488	101	366.18	234.11
s1494	100	371.16	235.81
s5378	97	1809.42	537.51
s9234	105	3045.64	751.093
s13207	233	5977.48	2047.51
s15850	94	5481.82	947.82
s35932	12	10860.50	5374.45
s38417	68	14199.90	6486.23
s38584	110	12901.50	3896.92

(c) MINTEST test set

Table 4: Comparison in *NT C* when using the proposed multiple scan chains and the traditional single scan chain

The same experiment was completed for non-compact test sets generated by ATOM test tool (Table 2(b)) and compact test sets generated by MINTEST compaction tool (Table 2(c)) respectively. It should be noted that all the three test sets achieve 100% fault coverage.

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circuit	power reduction (%)		
	ATALANTA	ATOM	MINTEST
s208	51.09	53.54	56.18
s298	62.10	59.94	59.75
s344	67.36	63.49	62.57
s349	60.12	59.54	56.66
s382	61.91	64.42	62.57
s386	21.59	31.73	30.84
s400	61.84	59.13	60.12
s420	51.23	59.13	60.12
s444	65.91	66.84	66.87
s510	48.03	42.84	42.01
s526	63.04	63.82	62.89
s641	63.90	67.24	64.43
s713	67.02	69.57	67.06
s820	19.22	20.64	18.45
s832	17.39	17.22	16.82
s838	52.41	59.39	62.47
s953	51.77	55.03	54.99
s1196	32.75	35.11	34.74
s1238	35.81	38.47	37.19
s1423	69.65	70.50	70.26
s1488	33.73	34.51	36.06
s1494	19.37	32.76	36.46
s5378	70.21	70.25	70.29
s9234	75.93	75.33	75.84
s13207	65.51	65.57	65.74
s15850	82.09	82.63	82.70
s35932	50.84	51.75	50.51
s38417	55.02	54.97	54.32
s38584	69.33	69.60	69.79

(a) Power reduction

Table 5: Comparison of experimental data for ATALANTA, ATOM, and MINTEST test sets.

It can be clearly seen that the proposed test application strategy has significantly smaller average value of *NT C* for all the benchmark circuits when compared to initial value of *NT C* computed using the traditional test application strategy from which employs a single scan chain.

circuit	volume of test data overhead (%)			test area overhead (%)
	ATALANTA	ATOM	MINTEST	
s208	3.26	1.70	4.11	10.00
s298	1.06	0.67	1.53	11.33
s344	4.68	1.81	8.65	11.11
s349	5.11	1.73	8.65	11.11
s382	0.78	0.34	1.00	9.09
s386	2.18	1.48	2.56	10.33
s400	0.75	1.08	2.46	10.63
s420	1.45	1.08	2.46	9.52
s444	1.13	0.48	1.56	11.04
s510	5.06	3.37	5.62	10.52
s526	0.62	0.35	0.76	11.11
s641	3.35	1.96	9.25	8.00
s713	3.35	1.94	9.25	8.00
s820	3.55	2.05	4.20	12.50
s832	2.04	1.17	2.49	10.71
s838	0.69	0.56	1.37	4.65
s953	0.51	0.79	0.93	6.81
s1196	0.93	0.57	1.16	6.81
s1238	0.86	0.54	1.08	4.16
s1423	1.06	0.55	3.73	3.79
s1488	1.44	0.87	1.69	4.16
s1494	1.82	1.19	2.28	6.12
s5378	0.25	0.18	0.67	2.60
s9234	0.11	0.19	0.69	2.06
s13207	0.07	0.04	0.15	0.91
s15850	0.14	0.09	0.67	0.92
s35932	0.06	0.03	0.33	0.25
s38417	0.01	0.01	0.09	0.38
s38584	0.02	0.01	0.14	0.42

(b) Overhead in volume of test data and test area

Table 6: Comparison of experimental data for ATALANTA ATOM and MINTEST test sets

To give an indication of the reductions in power dissipation, Table 3 shows the percentage reduction in power dissipation (Table 3(a)) and percentage overhead in volume of test data (columns 2-4 of Table 3(b)) and test area (column 5 of Table 3(b)).

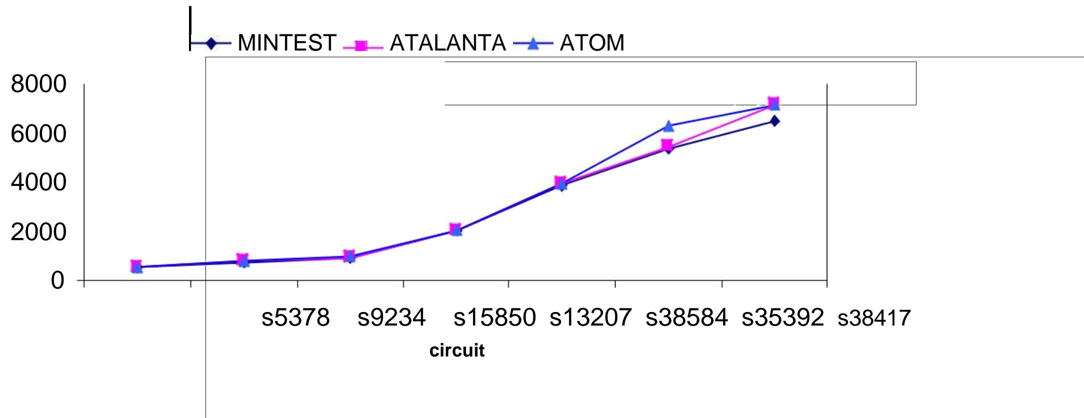


Figure 12: Curve illustrating the test set independent final value of *NT C*

The power dissipation is considered directly proportional to the average value of *NT C*. The test area overhead represents the extra logic required to multiplex the scan output signal (Figure 1) and it is computed accurately by synthesising and technology mapping the ISCAS89 circuits to AMS 0.35 micron technology. The volume of test data over-head represents the number of extra bits required for the extra test vectors (the number of scan chains multiplied by the number of primary inputs). Note that test area overhead decreases as the complexity of the circuit increases. This is due to the fact that extra area occupied by scan control register and selection logic required to control multiple scan chains is very small when compared to the size of large sequential circuits. The power reduction varies from approximately 82% as in the case of *15850* down to under 17% as in the case of *s832* when employing MINTEST. It should be noted that moderate power reduction as in the case of *s386*, *s510*, *s820*, *s832*, *s1488*, *s1494* is due to very small number of scan cells (5 to 6 scan cells only as shown in Table1) which are difficult to be partitioned in multiple scan chains. However, for modern complex digital circuits where the number of scan cells is significantly higher (1426as in the case of *s38584*) the power

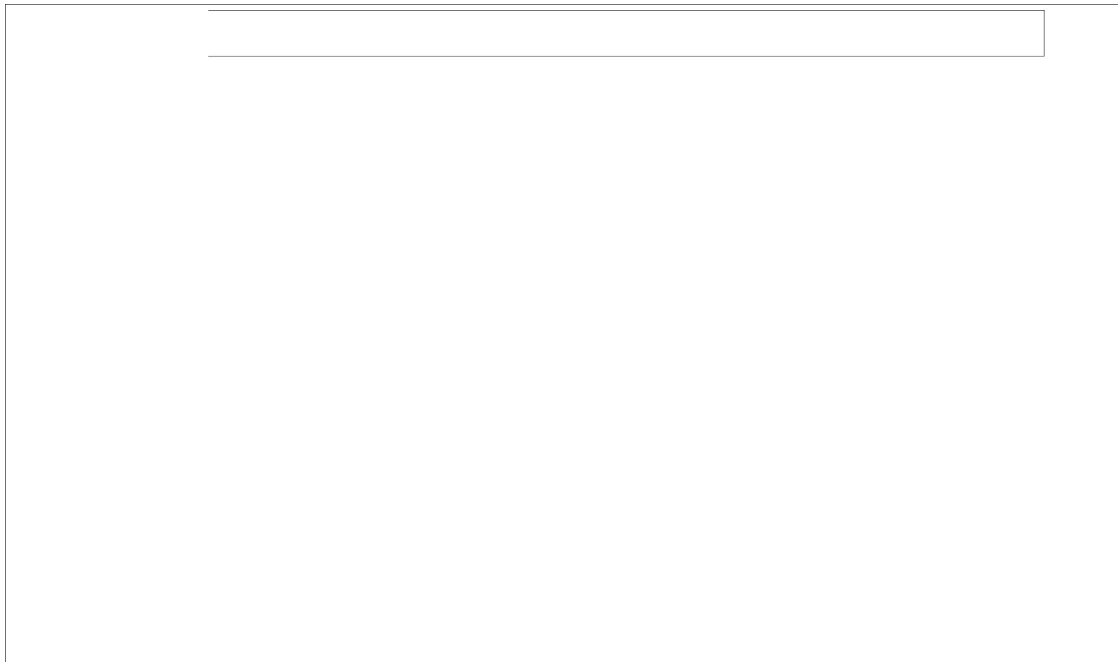
reduction is up to 69% at the expense of insignificant < 1% volume of test data and test area overhead. This clearly shows the advantage of the proposed power minimisation technique for large scan sequential circuits.

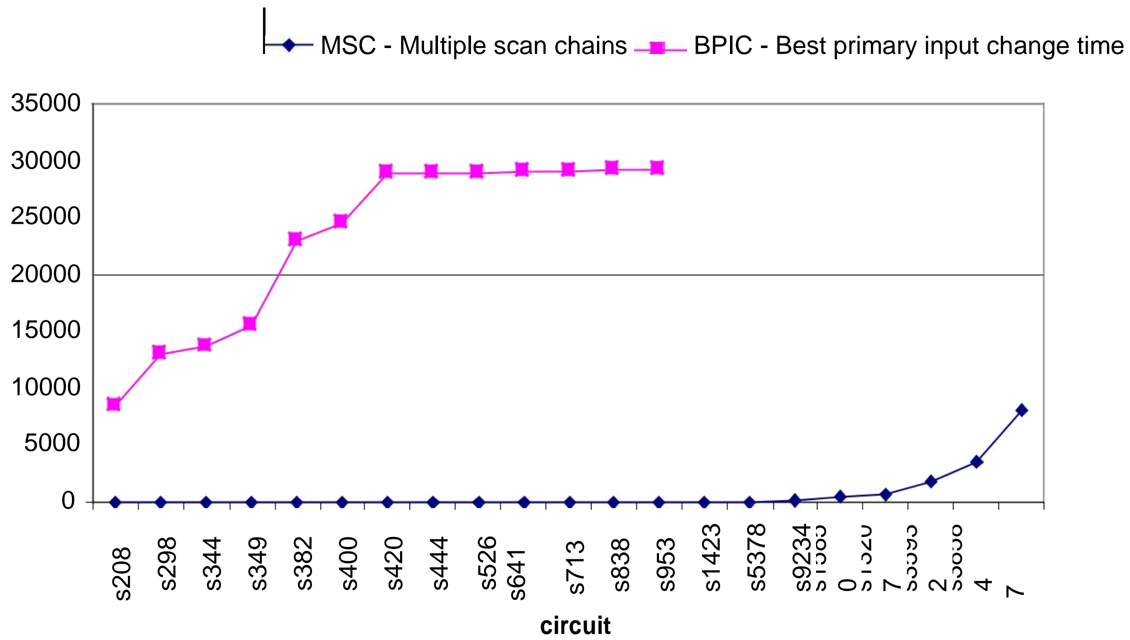
A further advantage of the proposed technique is that due to its test set independence the final average value of *NT C* is predictable within a given range of values regardless of test vectors applied to the circuit. This is justified by the fact that the proposed low over-head area multiple scan chain architecture is not overly sensitive to the values of test vectors since only a single chain is active at a time and the spurious transitions within the combinational circuit are eliminated by the extra primary input vector *regardless* of the value loaded in non-active scan chains. This is shown in Figure 12 where the graphs for average value of *NT C* for 7 largest ISCAS89 benchmark under three different size test sets are given. For all three test sets MINTEST, ATALANTA and ATOM the average values of *NT C* are approximately equal. This implies that the proposed technique can further be applied to more DFT methodologies such as scan-based BIST where regardless of the value of the pseudorandom test set the savings in power dissipation are guaranteed and final values of *NT C* are predictable.

Comparing Multiple Scan Chains-Based Power Minimisation and Best Primary Input Change Test Application Strategy

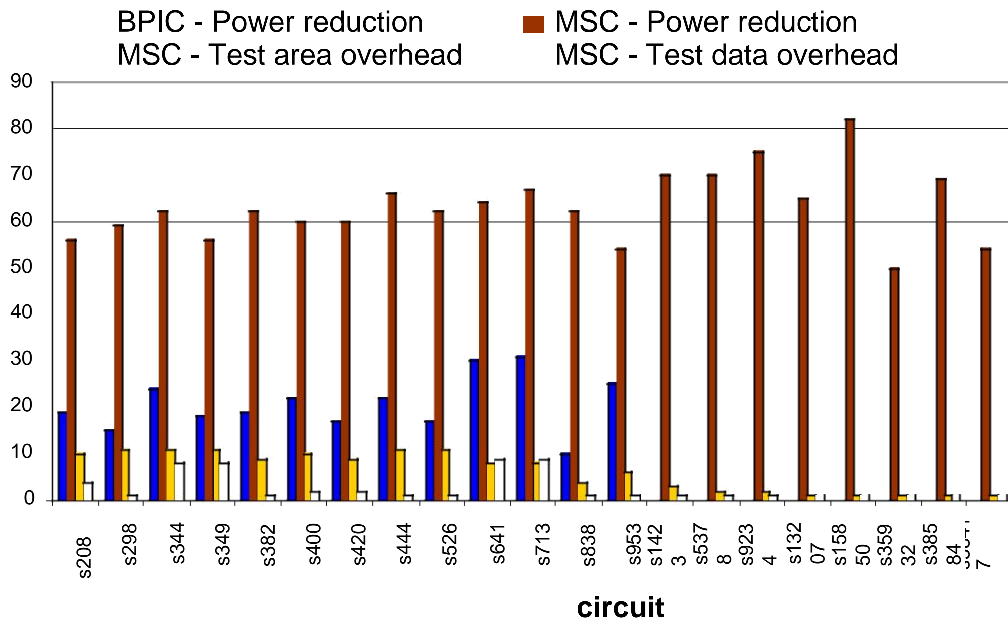
In order to show the suitability of the new multiple scan chain-based technique for large scan sequential circuits, a comparison, in terms of power reduction, overhead in volume of test data, test area, and computational time, for BPIC test application strategy proposed in this research paper and multiple scan chains-based technique, is given in Figure 13. It can be concluded from Figure 13(a), in the case of large sequential circuits which are infeasible for computing the best primary input change time using the test set dependent approach, the test set independent solution presented. Is applicable with low computational

time. For example, BPIC is computationally intractable for all the large scan sequential circuits, while multiple scan chains-based power minimisation yields considerable savings in power dissipation with low overhead in volume of test data and test area. For example circuit *s953*, the 25% savings in power dissipation in the case of BPIC (Chapter 3) are significantly smaller when compared to 54% savings in the case of multiple scan chains-based technique. This is achieved at the expense of additional overhead of 6% in test area, and 1% in volume of test data, as shown in Figure 13(b). However, for small to medium sized circuits where design space exploration of a small number of scan cell and test vector orderings is feasible within reasonable computational limits, BPIC is applicable since it has no penalty in test area, performance, test efficiency, test application time or volume of test data.





(a) Computational time



(b) Power reduction and overhead in test area and test data

Figure 13: Comparison in power reduction, overhead in volume of test data and test area, and computational time for BPIC test application strategy introduced and the newly proposed multiple scan chains (MSC) technique, when using MINTEST

Concluding Remarks

This research paper has presented a new technique based on multiple scan chains and it has shown how with low overhead in test area and volume of test data, and with no penalty in test application time, test efficiency, or performance, considerable savings in power dissipation during test application in large scan sequential circuits can be achieved in very low computational time. The technique is based on a new DFT architecture and a novel test application strategy. When compared to traditional approach which consists of a single scan chain, the proposed technique reduces spurious transitions in circuit under test leading to substantial reduction in power dissipation. The proposed technique is test set independent with no penalty in test application time. Substantial power savings are achieved for both compact and non-compact test sets, with no penalty in test efficiency. The newly introduced DFT architecture (Figure 1) does not introduce any penalty in performance, and it yields savings in clock tree power dissipation for *all* the test vectors of a very small test set where each test vector is essential, as described. The proposed DFT architecture requires low overhead in test area to control multiple scan chains, which are successfully combined with extra test vectors in the newly introduced test application strategy. Since a high number of extra test vectors emerges as a problem to testers which need to change to support the large volume of test data, the proposed technique based on a small number of extra test vectors introduces low overhead in volume of test data. Moreover, due to the efficient algorithms described in the proposed technique is computationally inexpensive, which makes it suitable for large sequential circuits. Finally, the synthesisable extra hardware required by the new DFT architecture introduced in, the efficient algorithms and the novel test application strategy described, make the technique proposed in this chapter easily embeddable in the existing VLSI de-sign flow using state of the art third party electronic design automation tools.

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