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Design and Implementation of Area Efficient Self Timed Adders for Low Power Applications in VLSI

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ABSTRACT:

In today's world there is a great need for low power design and area efficient high performance in DIP (Digital Image Processing) system. In this paper the proposed method presents a parallel single-rail self-timed adder. It uses recursive method for performing multi bit binary addition. This design attains good performance without any special speedup circuitry. A practical implementation is provided along with a completion detection unit. The implementation is regular and does not have any practical limitations of high fan outs. The recursive method based adder consumes least power among other Self-timed adders. In our work this can be reduced with proposed adder. This technique presents a pre-processing and post processing adder to minimize the multiplier technique. A high fan-in gate is required though but this is unavoidable for asynchronous logic and is managed by connecting the transistors in parallel. Simulations have been performed using cadence tool and superiority of the proposed approach over existing asynchronous adders. In this proposed system we are using a parallel prefix adder it is used to reduce the power consumption, area efficiently.

KEYWORDS: Asynchronous circuits, binary adder. CMOS design digital arithmetic, multiplier technique.

INTRODUCTION:

Low power has emerged as a principal theme in today‟s electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Binary addition is the single most important operation that a processor performs. Polonky et al. (1999) proposed an self-timed adder based on DI RSFQ primitives Self-timed or asynchronous design solves these problems by removing a global clockMost of the adders have been designed for synchronous circuits even though there is a strong interest in clockless/asynchronous processors/circuits. .Asynchronous circuits do not assume any quantization of time. Therefore, they hold great potential for logic design as they are free from several problems of clocked (synchronous) circuits. Aniset et al. (2002) presented an theory based on PMOS devices need to be sized up to attain the gate‟s performance. In principle, logic flow in asynchronous circuits is controlled by a request-acknowledgment handshaking protocol to establish a pipeline in the absence of clocks. Explicit handshaking blocks for small elements, such as bit adders, are expensive. Cornelius et al. (2006) presented a new technique these dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic circuit. Therefore, it is implicitly and efficiently managed using dual-rail carry propagation in adders. In this principle, logic flow in asynchronous circuits is mainly controlled by a request-acknowledgment handshaking protocol to establish a pipeline in the absence of clocks. Explicit handshaking blocks for small elements, such as bit adders, are expensive. Choudary et al. (2010) presented a technique based on which they proposed an addition operation since in ALU all other arithmetic operations can be derived interms of addition operationonly. Therefore, it is implicitly and efficiently managed using dual-rail carry propagation in adders.Self-timed refers to logic circuits that depend on and/or engineer timing assumptions for the correct operation. Self-timed adders have the potential to run faster averaged for dynamic data, as early completion sensing can avoid the need for the worst case bundled delay mechanism of synchronous circuits.

PIPELINED ADDERS USING SINGLE RAIL ENCODING:

The asynchronousReq/Ack handshake can be used to enable the adder block as well as to establish the flow of carry signals. These dual-rail signals can represent more than two logic values (invalid, 0, 1) and therefore can be used to generate bit-level acknowledgment when a bit operation is completed.

DELAY INSENSITIVE ADDERS USING DUAL RAILENCODING:

Delay insensitive (DI) adders are asynchronous adders that assert bundling constraints or DI operations. There are many variants of DI adders, such as DI ripple carry adder (DIRCA) and DI carry look-ahead adder (DICLA). DI adders use dual-rail encoding and are assumed to increase complexity

GENERAL BLOCK DIAGRAM OF PASTA:

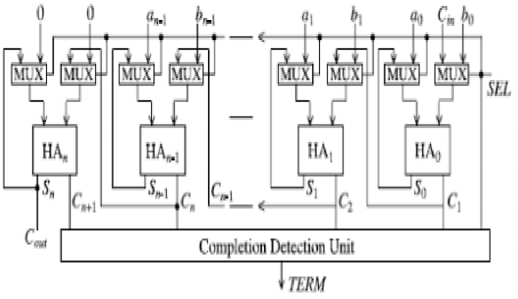


Fig 1: General block diagram of pasta

The general architecture of the adder is shown in Fig. 1. Theselection input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and will switch to feedback/carry paths for subsequent iterations using SEL = 1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero values.C.

RECURSIVE FORMULA FOR BINARY ADDITION:

Let S j i and C j i+1 denote the sum and carry, respectively, for i th bit at the j th iteration. The initial condition (j = 0) for addition is formulated as follows

$$S0i= ai \oplus bi \ (1.1)$$

$$C0i+1 = ai\ bi \ (1.2)$$

The j th iteration for the recursive addition is formulated by

$$S\ ji = S\ j-1 \oplus C\ j-1 \quad 0 \le i < n \ (1.3)$$

$$C\ ji+1= S\ j-1i\ C\ j-1 \quad 0 \le i \le n \ (1.4)$$

The recursion is terminated at kth iteration when the following condition is met:

$$Ck\ n + Ck\ n-1+ \cdots +Ck = 0,\ 0 \le k \le n$$

PROPOSED ADDER:

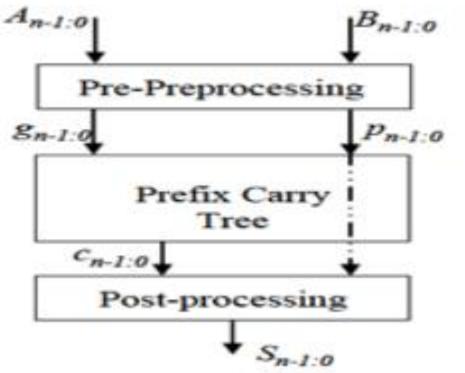
The addition of two binary numbers can be formulated as a prefix problem a new technique for high speed in speculative completion The corresponding parallel-prefix algorithms can be used for speeding up binary addition and for illustrating and understanding various addition principles. This section introduces a mathematical and visual formalism for prefix problems and algorithms

Two categories of prefix algorithms can be distinguished; the serial prefix, and the treePrefix Problems. In a prefix problem, n outputs (yn-1, yn-2, …., y0) are computed from ninputs (xn-1, xn-2, ….,x0) using an arbitrary associative operator

Tree-prefix algorithms include parallelism for calculation speed-up, and therefore form the category of parallel-prefix algorithms. It represents a serial algorithm for solving the prefix problemIn the prefix tree, there are n columns, corresponding to the number of input bits. The gates performing the • operation and which work in parallel are arranged in the same row, and similarly, the same gates connected in series are placed in consecutive rows. Thus, the number of rows m corresponds to the number of binary operations to be evaluated in series. The sum bits, si are finally obtained from a post processing step.

$$g_i = a_i \cdot b_i$$

$$p_i = a_i \oplus b_i;$$



Block diagram of parallel prefix adder

In the above equation, „.‟ operator is applied on two pairs of bits and, these bits represent generate and propagate signals used in addition. The output of the operator is a new pair of bits which is again combined using a dot operator „ ‟ or semi-dot operator „ ‟ with another pairs of bits. This procedural use of dot operator „ ‟ and semi-dot operator „ ‟ creates a prefix tree network which ultimately ends in the generation of all carry signals.In the final step, the sum bits of the adder are generated with the propagate signals of the operand bits and the preceding stage carry bit using a xor gate. Choudary(2008) proposed a new technique for basic arithmetic operation for higher automation The semi-dot operator „ ‟ will be present as last computation node in each column of the prefix graph structures, where it is essential to compute only generate term, whose value is the carry generated from that bit to the succeeding iterations

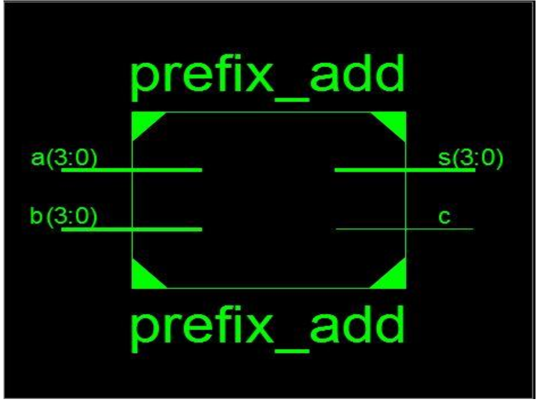


Fig 2: Block diagram of prefix adder

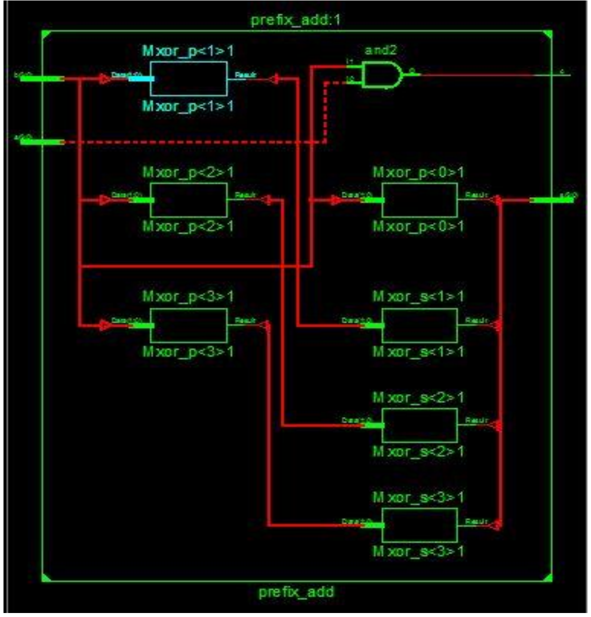


Fig 3: Rtl of prefix adder

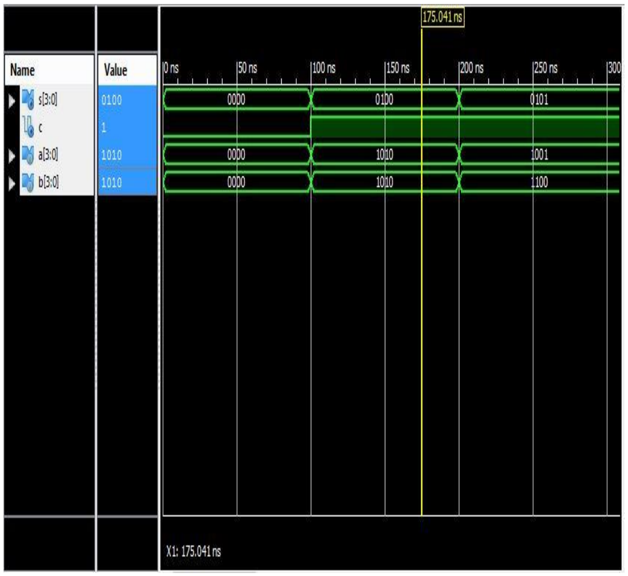


Fig 4: Simulation result of prefix adder

CONCLUSION:

A parallel prefix adder design is proposed for overall power consumption. The proposed adder provides overall area and power than the previous methods. The parallel asynchronous self timed adder circuit is efficiently described using a handshaking protocol and also compared with other adders proposed adders. The MAC unit is implemented and the process is achieved efficiently. Simulation results demonstrate the effectiveness of the proposed framework in parallel prefix adder using multiplication through addition process. The proposed method is implemented using digital CADANCE environment

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