International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 12
April 2018

Design and Analysis of Seven Level Inverter Topology with Realiable Configuration for Open End Winding Induction Motor

Lalu Mudavath & T.Dinesh
[1]Assistant professor, Department of EEE, Anurag group of Engineering(CVSR Engineering college), Venkatapur(V), Ghatkesar(M), Hyderabad.
[2]Assistant professor, Department of EEE, Anurag group of Engineering(CVSR Engineering college), Venkatapur(V), Ghatkesar(M), Hyderabad.

ABSTRACT-*In This paper proposes a seven level inverter fed induction motor with much reduced number of power electronic components. Nowadays, Multilevel inverters are mostly used due to these advantages with low harmonic distortion content, reduced circuit complexity, reduced number of switches, improved voltage quality and less voltage stress on power electronic devices. The proposed topology has been designed by connecting the multiple number of three phase two level inverters in back to back arrangement. The power quality is proportional to the number of levels in the output voltage waveform, however increasing the levels in output voltage beyond certain limit is not economical and adoptable. This question of limit on the level is also addressed in this paper. More over the voltage rating of the input DC voltage source in this topology is one third of that of the existing established topologies. A simple single triangular pulse width modulation scheme is incorporated. By using the simulation results we can analyze the proposed multilevel inverter. The proposed topology has been simulated using Matlab®/Simulink with six pole (5 HP) induction motor.*

Keywords— Multilevel Inverter, Power Quality, Pulse Width Modulation.

I. INTRODUCTION:

Nowadays with the rapid development of world industrial scenario the quantity of outcome from the industries is also enormously increased which further leaded to the great demand of high power requirement in the industries. The conventional power electronic devices and the three phase two level inverters are not effective to handle these high power industrial applications. In the past few decades the rapid evolution in the area of power electronic devices and along with the designers orientation together these two factors leads to the invention of different topologies of multilevel inverters[1] with low harmonic distortion content, reduced circuit complexity[2-3],reduced number of switches[4-5], improved voltage quality and less voltage stress on power electronic devices. Numerous pulse width modulation schemes are proposed for multilevel inverters[6-9].

The main three topologies multilevel inverters which are widely used in the industrial electronic applications are Diode/Neutral point clamped multilevel inverter[10], Flying capacitor multilevel inverter[11-12] and cascaded H-Bridge multilevel inverter[13]. In the NPC multilevel inverter the total DC link voltage will be divided into equal parts depending on the number of output voltage levels required. For this purpose capacitors should be incorporated due to which unequal voltage balancing problem raises and as the number levels increases clamping diodes increases tending to make the circuit more complex.

In FC multilevel inverter clamping should be done with the help of capacitors. Due the excess number capacitors and their charging, discharging time intervals unequal voltage distribution and commutation failures will occur. The CHB topology with isolated voltage sources is best suited for high voltage application. Since there are no secondary capacitors and clamping diodes so there will be no voltage balancing issues. However as the level increases the number of isolated sources increases and hence the number of power electronic components which makes the circuit and its control complex. For the researchers the other factors of concern are the overall drive should be less complex, more reliable and efficient.

II.DYNAMICMODELLING OF INDUCTION MOTOR:

The numbers of identical windings per phase are always half of the total number of poles[14-17]. Since in the proposed topology we are aiming for an output phase voltage of seven level, so the induction motor should contain six poles in its stator winding. Each identical winding contains two terminals so all the six terminals of respective stator windings will be taken out and these three set of windings will be connected in series. All the three windings are separated equally with respect to stator resistance and stator leakage reactance and each identical winding voltage is equal to one third of respective phase voltage in the stator winding. The identical profile winding voltage equations are given by

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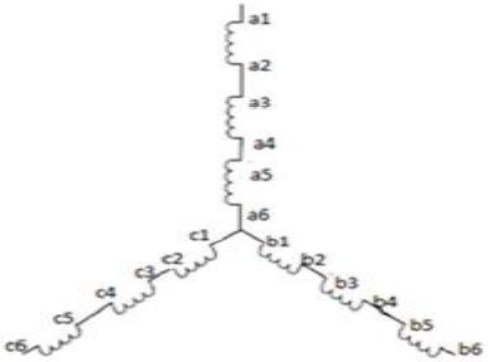
$$V_{a1} - V_{a2} = \left(\frac{r_s}{3}\right) * i_{as} + \left(\frac{L_{ss}}{3}\right) * i_{as} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{3}\right) * i_{bs} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{3}\right) * i_{cs} \quad (1)$$

$$V_{a3} - V_{a4} = \left(\frac{r_s}{3}\right) * i_{as} + \left(\frac{L_{ss}}{3}\right) * i_{as} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{3}\right) * i_{bs} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{3}\right) * i_{cs} \quad (2)$$

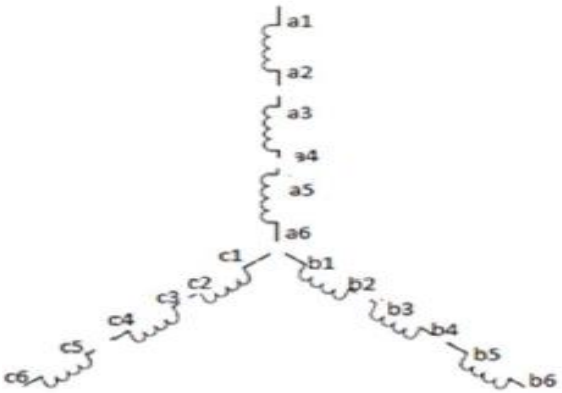
$$V_{a5} - V_{a6} = \left(\frac{r_s}{3}\right) * i_{as} + \left(\frac{L_{ss}}{3}\right) * i_{as} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{3}\right) * i_{bs} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{3}\right) * i_{cs} \quad (3)$$

Sum of all these three individual voltages gives the effective voltage across the phase 'A' winding of stator.

$$V_a = (V_{a1} - V_{a2}) + (V_{a3} - V_{a4}) + (V_{a5} - V_{a6}) \quad (4)$$



(a)



(b)

Figure(1): Induction Motor Stator Winding (a) Normal Arrangement (b) Proposed Winding Voltage equations in dq0 reference frame can be solved from the basic equations of induction motor [18].

$$V_{qs} = r_s * i_{qs} + \omega * \lambda_{ds} + \rho * \lambda_{qs}$$
$$V_{ds} = r_s * i_{ds} + \omega * \lambda_{qs} + \rho * \lambda_{ds}$$
$$V_{0s} = r_s * i_{0s} + \rho * \lambda_{qs}$$
$$V_{qr} = r_r * i_{qr} + (\omega - \omega_r) * \lambda_{dr} + \rho * \lambda_{qr}$$
$$V_{dr} = r_r * i_{dr} - (\omega - \omega_r) * \lambda_{qr} + \rho * \lambda_{qr}$$
$$V_{0r} = r * i_{0r} + \rho * \lambda_{0r} \quad (5)$$

The flux linkage equations are given by

$$\lambda_{qs} = L_{ss} * i_{qs} + L_M * i_{qr}$$
$$\lambda_{ds} = L_{ss} * i_{ds} + L_M * i_{dr}$$
$$\lambda_{0s} = L_{1s} * i_{0s}$$
$$\lambda_{qr} = L_{rr} * i_{qr} + L_M * i_{qs}$$
$$\lambda_{dr} = L_{rr} * i_{dr} + L_M * i_{ds}$$
$$\lambda_{0r} = L_{1r} * i_{0r} \quad (6)$$

The developed electromagnetic torque in terms of dq0 axis current is

$$T_e = \left(\frac{3}{2}\right) * \left(\frac{P}{2}\right) * L_m * \left(i_{qs} * i_{dr} * i_{ds} * i_{qr}\right) \quad (7)$$

Where

d: direct axis,
q: quadrature axis,
s: stator variable,
r: rotor variable,
Vds and Vqs: q and d–axis stator voltages,
Vdr and Vqr: q and d–axis rotor voltages,
r_r : Rotor resistance,
vr_s: Stator resistance,
L1s: stator leakage inductance,
L1r : rotor leakage inductance,
iqs ,ids: q and d–axis stator currents,
iqr, idr: q and d–axis rotor currents,
p: number of poles,
J: moment of inertia,
Te : electrical output torque,
TL : load torque.

Proposed seven level inverter topology:

III PROPOSED SEVEN LEVEL INVERTER TOPOLOGY:

The proposed seven level inverter topology is shown in figure(2). Total six terminals of each stator phase winding will be taken out. Each of the above six terminals fed by a separate inverter. All these six inverters will contain a single DC link voltage "Vdc/3". In the figure(2) (S11 to S16),(S21 to S26),(S31 to S36),(S41 to S46),(S51 to S56) and (S61 to S66) are the switches of respective inverters one to six. The complementary switches are (S11,S12),(S13,S14),(S15,S16) for the first inverter and in the similar manner remaining inverters complementary switches exist. (S1 to S6) and (S1' to S6') are the isolating switches needed to isolate the middle four inverters during the voltage levels of -2Vdc/3,- Vdc/3,0,Vdc/3,2Vdc/3. The possible seven levels of phase 'A' voltages are -Vdc,-2Vdc/3,-Vdc/3,0,Vdc/3,2Vdc/3,Vdc.

The proposed topology comparison with existing topologies is shown in table(1). It can be observed that it is far better than the NPC topology excluding the clamping diodes and it is superior to CHB topology which requires separate DC sources.

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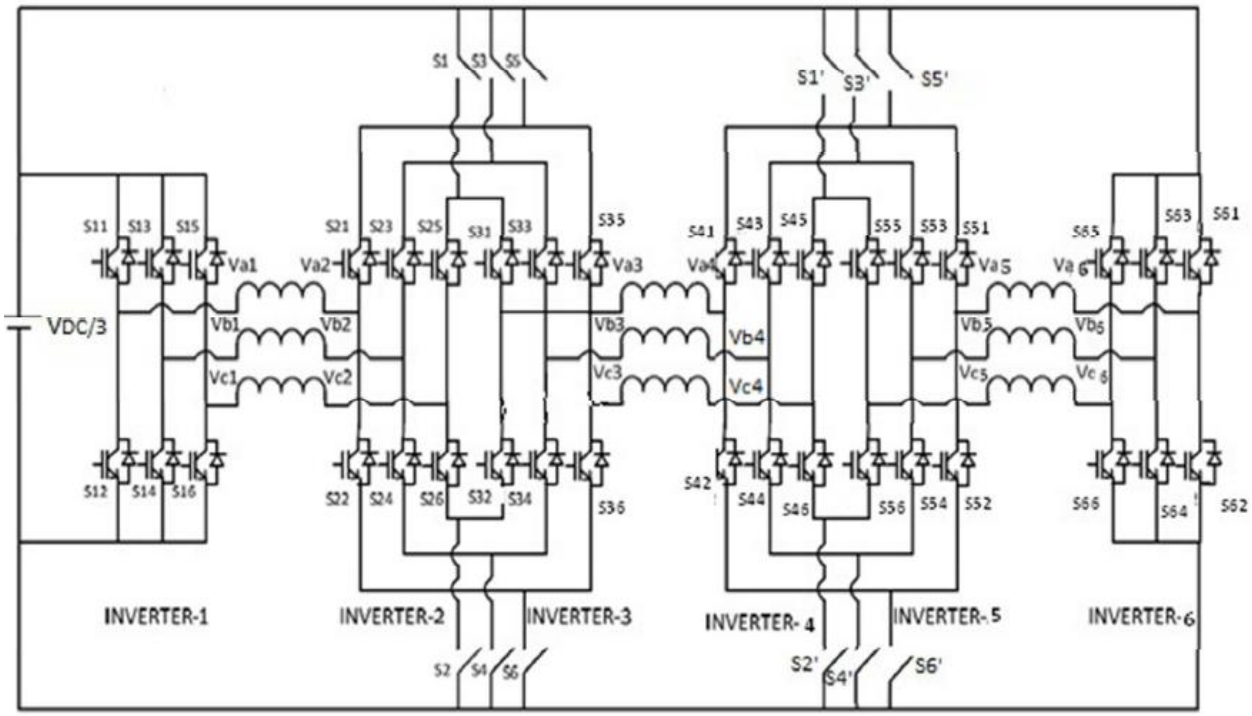
Comparing with the FC topology the clamping capacitor and capacitor voltage balancing issues can be excluded.



Figure(2): Proposed Seven Level Inverter Topology

Table (1): Comparison of Different Topologies

	NPC inverter	FC inverter	CHB inverter	Proposed inverter
Number of switches	36	36	36	36
Clamping Diodes	30	0	0	0
Isolated sources	1 (Vdc)	1 (Vdc)	12 (Vdc/3)	1 (Vdc/3)
Capacitors	6	36	0	0
Bidirectional switches	0	0	0	12

IV. SINGLE TRIANGULAR PULSE WIDTH MODULATION:

A single triangular pulse width modulation contains a single reference sine wave at 50 Hz and six carrier (triangular) signals [19]. Reference sine wave is of 50 Hz and carrier wave of 3 KHz.

Table (II): Comparison of Modulating And Carrier Waves For Different Voltage Levels

Modulating areas of reference and carrier waves	Output voltage levels
Vm>Vcr1	+Vdc
Vcr2<Vm<Vcr1	+2Vdc/3
Vcr3<Vm<Vcr3	+Vdc/3
Vcr4<Vm<Vcr3	0
Vcr5<Vm<Vcr4	-Vdc/3
Vcr6<Vm<Vcr5	-2Vdc/3
Vm<Vcr6	-Vdc

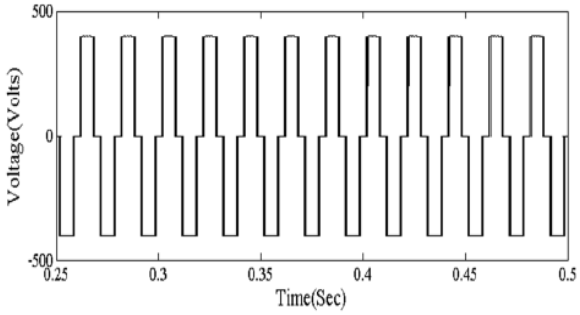
Operating areas and respective voltage levels of proposed topology when

- Vm>Vcr1; (S11,S22),(S31,S42),(S51,S62) of phase 'A' are operating giving a voltage of "+Vdc".
- Vcr2<Vm<Vcr1; (S11,S22),(S31,S42),(S52,S62) of phase 'A' are operating giving a voltage "+2Vdc/3".
- Vcr3<Vm<Vcr2; (S11,S22),(S32,S42),(S52,S62) of phase 'A' are operating giving a voltage "+Vdc/3".
- Vcr4<Vm<Vcr3; (S12,S22),(S32,S42),(S52,S62) of phase 'A' are operating giving a voltage "0".
- Vcr5<Vm<Vcr4; (S12,S22),(S32,S42),(S52,S61) of phase 'A' are operating giving a voltage "-Vdc/3".
- Vcr6<Vm<Vcr5; (S12,S22),(S32,S41),(S52,S61) of phase 'A' are operating giving a voltage "-2Vdc/3".
- Vm<Vcr6; (S12,S21),(S32,S41),(S52,S61) of phase 'A' are operating giving a voltage "-Vdc".

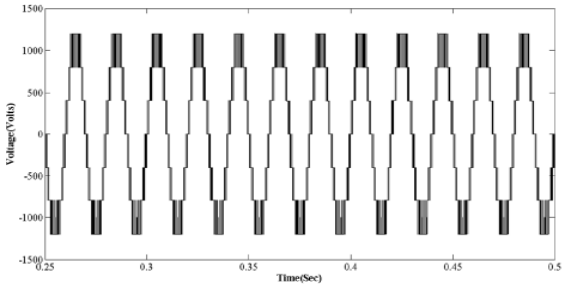
V.SIMULATION RESULTS:

The proposed topology has been simulated on 5HP induction motor. The individual voltages across three sectionalized phase 'A' windings are

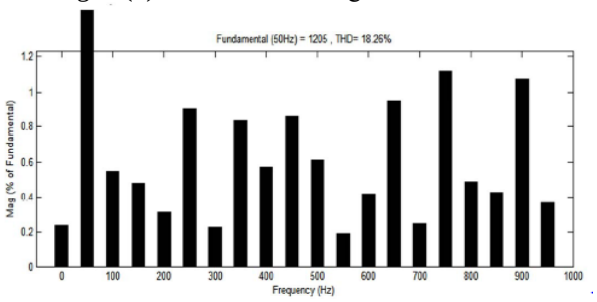
$(V_{a1} - V_{a2})$ $(V_{a3} - V_{a4})$and $(V_{a5} - V_{a6})$These individual voltages are of 3 level. The effective voltage of phase 'A' winding will be $(V_{a1} - V_{a2})$ + $(V_{a3} - V_{a4})$+ $(V_{a5} - V_{a6})$which is of seven level.



Figure(3): Three level voltage of sectionalized winding voltage of phase 'A'

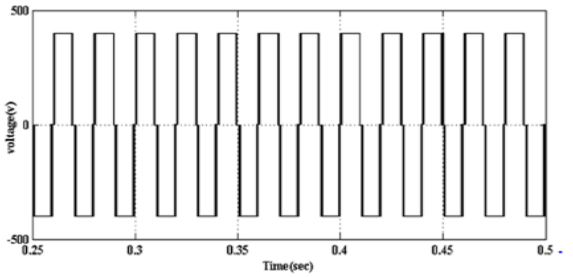


Figure(4): seven level voltage of Phase 'A'



Figure(5): THD of Seven Level Phase Voltage

In case if any of the switch or total bridge get failure due to internal or external fault condition the continuity of supply to the induction motor will not be interrupted i.e. only that part of sectionalized winding which is attached to the respective faulted bridge should be treated as faulted part and the remaining bridges will operate at normal condition. Since the fault is not affecting the remaining sectionalized windings now the total topology will operate at a phase voltage of 3 level hence there by increasing the reliability of the total system.



Figure(6): Three level phase 'A' voltage at bridge failure condition

VI .CONCLUSION:

In this paper a new topology of seven level inverter with less number of switches has been proposed and simulated with 5 HP six pole induction motor consisting of three identical voltage profile coils per phase in stator. The output phase voltage waveforms have been presented. If in the case of any one of the internal bridges (2, 3, 4, 5) failures the resultant topology will become three level inverter and hence there by increasing the reliability of the overall system. By using the single triangular pulse width modulation the triplen harmonics are almost shifted to carrier frequency having less impact on the system and improving overall efficiency of the system. Increasing the level beyond seven is not economical and adoptable for low and medium range induction motor drives. So it is suggested to maintain the output phase voltage level as seven and the THD content is also in acceptable range.

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