International Journal of Research Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 07
March 2018

Power Line Communication CMOS Receiver Design for UWB Communication

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Abstract— As the circuit complexity increases, the number of internal nodes increases proportionally, and individual internal nodes are less accessible due to the limited number of available I/O pins. To address the problem, we proposed power line communications (PLCs) at the IC level, specifically the dual use of power pins and power distribution networks for application/ observation of test data as well as delivery of power. A PLC receiver presented in this paper intends to demonstrate the proof of concept, specifically the transmission of data through power lines. The main design objective of the proposed PLC receiver is the robust operation under variations and droops of the supply voltage rather than high data speed. The PLC receiver is designed and fabricated in CMOS 0.18-μm technology under a supply voltage of 1.8 V. The measurement results show that the receiver can tolerate a voltage drop of up to 0.423 V for a data rate of 10 Mb/s. The power dissipation of the receiver is 3.26 mW under 1.8 V supply, and the core area of the receiver is 74.9 μm × 72.2 μm.

Index Terms— Design-for-testability (DFT), PLC at ICs, PLC receiver, power line communications (PLCs).

I. INTRODUCTION

WITH each new generation of deep submicrometer VLSI technologies, testing, debugging, and diagnosis of VLSI circuits become more difficult and expensive. In addition to higher circuit complexity for a deeper submicrometer technology, larger process variations, greater interconnection delays relative to transistor switching time, and larger leakage current also contribute to make the testing more challenging. It is a general consensus among test engineers that accessibility, i.e., controllability and observability, to internal nodes for both 2-D and 3-D ICs is essential to address the testing problems [1]–[12]. Conventional design-for-testability (DFT) methods, such as scan design, provide dedicated or shared signal paths between I/O pins and internal nodes [13]–[15]. As the circuit complexity increases, the number of internal nodes increases proportionally, and individual internal nodes are less accessible due to the limited number of available I/O pins.

One promising approach to provide ubiquitous accessibility to internal nodes is the dual use of power pins and power distribution networks (PDNs) for data communications as well as power delivery, which is essentially power line communications (PLCs) at the IC level [1]. The PLC at the IC level would be useful for low data rate communications such as scan design, system debugging, and fault diagnosis. The approach also eliminates the need to route a data path from the node to an external data pin. To the best of our knowledge, PLC in an IC environment was exclusively reported in [1] and [21]–[29]. Fig. 1 shows the conceptual PLC system in an IC environment considered for our research. A test instrument sends the data superimposed on the supply voltage of a system board. The signal travels through a power pin(s), the power planes of a package, and the PDN, and then it reaches at the intended node(s). The PLC receiver embedded inside a chip extracts the data from the power line. All the previous PLC receivers designed in [21]–[23], [25]–[27], and [29] report only the simulation results. This paper presents a PLC receiver, whose main design objective is robust operation under supply voltage variations and droops. The proposed PLC receiver was designed and fabricated in CMOS 0.18-μm technology with a supply voltage of 1.8 V.

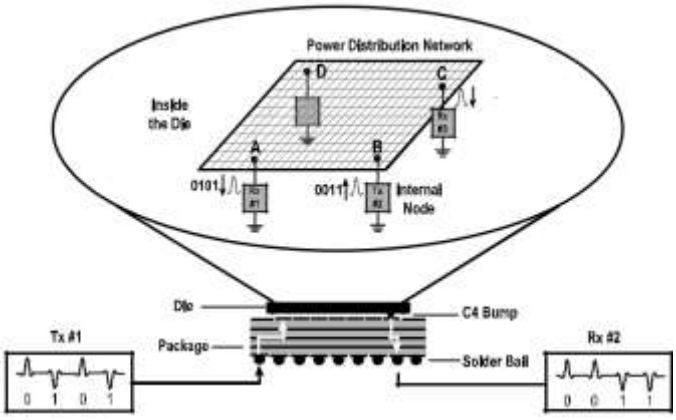

Fig. 1. Proposed conceptual PLC system in an IC environment.

The remainder of this paper is organized as follows. Section II provides the background of the proposed work, specifically operating conditions of PLC in ICs and our previous works. Section III describes the proposed PLC receiver and its building blocks. Section IV presents the measured results. Section V provides the conclusions and the future works for PLC in ICs.

II. Preliminaries

A. Operating Environment

applications as power lines of residential buildings and long distance transmission lines. First, power lines of a chip are very noisy due to factors, such as cyclostationary background noise, resulting from switching synchronous to the main and subclocks, strong deterministic components at frequencies corresponding to those clocks, and low-frequency (20–100 MHz) noise resulting from the resonances of the PDN [16]. Resultantly, the signal-to-noise ratio (SNR) of PLC at the IC level is low, which would require special treatments. One rudimentary approach is to increase the signal level of the data superimposed on the supply voltage. However, the superimposed data signal should not affect the integrity of the supply voltage, and the variations of the supply voltage for ICs should remain less than ±10% [17]. Second, the supply voltage varies and droops in space. It is caused by the factors such as nonideal voltage regulators, IR drop, and varying power consumption of underlying blocks. Bernstein *et al.* [30] reported that the supply voltage droop ranges from 3% to 15% of the supply voltage across the chip area. Therefore, it is necessary for a PLC receiver in an IC to overcome large voltage variations and droops. Third, a PDN is heavily damped with the decoupling capacitors connected to power lines. It intends to reduce the slew rate of current variations by locally supplying or sinking currents and suppress voltage and current ringings at power lines. Consequently, a PDN behaves as a low-pass filter, which prevents high-frequency data signals from propagating through the PDN. The problem is aggravated when a data signal travels through the power and ground planes of the package shown in Fig. 1.

B. Previous Works

To the best of our knowledge, we are the only group who reported the works on PLC in ICs in [1] and [21]–[29]. Our group proposed PLC in ICs to reduce the pin count, size, and hence the cost of a chip initially [21] and later to increase the channel capacity for the multiple parallel scan design in [1]. To follow up the proposal, we investigated several relevant topics for PLC in ICs, and reviewed them briefly as follows.

We measured the propagation loss from a core power supply pin to an on-chip node of a PDN of a cold Pentium 4 die (65 nm version) [24]. The largest passband was observed 2 GHz over a 200-MHz band, and the path loss increases above 40 dB beyond 2.5 GHz. Other measurements were carried out on three different samples of cold 45-nm Core 2 Duo processors and two randomly picked locations on the PDNs [28]. The averaged transfer function shows narrow sporadic passbands, where about 5% 7% of the input signal passes through the PDN. We observed that there is little correlation between the passbands of the 65 nm Pentium 4 and that for the 45-nm Core 2 Duo processors.

PLC at the IC level faces a different set of technical challenges from that of the traditional PLC over suc

We suggested the use of ultrawideband (UWB) and direct-sequence code division multiple access (DS-CDMA) communication technologies to circumvent the blocking of data signals in low frequencies at packages and PDNs and increase the SNR [21], [22], [25]. Compared with the traditional narrow-band communication systems,UWB signaling has several advantages, such as high data rate, low average power, and simple RF circuitry [31]. Shannon's theorem states that the channel capacity is given as $B \times \log_2(1 + SNR)$, where B is the bandwidth [32]. As the bandwidth is much larger (on the order of several gigahertz) for UWB than a narrow-band signal, the SNR can be much smaller for UWB to achieve the same data rate. The DS-CDMA technology assigns a codeword to each bit of information called spreading, and orthogonal codewords are assigned to different users or power pins for the PLC in ICs to support multiple channels. The spreading operation represents 1 bit of data as a series of binary pulses spread over a codeword, which increases the pulse repetition frequency. The benefit of spreading is the processing gain, which is $10 \times \log(spreading\_factor)$ in decibel. For example, the spreading factor for 4-bit codewords is 4, which yields a processing gain of 6 dB, or increases the SNR by 6 dB. We also investigated the modeling of I/O pads and PDNs, and estimated the performance of the proposed PLC systems [22], [25].

We designed several versions of PLC receivers and transmit-ters for the proposed PLC system in ICs [23], [25]–[27], [29]. The first PLC receiver was designed in TSMC 0.18-μm CMOS process [23]. Transient simulations indicate that the PLC receiver can recover data from impulses with the ampli-tude of 90 mV and the period of 300 ps superimposed on the supply voltage of 1.8 V. The pulse repetition rate of the impulses is 1 GHz. A PLC receiver based on a correlator is reported in [26], and its improved version is reported in [27]. Another PLC receiver based on a differential Schmitt trigger is presented in [29]. Design of a transmitter for the proposed system is reported in [25]. All the above PLC receivers and transmitters report only simulation results.

This paper presents a PLC receiver whose main design objective is the robust operation under voltage variations and droops of the supply voltage. The PLC receiver intends to demonstrate the feasibility of a robust receiver as a proof of concept. Therefore, regular pulses (rather than UWB) with a low repetition frequency of 10 Mb/s and a simple amplitude shift keying (ASK) are adopted for the receiver. The receiver was designed and fabricated in CMOS 0.18-μm technology with a supply voltage of 1.8 V.

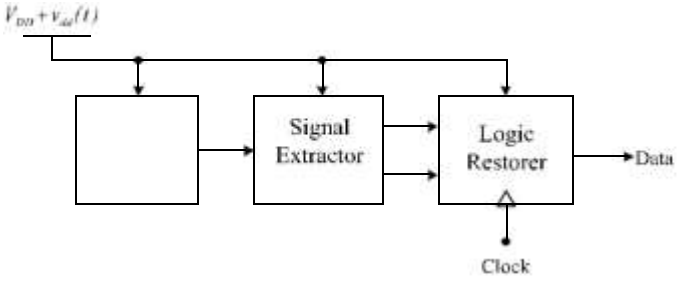

Fig. 2. Block diagram of the proposed PLC receiver.

system design (such as adoption of UWB and DS-CDMA technologies) and the circuit design such as a differential Schmitt trigger adopted for the proposed PLC receiver.

III. Proposed PLC Receiver

The proposed on-chip PLC receiver receives the data superimposed on power lines, and the data (such as scan test data) are sent from a test instrument. Therefore, the transmitter for the PLC receiver is an external instrument rather than the one on the same chip. The receiver was designed in CMOS 0.18-μm technology with a supply voltage of 1.8 V. It consists of three building blocks, and this section describes the design of each building block.

A. Block Diagram

A block diagram of the proposed PLC receiver is shown in Fig. 2. The proposed PLC receiver consists of three blocks, each sharing the same supply voltage ($V_{DD} + v_{dd}(t)$). The first block is a level shifter, which lowers the dc level of the signal superimposed on the supply voltage. The level-shifted signal is processed by the subsequent block, a signal extractor, which amplifies the signal and converts it to a differential signal. The logic restorer, which is a differential Schmitt trigger, recovers logic values from the differential signal. The design and operation of each block is explained below.

B. Level Shifter

The level shifter shown in Fig. 3 can be treated as a common source amplifier with diode-connected load as in which the amplifier input is fixed to a bias voltage V_{bias}.

The level shifter propagates the data signal $v_{dd}(t)$ imposed on the supply voltage V_{DD} to the output while lowering the dc voltage level of the signal to 0.5 V_{DD}. To propagate the data signal superimposed on the supply voltage to the output, the output should be sensitive to supply voltage variations. In other words, contrary to a typical amplifier design, the power supply

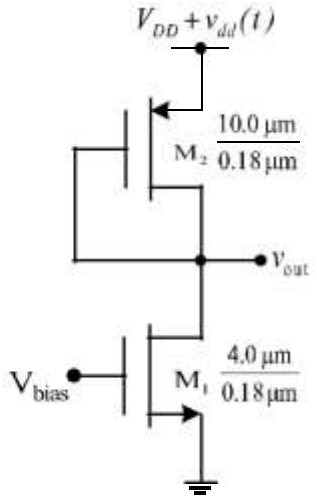

Fig. 3. Level shifter.

where A_v is the small-signal voltage gain from the input (i.e., the gate of M_1) to the output of the amplifier, and $A_{V_{DD}}$ is the small-signal gain from the power supply to the output. A_v is obtained as

$$A_v \approx -\frac{g_{m1}}{g_{m2}} \tag{2}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. $A_{V_{DD}}$ is obtained as in (3) and becomes 1 ignoring the channel length modulation [34]

$$A_{V_{DD}} = \frac{r_{o1}}{1/g_{m2} + r_{o1}} \approx 1. \tag{3}$$

Thus, the PSRR of a common source amplifier is expressed as

$$\text{PSRR} \approx -\frac{g_{m1}}{g_{m2}}. \tag{4}$$

The transconductance of a MOS transistor is

$$g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH}). \tag{5}$$

By substituting (5) in (4), the PSRR becomes

$$\text{PSRR} \approx \frac{\mu_n (W/L)_1 (V_{GS} - V_{TH})_1}{\mu_n (W/L)_2 (V_{GS} - V_{TH})_2}. \tag{6}$$

Equation (6) indicates that the PSRR can be lowered by setting $(W/L)_1$ small, $(W/L)_2$ large, the overdrive voltage of M_1 small, and the overdrive voltage of M_2 large. This means that the bias voltage and the W/L ratio of M_1 should be set to small, while operating M_1 in saturation. Since the desired dc voltage level at the output of the sensing circuit is 0.5 V_{DD}, the condition sets the overdrive voltage of M_2.

superimposed on power lines to the operation of digital circuits.

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