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Design of High Performance Power Efficient Flip Flops using Transmission Gates

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Abstract— Flip-flop plays a major role in designing a synchronous circuits and memory. In this paper we have shown the comparison of performance for various circuits of flip flops, master-slave flip flops and transmission gates .FFs are mostly used to collect the group of data for a storage purpose and the performance includes delay, area minimization and power reduction. The delay can be minimized by transistor sizing and variation of voltage. The proposed circuits are simulated and compared using 90nm and 45nm technology.

Keywords—flip-flops, masterslave, transmission gates, circuit optimization.

I. INTRODUCTION

The main purpose of flip- flops is used as data path structure and allowed for collection of data proceeded by combinational circuits and synchronization operation off level signal [5]. When the critical path occurs in the placement of FF a small data to output delay can be exhibited as well as when the circuit speed is primary concern, the logical effort can be concerned. FF can be simple or clocked, during the past 12 years the development has so much of low power FF have been created. According to actual chip design, the convenient FF is mostly used as a preferred flip-flop because it is well balanced in power, performance and cell area [5]. The most popular and simplest FF is transmission gate and many of them have proposed in the past. It includes charge and discharge of internal node, minimization of area, power dissipation and absence of pre-charge [5]. To get comparable results the analysis makes more difficult for the simulation of latches and FF using various design styles. The focus on this paper is to give helpful information about the comparison of various circuits by calculating their delay, performance and area.

In existing system, the speed performance of traditional one is always outperforms the existing system. The improvement can be increased by transistor sizing and variation in voltage. The delay can be calculated by two parameters: data to out and clock to out. The design strategy for high speed design includes transistor sizing between master and slave, sizing to increase the speed of the flip-flop [5]. The sizing between master and slave include the behavior of whole block inverter+ transmission gate. In proposed work the delay can be further decreased by sizing of transistors and variation in voltage.

Timing behavior

Timing behavior if FF can be defined by two parts,

- Data to clock (D-Clk)
- Clock to output (Clk-Q)

The overall timing of a FF can be introduced and sum of the above contribution is affected by the clock duration. The influence of FF timing on pipeline speed performance can be minimized by the parameter data to output [5].

The minimum time between a data change and the trigger edge of clock pulse is defined as *setup time,* by assuming the wide clock pulse the output will be guaranteed to change as to become equal to new data value [4].

The minimum time that the data signal must be held constant after the triggering edge of the clock signal [4].

II. PROPOSED WORK

In the proposed work we make further modification to improve the performance of various circuits by varying the values of the size of transistor and voltages. The comparison results show that the proposed work outperforms the traditional one. It shows that by doing the sizing and change of voltage, the delay can be minimized the average power and peak voltage can be calculated. The comparison results can be shown in simulation and analysis section and it has been done using 45nm and 90 nm technology, so it will provide the better information from the comparison. Here section III deals with the simulation and analysis of various circuits and the final view of the paper is concluded in section IV.

The comparison of the results can be determined by the sizing of transistors by keeping PMOS as 240nm and NMOS as 120 nm and it can be varied by including the number of transistors. Voltage is kept as 1.5V and the same values are place for both 90nm and 45nm.

III. SIMULATION AND ANALYSIS

1. C^2MOS MS FLIPFLOP

The transmission gates are completely replaced with clock gating transistors in C^2MOS Master-slave flip-flop. The gate inverters can be derived from the inverter plus Transmission gate [5]. The delay can be calculated from the rising and falling edge of the given output [5].

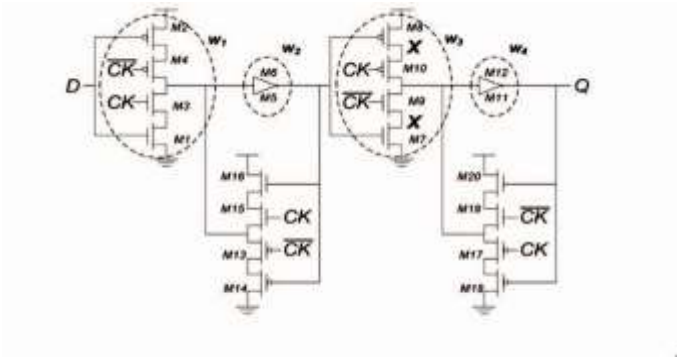

Fig1. C^2MOS flipflop[5]

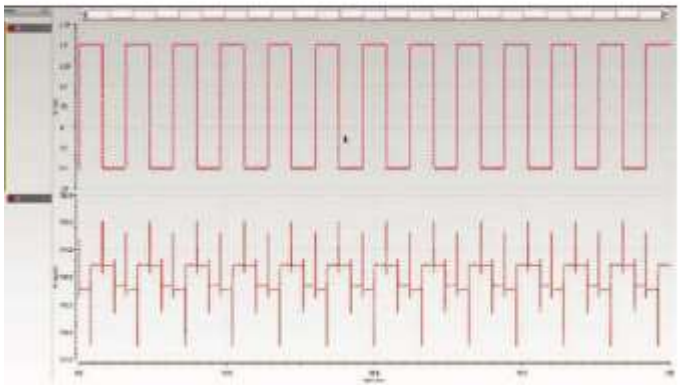

Fig2. Output waveform on cadence simulation (90nm)

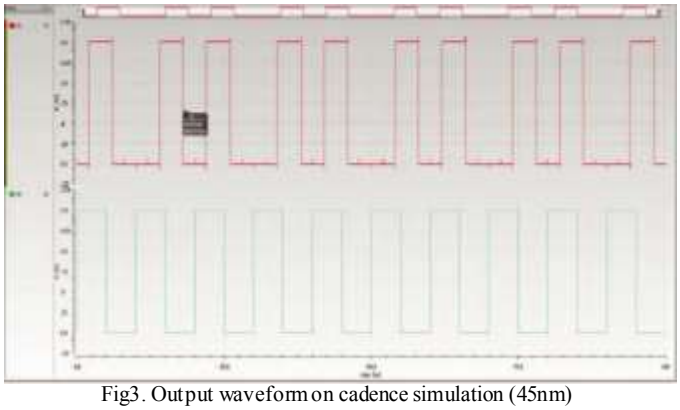

Fig3. Output waveform on cadence simulation (45nm)

2. MODIFIED C^2MOS LATCH

Modified C^2MOS master slave latch is simple and symmetric in structure [4]. Here gate inverters are used to express all critical transistor width as a function of one variable. The iterative procedure can be taken for optimizing the delay and power which cannot be obtained at same time [4].

Size of the transistor is varied according to the increase of transistors and the average power and delay can be calculated using the output signal and the peak voltage can be calculated from maximum voltage values. The values can be varied by changing the transistor size and voltages.

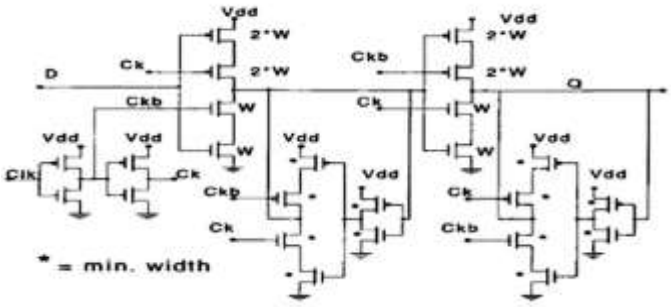

Fig4. Modified C^2MOS latch[4]

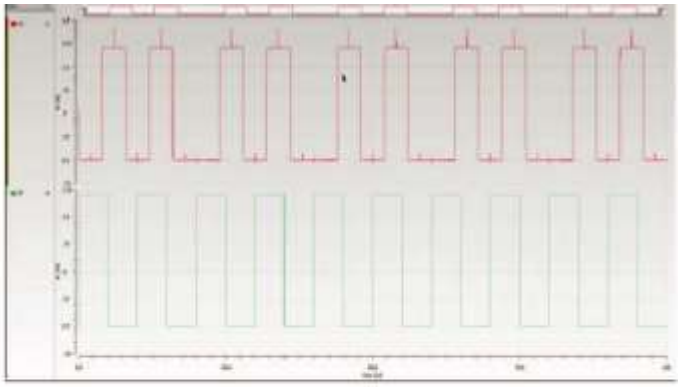

Fig5. Output waveform on cadence simulation (90nm)

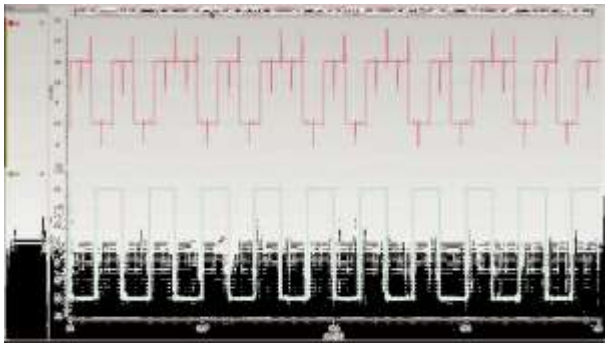

Fig6. Output waveform on cadence simulation (45nm)

3. HYBRID LATCH FLIPFLOP

One of the FF used in high speed design is Hybrid latch flip-flop. Power delay product is very less because of this the speed of the circuit can be increased [4]. The main advantage of this circuit is because of its robustness to clock skew [4].

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the power distribution [4]. It is very suitable for high performance circuits.

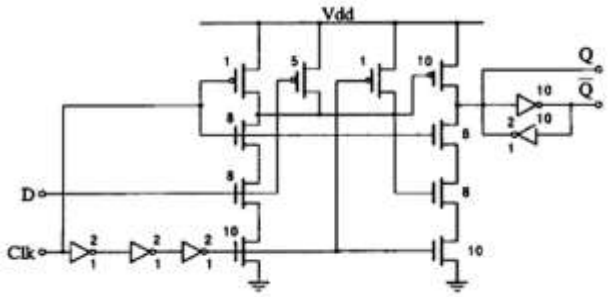


Fig7.Hybrid latch flipflop[4]

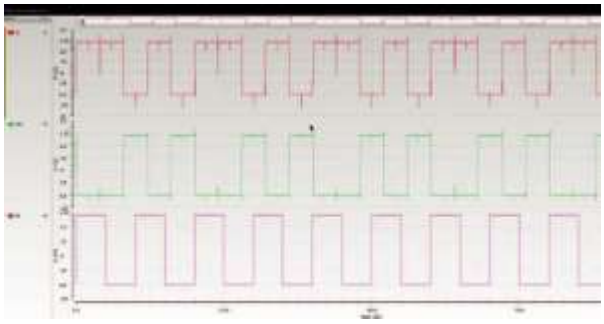
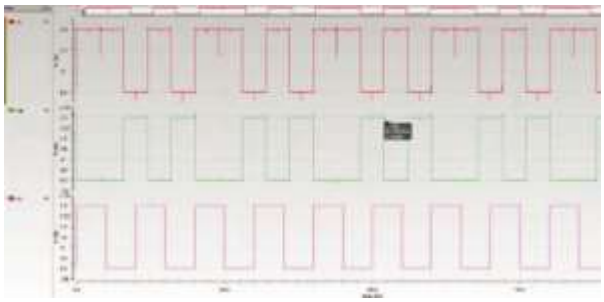


Fig8.Output waveform on cadence simulation (90nm)



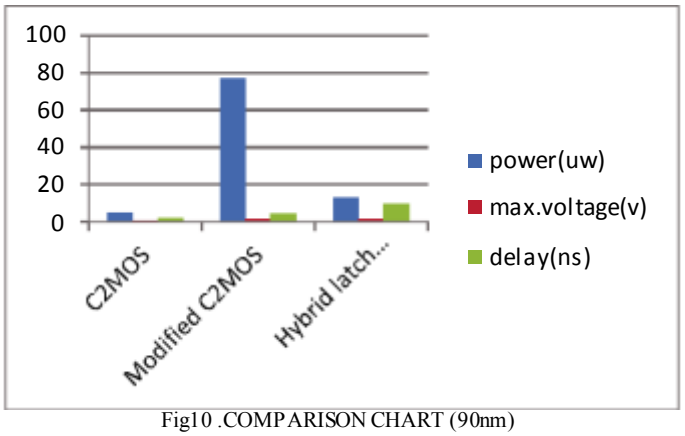


Fig10 .COMPARISON CHART (90nm)

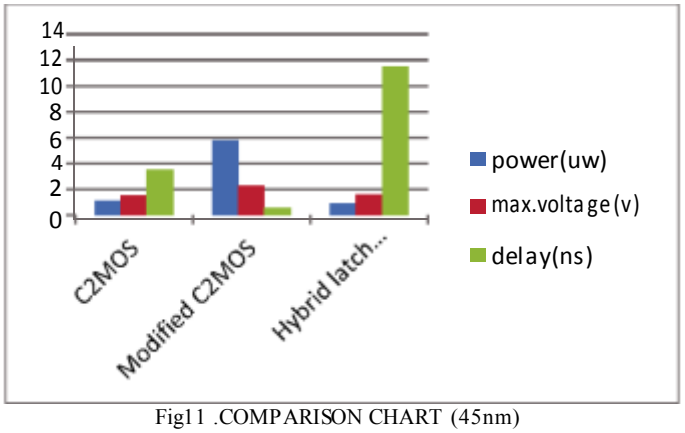


Fig11 .COMPARISON CHART (45nm)

From the table we shown that the comparison of various circuits using 90nm and 45nm, by using 45nm we can reduce the area further and delay can also be varied. Here the power is reduced compared to 90nm technology which leads to

improve the performance.

IV. CONCLUSION

In this work, the high speed design deal with the sizing of various circuits includes transmission gates, master slave, latches and flip-flops. The implementation of proposed circuits in 45nm shows the power saving and delay reduction. The performance is increased according to the sizing of transistors and variation in voltage. As a final view the comparison result shows the performance of proposed work.

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