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4 Bit Comparator Design Based on Reversible Logic Gates

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***Abstract*—Today, reversible logic circuits has attracted considerable attention in improving some fields like nanotechnology, quantum computing, and low power design. In this paper 4 bit reversible comparator based on classical logic circuit is represented which uses existing reversible gates. In this design we try to reduce optimization parameters like number of constant inputs, garbage outputs, and quantum cost. The results show that, the proposed comparator has 4 quantum cost and one constant input less than the prior design.**

***Index Terms*—reversible gates; reversible comparator; quantum cost; constant inputs; garbage outputs**Quantum cost refers to the cost of the circuit interms of primitive gate [4].

In proposed paper, 4 bit reversible comparator is designed. First of all, in section II some reversible logic gates, which are used in circuit construction, are described. Classical implementation of comparator is represented in section III. New design of 4 bit reversible comparator and comparing with prior design are presented in section IV and V, respectively. Finally, the conclusion is made in section VI.

II. BASIC REVERSIBLE LOGIC GATE

I. INTRODUCTION

Reversible logic has been considered as one of the promising practical strategies for power-efficient computing [1]. R. Landauer shows when one bit of information loses, KTln2 joules of energy dissipate (K is the Boltzman's constant and T is the operational temperature) [2]. Later, Bennett [3] proved that this energy could be saved by using reversible logic circuit. In fact, when the inputs cannot be recovered from circuit's outputs, information loss appears. Reversible logic circuits can handle this issue. In this logic, one to one mapping exists between the inputs and outputs, the number of inputs and outputs is equal, and inputs can be recovered from outputs. Reversible logic circuit utilizes in many applications such as nanotechnology, quantum computing, optical information processing, and quantum dot cellular automata (QCA). In order to achieving an optimized reversible circuit, some points should be considered:

1) Fan-out is forbidden.
2) Feedback and loop are not allowed.
3) Delay should be minimum.
4) Optimization parameters should be minimum. The parameters such as number of reversible gates, number of constant inputs, garbage outputs, and quantum cost (QC) can be named as optimization parameters and are defined as:

1) The inputs, which equal to 0 or 1, are constant inputs.
2) Garbage outputs are output vectors which do not generate any useful function.

In this section, some basic reversible gates, which are used in comparator structure, are introduced. These gates are NOT gate, N-bit Controlled-Not Gate, TR gate and BJN gate.

1×1 NOT gate, which has the zero quantum cost, is demonstrated in Fig. 1.

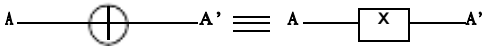


Figure 1. 1*1 NOT gate

N-bit Controlled-Not Gate is shown in Fig. 2. Its quantum cost is equal to n-1. In this gate, Q = A', when all of the control inputs are 1. Else, if only one of the control inputs is zero, Q = A.

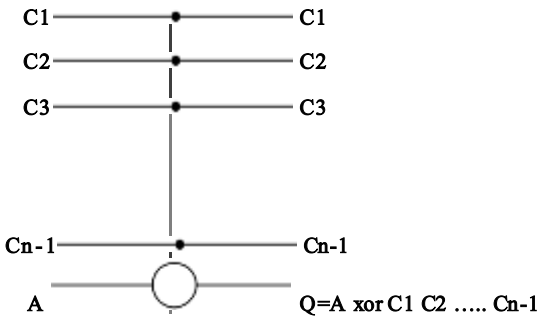


Figure 2. N-bit Controlled-Not Gate

Fig. 3, shows TR gate. Its new quantum implementation, which is represented in [5], is demonstrated in Fig. 4. The quantum cost of this gate reduces to 4 by this new quantum implementation. Earlier, the TR gate quantum cost was estimated as 6 in [6].

BJN gate and its quantum implementation are shown in Fig. 5, and Fig. 6, respectively. This gate is introduced in [7] and has the quantum cost of 5.

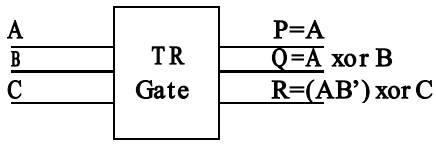


Figure 3. TR gate

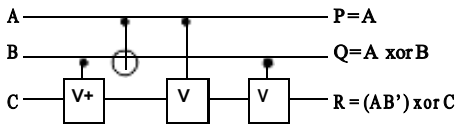
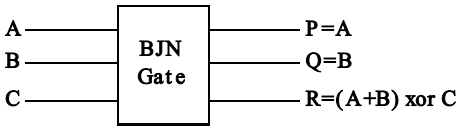


Figure 4. Quantum implementation of TR gate



DISCUSSION AND COMPARISON

As shown in Fig. 9, this circuit produces a total number of 15 garbage outputs, 10 constant inputs and 18 gates (consist of TR, BJN, NOT and N-bit Controlled NOT gate). The quantum cost of this reversible comparator is 38. In [5] 8 bit reversible comparator is represented. The quantum cost of this circuit is 135, which refers to 7 * quantum cost of 2-bit comparator + quantum cost of the reversible output circuit. The number of garbage outputs of this 8 bit comparator is 42 (7 * garbage outputs of 2 bit comparator = 7 × 6 = 42). If this comparator converts to 4 bit, the garbage output and quantum cost are equal to 63 and 18, respectively. The constant inputs number of equivalent 4 bit comparator is 13, too. If proposed circuit compares with this design, it can be seen that our comparator is optimized in number of constant inputs, garbage outputs, and quantum cost. Comparisons between proposed comparator and prior designs are reported in Table I.

Figure 5. BJN gate

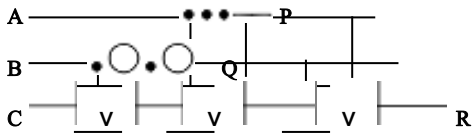


Figure 6. Quantum implementation of BJN gate

III. CLASSICAL IMPLEMENTATION OF COMPARATOR

In 4 bit logic comparator, two 4 bit numbers are compared with each other and the result shows that if one number is larger or less than other or if the two numbers are equal with each other. For example, assume A=A3 A2 A1 A0 and B=B3 B2 B1 B0, for comparing these two numbers, we use these functions:

$$(A = B) = x3\ x2\ x1\ x0. \quad (1)$$

$$(A > B) = A3\,B3' + x3\ A2\,B2' + x3\ x2\ A1\,B1' + x3\ x2\ x1\ A0\,B0'. \quad (2)$$

$$(A < B) = A3'\,B3 + x3\ A2'\,B2 + x3\ x2\ A1'\,B1 + x3\ x2\ x1\ A0'\,B0. \quad (3)$$

$$xi = Ai\,Bi + Ai'\,Bi' \text{ , for } i=0,1,2,3. \quad (4)$$

4 bit classical comparator is shown in Fig. 7,. In this figure, A=B line and $A>B$ line are produced based on (1) and (2) functions, respectively. A<B line is manufactured from A=B and A>B line.

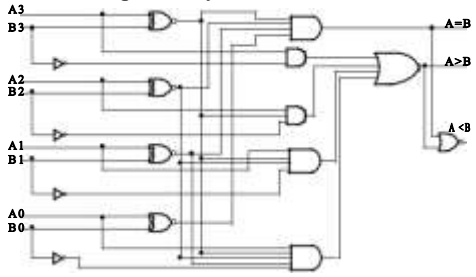


Figure 7. 4 bit classical comparator

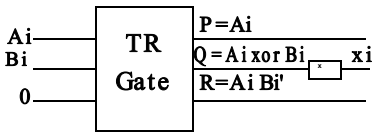
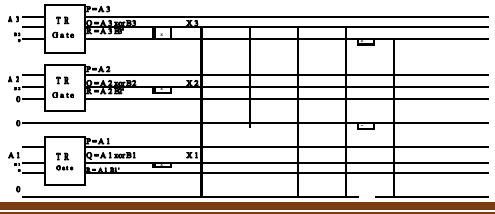


Figure 8. Producing xi and $Ai\,Bi'$



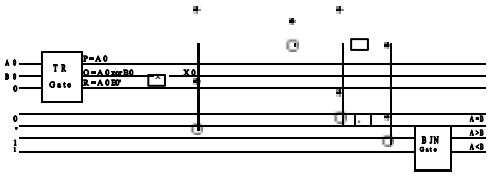


Figure 9. Proposed 4 bit reversible comparator

TABLE I. COMPARISON OF PROPOSED COMPARATOR WITH PRIOR WORKS

IV. DESIGN OF 4 BIT REVERSIBLE COMPARATOR

Our reversible comparator is based on last functions and construction. We use TR gate and NOT gate to produce *xi* and *Ai Bi'*. Producing these functions is shown in Fig. 8. Proposed reversible comparator is demonstrated in Fig. 9.

VI. CONCLUSION

In this paper, 4 bit reversible comparator based on reversible logic gates is designed. Compared with prior designs, proposed circuit is optimized in number of constant inputs, number of garbage outputs and, quantum cost. This reversible circuit is useful for nanotechnology, quantum computing and low power design.

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