



Five Level Cascaded H-Bridge Multilevel Inverter Using Pulse width Modulation

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Abstract The multilevel inverter utilization has been increased since the last decade. These new type of inverters are suitable in various high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. This paper presents an asymmetrical five level cascaded H-bridge multilevel inverter, using multicarrier pulse width modulation technique. And also comparison is made between multicarrier pulse width modulation and the embedded matlab function. The Simulation results are presented to prove that THD is reduced with the multicarrier modulation. This topology also reduces the number of switches and also the cost. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality.

2 Introduction

1. Demand for high-voltage, high power converters capable of producing high-quality waveforms while utilizing low voltage devices and reduced switching frequencies has led to the multilevel inverter development with regard to semiconductor power switch voltage

limits. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. The most attractive features of multilevel inverters are as follows:-

- 1) They can generate output voltages with extremely low distortion and lower dv/dt .
- 2) They draw input current with very low distortion.
- 3) They generate smaller common mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
- 4) They can operate with a lower switching frequency.
- 6.
7. The multilevel inverter has been implemented in various applications ranging from medium to high-power levels, such as motor drives, power conditioning devices, also conventional or renewable energy generation and distribution. The different multilevel inverter structures are cascaded H-bridge, diode clamped and flying capacitor multilevel



inverter [4]. Among the three topologies, the cascaded multilevel inverter has the potential to be the most reliable and achieve the best fault tolerance owing to its modularity, a feature that enables the inverter to continue operating at lower power levels after cell failure. Modularity also permits the cascaded multilevel inverter to be stacked easily for high power and high-voltage applications. The cascaded multilevel inverter typically comprises several identical single phase H-bridge cells cascaded in series at its output side. This configuration is commonly referred to as a cascaded H-bridge, which can be classified as symmetrical if the dc bus voltages are equal in all the series power

3. Brief Literature Survey

Divya Subramanian, Rebiya Rasheed [1] In this paper, a five level cascaded H-bridge multilevel with multicarrier pulse width modulation and embedded matlab function, is presented. The simulation results show that the total harmonic distortion is low for multicarrier modulation method. The total harmonic distortion can be further reduced by using filter circuit. This circuit also reduces the number of switches and sources.

Dinko Vukadinovi, Ljubomir Kuli, Mateo Basi [2] This paper presents an operation analysis of a single-phase half bridge inverter with ultra-fast IGBTs (insulated gate bipolar transistors) and freewheeling diodes. Theoretical and experimental prerequisites for an analysis of voltage distortion effects caused by the dead time are made. This is one of the trends of modern research in the field of industrial electronics.

M. Kavitha1, A. Arunkumar [3] In this paper mainly focused on the design and implementation of Papers presented in ICIREST-2018Conference can be accessed from <https://edupediapublications.org/journals/index.php/IJR/issue/archive>

new topology in a single phase five level cascaded H-bridge multilevel inverter by using only a five switches and two DC power source. The main objective of this paper is to increase number of levels with a low number of switches and sources at the output without adding any complexity to the power circuit.

Zhong Du, Leon M. Tolber, John N. Chiasson and Burak ozpineci [4] A method is presented showing that a cascade multilevel inverter can be implemented using only a single DC power source and capacitors. A standard cascade multilevel inverter requires n DC sources for $2n+1$ levels. Without requiring transformers, the scheme proposed here allows the use of a single DC power source (e.g., a battery or a fuel cell stack) with the remaining $n-1$ DC sources being capacitors.

P. Vinod Kumar, Ch. Santosh Kumar and K. Ramesh Reddy [5] This paper deals with Single Phase Five level Inverter using Multi Carrier Based Pulse width modulation Technique. The voltage quality of conventional two level inverter is poor due the presence of harmonics and hence produces power loss which reduces the efficiency of the system. The multilevel inverter is used to improve the voltage quality by reducing the harmonics, as the number of voltage levels of multilevel inverter is increased the harmonics are reduced and hence losses are minimized significantly. The simulation of single phase cascaded five level multilevel is done using Multicarrier PWM technique and compared with stepped wave.

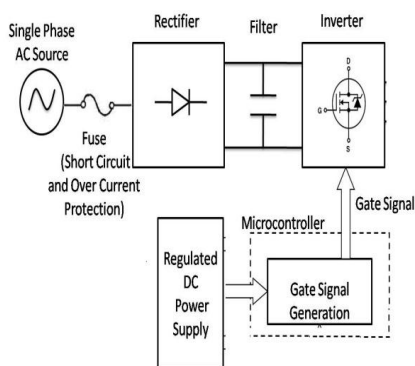
4 Research and Objective



The primary objectives of this project can be summarized as follows

- 1] To Stimulate a of Five Level Cascaded H-Bridge Multilevel Inverter
- 2] Hardware Implementantion of Five Level Cascade H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique.
- 3]This Analysis is Done to Compare Simulation of Single Phase Five Level Inverter Using Matlab Software With Hardware Model of Single Phase Five Level Inverter

5 Block Diagram



6

Hardware Requirements

Inverter, Rectifier, diode, capacitor, semiconductor, capacitor voltage source, power supply, switches, microcontroller

7 Specifications Preferred

A Signal is supplied from three or single phase grid. It consists of a diode rectifier, DC link filter and an inverter. The rectifier converts supply AC voltage into DC voltage. The DC voltage is filtered by a capacitor in the DC link. The inverter converts the DC to an variable voltage, The rectifier section of an block, called the front end, is responsible for generating current harmonics into the power supply system. Therefore, to reduce the total harmonic distortion (THD) of phase current it is necessary to add additional capacitors.

8 Conclusion

In the Present Work , performance of cascaded five level inverter using hybrid pulse width modulation technique has been analyzed. The topology used in this technique reduces the number of power switches and switching losses. In the Cascaded H-bridge multilevel inverter is popular in the multilevel inverter family. Out of various PWM techniques level gives a good harmonic performance. The modified PWM technique has also been developed to reduce switching losses. Also, the proposed method can reduce the number of required power switches compared to the cascaded multilevel inverter. From the FFT analysis we get minimum THD of 256.93% and the fundamental frequency 7.567Hz shows



performance of the cascaded hybrid five level inverter.

The simulation results show that this hybrid five level inverter topology can be applied for high power applications. Thus the proposed method will reduce the cost, and also used only 6 switches, harmonic reduction and the heat losses.

References

- [1] Zhong Du, Student Member, *IEEE*, Leon M. Tolbert, Member, *IEEE*, M. J. Hossain, Member, *IEEE*, "A Cascade Multilevel Inverter Using a Single DC Source", IEEE-0-7803-9547-6/06/\$20.00 ©2006 IEEE.
- [2] M. Kavitha¹, A. Arunkumar², N. Gokulnath³, S. Arun, "New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources," *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)* ISSN: 2278-1676 Volume 2, Issue 6 (Sep-Oct. 2012)
- [3] Divya Subramanian, Rebiya Rasheed on "Five Level Cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique" *International Journal of Engineering and Innovative Technology (IJEIT)* Volume 3, Issue 1, July 2013
- [4] P. Vinod Kumar, Ch. Santosh Kumar and K. Ramesh Reddy "Single Phase Cascaded Multilevel Inverter Using Multicarrier Pwm Technique" *ARPN Journal of Engineering and Applied Sciences* ©2006-2013 Asian Research Publishing Network (ARPN)
- [5] Dinko Vukadinovic, Ljubomir Kulilic, and Mateo Basic "A Half Bridge Inverter with Ultra-Fast IGBT Module – Modeling and Experimentation," *ELECTRONICS*, VOL. 13, NO. 2, DECEMBER 2009
- [6] V.Srimaheswaran, R.Uthirasamy, "Cascaded Multilevel Inverter for PV Cell Application Using PIC Microcontroller," *International Journal of Innovative Technology and Exploring Engineering*, vol. 2, no. 3, pp.19-24, February 2013
- [7] C.Venugopal, S.Mathew, "A Single Source Five Level Inverter with Reduced Number of Switches," *International Journal of Advanced Research in Electrical Electronics and Instrumentation Engineering*, vol.4, no. 5, May 2015
- [8] A.Nabae, I.Takahashi, H.Akagi, "A new neutral-point clamped PWM inverter," *Industry Applications, IEEE Transactions*, vol.IA-17, no 5, pp.518-523, Sept. 1981.