



## **Simulation Study of the Three-Phase Flying Capacitor Inverters: Modulation Strategies and Applications**

Sanjeevani Gondane  
Student of MTech

Tulsiramji Gaikwad Patil College of Engineering and  
Technology  
Mohagaon, Wardha Road, Nagpur, Maharashtra  
Email: [sanjeevanigondane@gmail.com](mailto:sanjeevanigondane@gmail.com)

Pratik Ghutke

AP, Electrical Engineering Department  
Tulsiramji Gaikwad Patil College of Engineering and  
Technology  
Mohagaon, Wardha Road, Nagpur, Maharashtra  
Email: [pratik.electrical@tgpacet.com](mailto:pratik.electrical@tgpacet.com)

### **ABSTRACT**

This paper is a simulation study of modulation strategies in three-phase flying capacitor inverters in MATLAB simulink. The flying capacitor multilevel converter is a recently developed converter topology assuring a flexible control and modular design. However, the flying capacitor multilevel converter requires a balanced DC voltage distribution. This can be realized by using a special control leading to natural balancing or by measuring the voltages and selecting the appropriate switching state. Under investigation those strategies that solve the capacitor voltage balancing problem, Carrier based phase-shift PWM method with APOD, IPD, POD are presented and corresponding voltage harmonic distortion values are analyzed for 3 level and 5 level Flying capacitor multilevel inverters. A general mathematical model for an N-level inverter is used for circuit operation analysis and a review of power system applications of flying capacitor multilevel inverters are presented.

**Keywords:** Flying Capacitor multilevel converters (FCMLC), MATLAB simulink model, Phase-shift PWM method.

### **1. INTRODUCTION**

Increasing demand for industrial power converters and some of interesting advantages of multilevel inverters such as low distortion in output voltage with relatively low switching frequency, low harmonic and electromagnetic interference (EMI), attracted researchers' attentions. Upto now, several topologies of multilevel inverters are represented. The main applicable topologies are Diode Clamped Inverter (DCI), Flying Capacitor Inverter (FCI) and Cascade Multilevel Inverter (CMI). In order to achieve this higher power rating, the voltage and current capabilities of the devices used in the converter need to be increased. Current insulated gate bipolar transistor (IGBT) technology extends upto 6.5 kV 900 A per switching device.

Meynard and Foch introduced a flying-capacitor-based inverter in 1992. The flying capacitor inverter has many attractive properties for medium voltage applications, including in particular the advantage of transformerless operation, and the ability to naturally maintain the cell capacitor voltages at their target operating levels [1]. This property is called natural balancing, and allows in principle the construction of such inverters with a large number of voltage levels. The three cell implementation of this circuit is shown in Figure 1, uses a series connection of "cells" comprising a flying capacitor and its associated complementary switch pair, and produces a switched.

The proposed model for study of the carrier-based PWM method in three-phase flying capacitor inverters is based on inverter switching function rather than actual circuit configuration. This model will be used for harmonic analysis of the output voltage of the inverter for different PWM strategies. The analyzed PWM strategies are those which allow the voltage balancing of flying capacitors. Section II gives basic of Flying capacitor for 3 level and 5 level with mathematical model, Section III gives modulation strategies and simulation model Section IV simulation and analysis and lastly Section V presented various power system applications and Section VI conclusions are drawn.

### **2. FLYING CAPACITOR MULTILEVEL INVERTER**

The power switches are Operation of Flying capacitor Multilevel inverters operated as complementary pairs (SL1 and SL1', etc.), and intermediate voltage levels are realized by routing the load current through paths that include the clamping- or cell-capacitor flying-capacitor multilevel inverter used for synthesizing approximated sinusoidal load voltages using staircase angle commutation control. The basic operation is described and a mathematical model is used to investigate all switching permutations.



**A) Basic Circuit Operation**

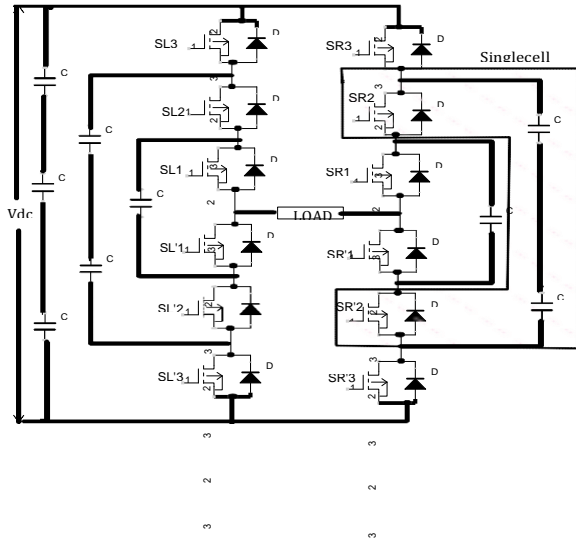


Figure.1. Schematic of FCMLI. (Cells connected in series)

The flying-capacitor inverter can be constructed to give an unlimited number of voltage levels, but for practical designs they are normally limited to seven levels. The number of possible voltage levels is related to the number of power switching devices connected in series in a ch inverter leg. The circuit topology's inverter legs is in the form of a series of connected cells nested inwardly toward the load from the dc-link. Each cell, shown highlighted in Figure 1, has a capacitor and two power switches each comprising a transistor with an anti-parallel diode and operated in a complementary manner. In an N-cell inverter, each limb has 2N switches and applies N+1 distinct dc voltage levels from zero to  $V_{dc}$  across the load. The single-phase inverter full-bridge can also apply negative voltage levels across the load and so an N-cell inverter has 2N+1 distinct voltage levels. In a balanced inverter, the floating cell-capacitor average voltages are kept at multiples of the  $V_{dc}/N$ . The capacitor associated with the complementary switch pair nearest the load terminal will have the lowest voltage ( $V_{dc}/N$ ), while the highest voltage ( $(N-1)V_{dc}/N$ ) capacitor is associated with switches connected to  $V_{dc}$ . The voltage contribution of each half-

limb will depend on the number of switches in conduction in its upper portion. Therefore with switches in conduction, the m<sup>th</sup> voltage level is applied at the load terminal with respect to zero. The full load voltage is the difference between the left and right half-limb voltage levels. This voltage can be expressed as

$$V_{load} = \frac{V_{dc}}{N} \times \left( \sum_{n=1}^N S_{Ln} - \sum_{n=1}^N S_{Rn} \right) \quad \dots (1)$$

where  $S_{Ln}$  and  $S_{Rn}$  ( $n=1, 2, \dots, N$ ) represent the left and right half-limb cell switch states, respectively, and logic '1' represents the upper switch in conduction and the lower switch in its blocking state.

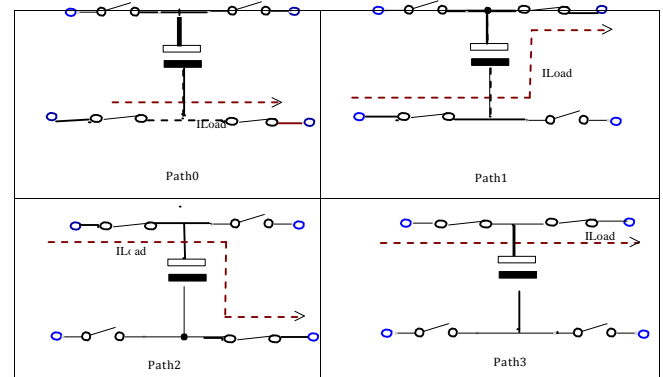


Figure 2: Cell-Capacitor Current Paths

**B) Capacitor Voltage Balancing**

One of the main reasons for using the multilevel flying-capacitor inverter is to operate at voltages higher than the individual power switch blocking capability. Safe operation entails keeping the cell-capacitor voltage differences within a restricted voltage band and so the capacitor voltages are balanced. The flying-capacitor inverter can operate within its inherent capacitor voltage balancing, so long as the control utilizes all the modes of charging and discharging at an intermediary voltage level. Figure 2 shows all the possible current paths for one cell-capacitor.

The paths 0 and 3, and the paths 1 and 2 form complementary pairs where their correct usage can ensure capacitor voltage balancing and power loss sharing. In the steady state, paths 1 and 2 used over consecutive cycles will balance the capacitor voltage and device



**International Journal of Research**  
*eISSN: 2348-6848 & pISSN: 2348-795X Vol-5 Special Issue-13*  
**International Conference on Innovation and Research in  
Engineering, Science & Technology**  
Held on 23<sup>rd</sup> & 24<sup>th</sup> February 2018, Organized by Tulsiramji Gaikwad  
Patil College of Engineering & Technology, Nagpur,  
441108, Maharashtra, India.



elosses, as long as the operating period coincides with the same angular position in the cycle. This will lead to one change in the charge on the capacitor, since the current integrals for each path would be equal and of opposite polarity. In the case of paths 0 and 3, their complementary usage must entail angular periods where the current is of equal and opposite polarity, thus ensuring the losses in each power device are the same.

*C) Circuit Mathematical Model*



The fundamental operation and characteristics of the flying-capacitor inverter can offer a great deal of flexibility in terms of operating modes compared to conventional two-level bridges. Complexity increases dramatically as the number of levels increases, and this makes it difficult to analyze the circuit operation. Therefore, a simple mathematical model is developed which can assist circuit analysis under different switch states. The mathematical equations for the inverter are constructed by expressing the rate of change of cell capacitor voltage, the output load voltage and current for all valid switching states. The equations are in a generalized form applicable to any N-cell inverter and the power switch states are included separately. The matrix form of the model for a generalized inverter half-bridge (chopper) with an R-L load, shown in Figure 3, is given below:

$$\frac{d[V]}{dt} = -[C] \times [A]^T \times [S] \times i_o \quad \dots (2)$$

$$V_{cn} = [C] \times [A] \times [V] \quad \dots (3)$$

$$\frac{di_o}{dt} = \frac{1}{L} (V_o - R i_o) \quad \dots (4)$$

where,

$$V = \begin{bmatrix} v_{c_n} \\ v_{c_{n-1}} \\ \dots \\ v_{c_2} \\ v_{c_1} \end{bmatrix} \quad S = \begin{bmatrix} S_n \\ S_{n-1} \\ \dots \\ S_2 \\ S_1 \end{bmatrix}$$

$$A = \begin{bmatrix} 1 & -1 & 0 & 0 & \dots \\ 0 & 1 & -1 & \dots & 0 \\ 0 & 0 & \dots & -1 & 0 \\ 0 & \dots & 0 & 1 & -1 \\ \dots & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{1}{C_n} & -1 & 0 & 0 & \dots \\ 0 & \frac{1}{C_{n-1}} & 0 & \dots & 0 \\ 0 & 0 & \dots & \frac{1}{C_2} & 0 \\ 0 & 0 & 0 & \frac{1}{C_1} & 0 \\ \dots & 0 & 0 & 0 & \frac{1}{C_1} \end{bmatrix}$$

is the mode switch state vector where 1 indicates the high-side switch conducting and 0 the low-side switch conducting for each cell complementary pair. Equation (4) represents the load characteristic and so is modified to represent other types of load.

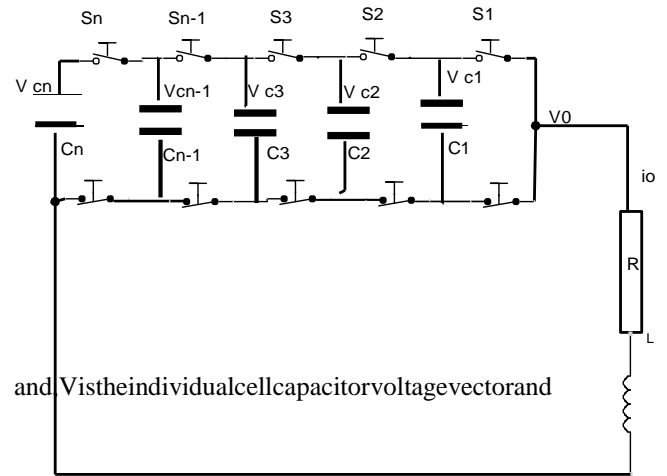


Fig.3 Inverter leg of flying capacitor multilevel inverter.

The above matrix relationships governing the flying-capacitor inverter can be incorporated within a simple fixed time-stepping procedure to calculate the load voltage  $v_o$  and current  $i_o$  with a particular switch state operated over a specific time period. By combining different switch states operated over different time periods any switching sequence pattern can be simulated efficiently. This feature is very useful for analyzing the inverter's operation when synthesizing a sinusoid using a fixed control switching sequence. For example in a three-cell, single-phase inverter the A and C matrices are as follows:

$$A = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 2/C_c & -1 \\ 0 & 0 & 1/C_c \end{bmatrix}$$

where  $C_c$  is the basic cell capacitance. By solving equations (1), (2) and (3) by iteration



**International Journal of Research**  
*eISSN: 2348-6848 & pISSN: 2348-795X Vol-5 Special Issue-13*  
**International Conference on Innovation and Research in  
Engineering, Science & Technology**  
Held on 23<sup>rd</sup> & 24<sup>th</sup> February 2018, Organized by Tulsiramji Gaikwad  
Patil College of Engineering & Technology, Nagpur,  
441108, Maharashtra, India.



,the complete output load waveform scan be found for a given switching mode as defined by S.

The capacitor voltage can be controlled in two ways. Either the capacitor voltage and current direction are measured and an appropriate switch state is chosen to



correct the capacitor voltage or a natural balancing scheme is used. Natural balancing scheme (which maintains the steady state stability of the capacitor voltages by using equal duty cycles for every pair of complementary switches. This can be done by using a special pulse width modulation (PWM) scheme.) is discussed in section III.

*i. Measuring capacitor voltage and current and choosing*

*switch state:*

This method requires measuring all the voltages of the capacitor buses and the direction of the phase current. When the sign of the error of the capacitor voltages and the direction of the current is known, an appropriate switch state for the desired output voltage can be assigned. This way the output voltage can be chosen at every instant, while always being sure the errors of the capacitor voltages are corrected.

independent capacitors clamping the device voltage to one capacitor

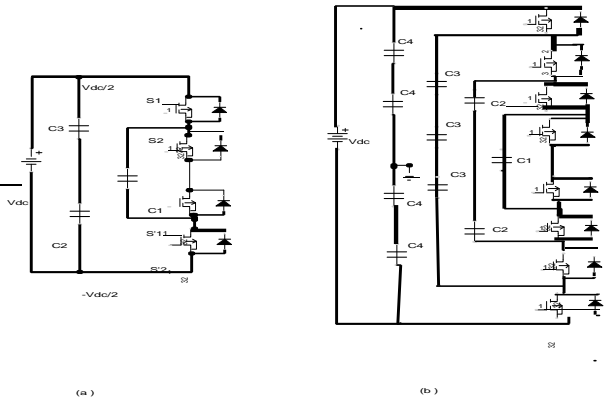


Fig.4 Phase Leg of (a) Three level FCMLI (b) Five Level FCMLI

TABLE I SWITCHING TABLE

unbalance			Switch state (positive current)		
C1	C2	C3	$-V_{dc}/4$	0	$+V_{dc}/4$
-	-	-	1000	1100	1110
-	-	+	1000,00 01	1100,10 01	1101
-	+	-	1000,00 10	1010,00 11	1110,10 11
-	+	+	1000,00 01	1001,01 10	1011
+	-	-	0100	1100,01 10	1110,01 11
+	-	+	0100,00 01	1100,01 01	1101,01 11
+	+	-	0010	0110,00 11	1110,01 11
+	+	+	0001	0011	0111

Table I is a table with the switching states for a positive current, there is no choice when the desired output voltage  $V_{an}$  is  $\pm V_{dc}/2$ , so this is not in the table. For every possibility of deviation of the capacitor voltages (+ or -), a switch state can be determined. Here 1000 means  $S_1$  is on and  $S_2, S_3, S_4$  are off. A similar table is available for a negative current.

**3. SIMULATION MODEL AND MODULATION TECHNIQUES**

voltage level. The inverter in Fig. 3(a) provides a three-level output across a and n, i.e.  $V_{an} = V_{dc}/2, 0, -V_{dc}/2$ . For voltage level  $V_{dc}/2$  switches  $S_1$  and  $S_2$  need to be turned on; for  $-V_{dc}/2$  switches  $S'_1$  and  $S'_2$  and for the 0 level, either pair  $(S_1, S'_1)$  or  $(S_2, S'_2)$  need to be turned on. Clamping capacitor  $C_1$  is charged when  $S_1$  and  $S'_1$  are turned on, and is discharged when  $S_2$  and  $S'_2$  are returned on. The charge of  $C_1$  can be balanced by proper selection of the 0-level switch combination. Fig. 5 shows MATLAB simulink model for 3 level FCMLI.

In Fig. 4(b) shows a phase-leg of a 5 level flying capacitor multilevel converter. In this circuit, independent capacitors clamp the device voltage to one capacitor voltage level. This converter topology has more flexibility than other multilevel converter topologies like the diode-clamped converter. Switches  $S_1, S_2, S_3$  and  $S_4$  are complementary with the corresponding switches  $S'_1, S'_2, S'_3, S'_4$ .

*A) Flying capacitor multilevel inverter operation:*

Fig. 3(a) illustrates the fundamental building block of a phase-leg 3-level capacitor-clamped inverter. The circuit has been called the flying capacitor inverter with



$S_3$  and  $S_4$ . The voltages of the capacitor banks are assumed to be at the nominal level at steady state. In Fig. 4b, each capacitor symbol assigns for the same voltage value. So the first capacitor bank ( $C_1$ ) has a voltage of  $V_{dc}/4$ , the second ( $2 \times C_2$ ) has a voltage of  $V_{dc}/2$ , the third ( $3 \times C_3$ ) has a voltage of  $3V_{dc}/4$  and the fourth is the DC-bus and has a voltage  $V_{dc}$ . The voltage of the five-

level phase-leg 'a' output with respect to the neutral point  $n$ ,  $V_{an}$ , can be synthesized by the following switch combinations. Here, the mentioned switches are on, the complementary are off.

1.  $V_{an} = V_{dc}/2$ : turn on all upper switches,  $S_1, S_2, S_3$  and  $S_4$ .
2.  $V_{an} = V_{dc}/4$ : one of the upper switches is turned off and its complementary is turned on. When for example  $S_2$  is turned on,  $V_{an} = V_{dc}/4$  because of the following



calculation:  $V_{dc}/2$  (of upper  $C_4$ 's)  $- 3V_{dc}/4$  (of  $C_3$ 's)  $+ V_{dc}/2$  (of  $C_2$ 's). This way series connection of capacitors is made to create the desired output.

3.  $V_{an} = 0V$ : now two upper switches are returned off and their complementary switches are returned on. A similar calculation as above can be made.
4.  $V_{an} = -V_{dc}/4$ : in this case, there is only one of the upper switch on.
5.  $V_{an} = -V_{dc}/2$ : turn on all lower switches,  $S^1_1, S^1_2, S^1_3$  and  $S^1_4$ .

The voltage over the capacitors changes as current flows through the capacitors. By choosing an appropriate switch state for a desired output voltage according to the current direction, it is possible to control the voltage over the capacitors.

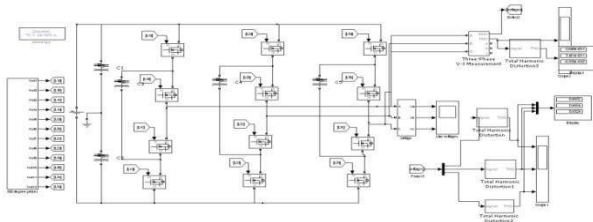


Fig. 5. MATLAB Simulink model for 3 Level FCMLI

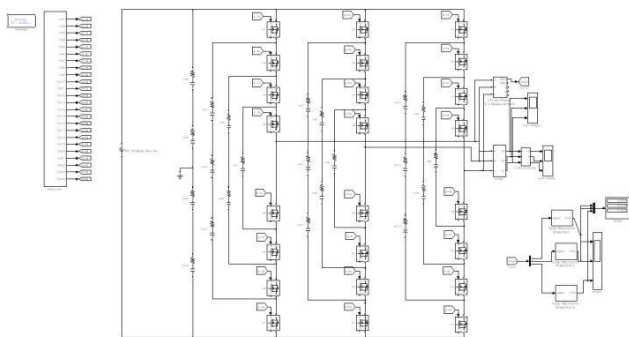


Fig. 6. MATLAB Simulink Model for 5 Level FCMLI

**B) PWM Methods for voltage balancing for flying capacitor:**

Natural balancing of a flying capacitor multilevel converter is a technique which maintains the steady state stability of the capacitor voltages by using equal duty cycles for every pair of complementary switches. This can be done by using a special pulse width modulation (PWM) scheme. In this scheme, every pair of switches has a carrier signal

carriers, the switch state of the corresponding switch pair is defined. When the reference signal is above the carrier, the upper switch is on and when below, the lower switch is on.

Controlling mechanisms for multilevel voltage source inverter can be classified into PWM and stepped techniques. PWM scheme consists of closed loop and open loop modulations. Sinusoidal PWM, SVM and sigma-delta modulation are three main control schemes of open loop modulation. Figure 7 shows the classification of modulation strategies for MLIs.

In this paper we consider carrier based pulse width

modulation which has a 90 degree phase change, also called phase shift carrier PWM (PSCPWM). When a reference signal, normally the desired output voltage, is compared with the





modulation(CBPWM).CBPWMhasitselfthreebranchesnamely:In-PhaseDisposition(IPD),AlternativePhaseOppositeDisposition(APOD)andPhaseOppositeDisposition(POD).Although,SVMdirectlycontrolsline-to-linevoltagesoftheinverter,allofCBPWMsubtechniquescontrol eachphaselegofinverterseparately.

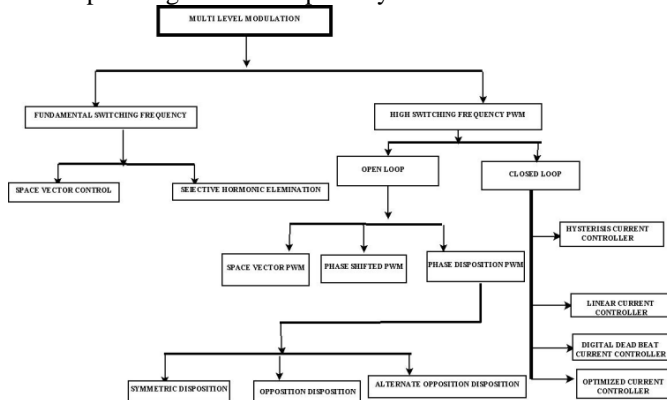


Figure.7.ClassificationofmodulationstrategiesforMLIs

Inthiscaseforthenlevel flyingcapacitorthen-1 carriersignalsarephaseshiftedby $T_p/(n-1)$ .Fig.8presents the carriersignals,modulatorsignalandconnection functionsforfivelevelcapacitorflyinginverterforoneleg.Inthiscasetherearefourcarriersignals:

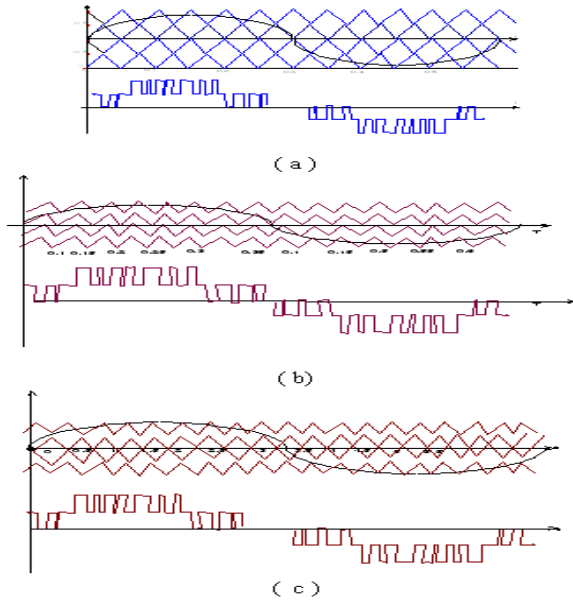


Fig.8. Different Modulations sub-techniques and relative inverter output voltage waveform: (a) APD, (b) IPD, (c) POD

Space vector PWM waveform has some advantages such as ease of digital control and switching waveform optimization. From Fig. 9, SVM identifies each switching state as a point in complex ( $\alpha, \beta$ ) space. A reference phasor rotating in the ( $\alpha, \beta$ ) plane at the fundamental frequency is sampled with in each switching period, and the three nearest vectors are selected. Duty cycle of each vector can be calculated by the time average principle:

$$T_1 U_1 + T_2 U_2 + T_3 U_3 = T_s U^*$$

$$T_1 + T_2 + T_3 = T_s$$

where  $T_1, T_2$  and  $T_3$  are duty cycles of  $U_1, U_2$  and  $U_3$ , respectively and  $T_s$  is the switching period. In multilevel inverters, more than one switching state is available for medium vectors. For instance, the space vector of  $A$  in Fig. 4 has four different switching states which are  $[-E, -2E, -2E], [0, -E, -E], [E, 0, 0]$ , and  $[2E, E, E]$ .

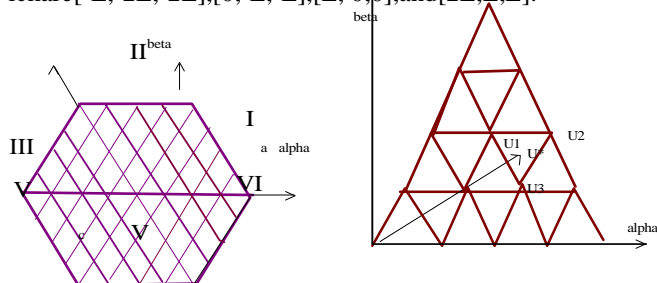


Fig.9 Space Vector Pulsewidth Modulation Scheme.

#### 4. SIMULATION RESULTS

The CBPWM (IPD, APOD, POD), methods presented above are analyzed with respect to their harmonic content and total harmonic distortion factor (THD) for 3 level and 5 level FCMLI. Ba

sef frequency  $= \omega_B = 2\pi f_1 = 2 \times 3.14 \times 50 = 314 \frac{rad}{sec}$ .  
 Carrier frequency  $= f_{cr} = 1000 \text{ hz}$ .

Table III FCMLC (5L) Component Specifications

Number of mains switches	36
Device ON resistance	0.01 $\Omega$
Device OFF resistance	1.0E6 $\Omega$
Forward voltage drop	0v
Forward breakover Voltage	0.2KV
Reverse withstand Voltage	0.2KV
Snubber resistance	500 $\Omega$

Output waveform of three level inverter and harmonic spectrums shown in Fig 10 to 13.

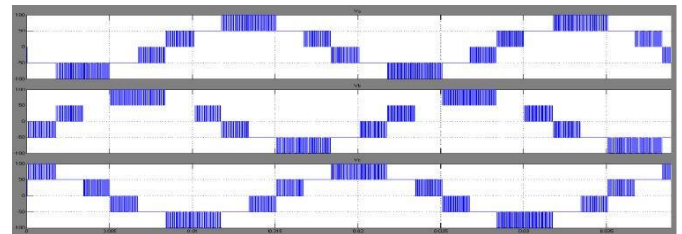


Fig. 10. Output voltage waveform for 3-Level FCMLI

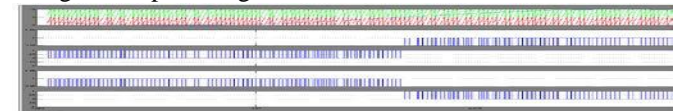


Fig. 11. Carrier signals ( $u_D$ ) and triggering pulses for 3-Level MLI

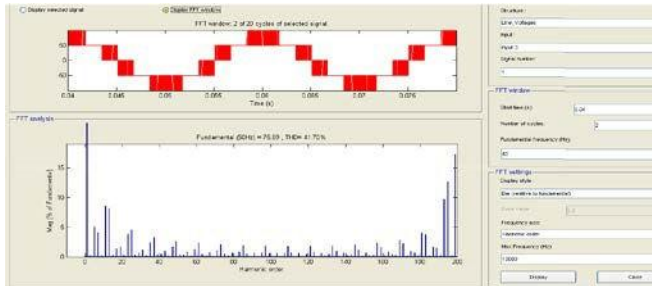


Fig. 12 Phase voltage and fourier components for three level lying capacitor inverter with phaseshifted carriers signals. (A POD)

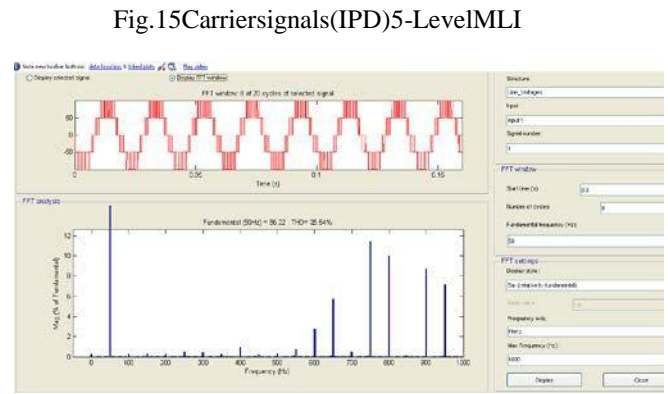


Fig. 15 Carriers signals (IPD) 5-Level MLI

Fig. 16 Phase voltage and fourier components for three level lying capacitor inverter with phaseshifted carriers signals. (P ID).

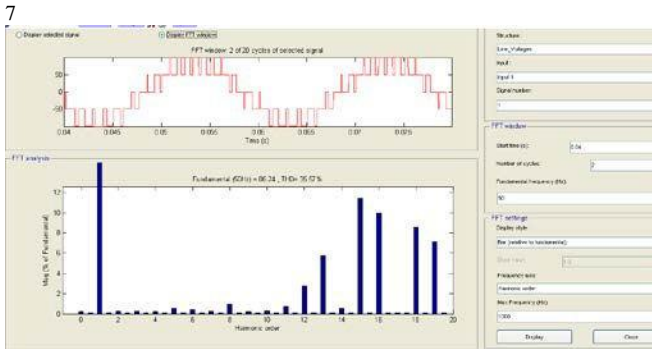


Fig. 13 Phase voltage and fourier components for three level lying capacitor inverter with phaseshifted carriers signals. (P ID)

TABLE II % THD OF THREE LEVEL WITH IPD AND AOPD

Three Level FC MLI	IPD Modulation % THD of output Voltage			AOPD Modulation % THD of output Voltage		
	Ph - A	Ph - B	Ph - C	Ph - A	Ph - B	Ph - C
ma=1, fm=50 Hz fcr=1000 hz	35.6%	36.94%	34.23%	39.4%	41.6%	40.2%
ma=0.8, fm=50 Hz fcr=1000 hz	35.9%	38.43%	37.35%	41.1%	43.01%	40.59%

Output waveform of five level inverter and harmonic spectrum shown in Fig 14 to 16.

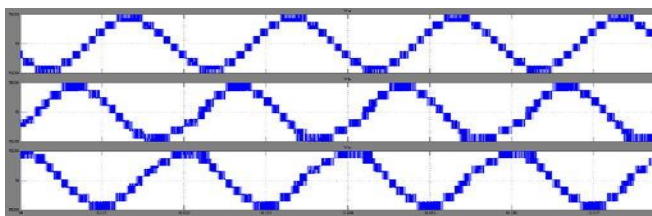


Fig. 14. Output voltage wave form for 5-Level FC MLI

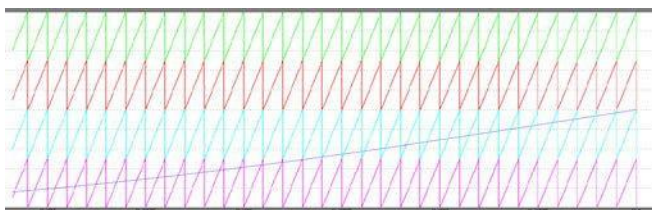


Table II gives the % THD values of three level FC MLI with IPD and AOPD modulation. In summary, the IPD modulation produces a better harmonic profile than the AOPD modulation. And Table III summarizes the % THD values for three level FC MLI and five level FC MLI with IPD modulation. Fig 17 shows graph of % THD values of three level and five level FC MLI with respect to carrier frequencies.

TABLE III % THD OF

THREE LEVEL AND FIVE LEVEL FC MLI WITH IPD



**International Journal of Research**  
*eISSN: 2348-6848 & pISSN: 2348-795X Vol-5 Special Issue-13*  
**International Conference on Innovation and Research in  
Engineering, Science & Technology**  
Held on 23<sup>rd</sup> & 24<sup>th</sup> February 2018, Organized by Tulsiramji Gaikwad  
Patil College of Engineering & Technology, Nagpur,  
441108, Maharashtra, India.



IPD Modulati on	ThreeLevelFCMLI			FiveLevelFCMLI		
	Ph -A	Ph- B	Ph- C	Ph- A	Ph- B	Ph- C
ma=0.8 Fm =50 Hz Fcr	35. 9	38.4 3	37.3 5	23.1 2	26.2 5	25.4 2

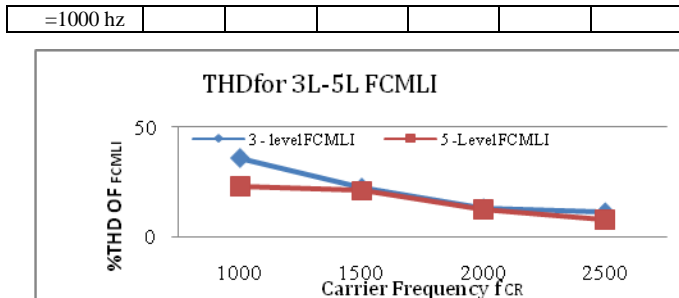


Fig 17 %THD values of three level and five level FCMLIs with respective carrier frequencies

The THD are calculated for the first 200 harmonics. The modulation index is 1 and switching frequency is 1000 Hz. Three-phase reference signals are obtained by adding the offset voltage  $V_{off}$  to the original phase voltages to obtain an equivalent reference voltage. The offset voltage is defined as:

$$V_{off} = - \frac{[\max[(V_a^* + V_b^*) + V_c^*] + \max[(V_a^* + V_b^*) + V_c^*]]}{2}$$

The THD values obtained by simulation using the presented model of the inverter for three and five level flying capacitor inverter for phase shifted PWM method (PSPWM). From Fig. 12, 13 and 16 we can see that the harmonic carrier bands appear at frequencies  $f_h$  given by:

$$f_h = k(n-1)f_p$$

where 'k' is an integer ( $k=1,2,3,\dots$ ),  $f_p$  is the frequency of carrier signal and  $n$  is the number of inverter levels.

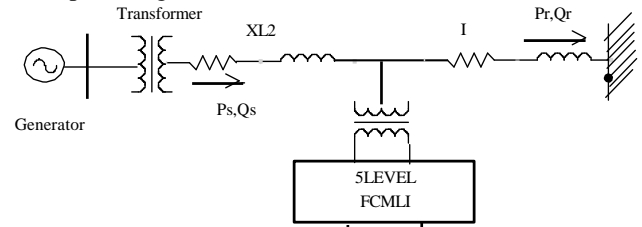
## 5. APPLICATIONS OF FCMLI IN MULTILEVEL INVERTERS IN POWER SYSTEMS

The main applications of FCMLI are FACTS (static synchronous compensator (STATCOM), static synchronous series compensator, unified power flow controller (UPFC)) and Power Line conditioner or Active Power Filters (APF).

At present, there are three benchmark multilevel inverter topologies: i) diode-clamped multilevel inverter (DCMLI), ii) cascade H-bridge inverter, and iii) flying capacitor multilevel inverter (FCMLI). DCMLI suffers from the limitations of dc-link voltage unbalance, indirect clamping of the inner devices and multiple blocking voltages of the clamping diodes. H-bridge cascade inverter has limitations such as, the requirement to

back-to-back arrangement (e.g., in UPFC) is not possible because a short-circuit will be introduced when two back-to-back converters are not switching synchronously. In this inverter, the switching modulation needs to be optimized for high performance applications due to a limited combination of switching patterns. Moreover, for reactive power exchange, the over-pulsation at twice the output frequency occurring with the dc-link of each H-bridge inverter necessitates over-sizing of the link capacitors.

The FCMLI attempts to address some of the limitations imposed by the above-mentioned inverters. With the increase in the number of output voltage levels, the number of dc-link



flange number of inverter to decrease the harmonics and complex dc-voltage regulation loop. It needs separated dc sources for real power conversion and thus has some limited applications. Connecting separated dc sources between two converters in



Fig.18(a) STATCOM compensated single machine infinite bus system.

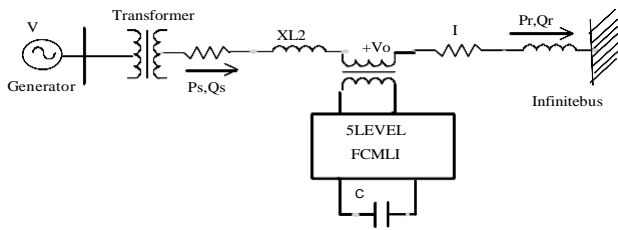


Fig.18.(b) SSSC compensated single machine infinite bus system. capacitors in cascade and in DCMLI increase and hence their control becomes more complex especially in transient conditions. However, the dc-capacitor control loop in FCMLI is as simple as in the conventional two-level inverter and is independent of the number of output voltage levels.

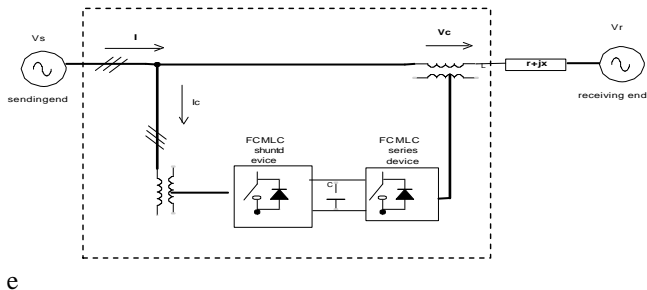


Fig. 18(c) System configuration of a UPFC based on FCMLI

The typical structure of FCMLI makes it possible to split the voltage constraints and to distribute them on several switches of smaller ratings in series. This also makes it possible to obtain a significant improvement of the output

waveform to increase the apparent frequency of this wave, allowing a significant reduction of the filtering requirements. The use of capacitors for the voltage clamping instead of diodes as in DCMLI, permits several switch combinations for a particular voltage level generation, which may be used for preferential charging and discharging of capacitors.

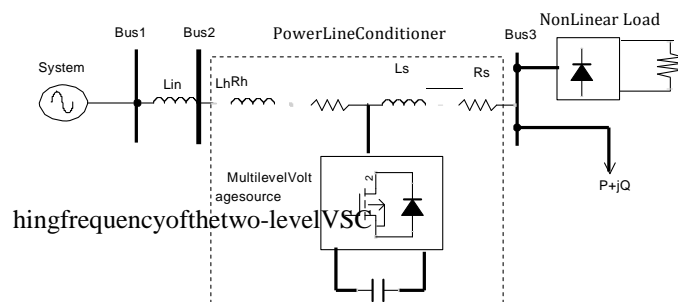
The control strategy uses an inherent feature of FCMLI and is sufficient to have balanced dc voltages of the flying capacitors if the voltage of the main dc bus capacitor is balanced. Therefore, a complex dc capacitor voltage control loop is not required in an FCMLI-based FACTS controllers and independent control of the output voltage and flying capacitor voltages can be achieved. Even though the FCMLI offers various features, extensive research has not been reported on its potential FACTS applications. Fig. 18 shows single diagrams for FCMLI based (a) STATCOM (b) SSSC (c) UPFC.

It is probably due to some of its limitations such as requirements of a large number of capacitors and their efficient control. Some research has reported control schemes for balancing the flying capacitor voltages, which use PI controllers for each flying capacitor voltage balancing.

It is probably due to some of its limitations such as requirements of a large number of capacitors and their efficient control. Some research has reported control schemes for balancing the flying capacitor voltages, which use PI controllers for each flying capacitor voltage balancing.

In industrial or distribution system applications where voltage ranges from 4.16 to 13.8 kV, either large reactors or very high switching

frequency of the two-level VSC can be employed to meet system harmonic requirements. In the first case, since the reactors are in series with the load, intolerable voltage drop will be caused by the reactors. Very high switching frequency cannot be achieved due to the switching speed limit of high-voltage high-power devices. To solve the problems stated above, a flying-capacitor multilevel VSC is employed. Phase-shifted sinusoidal PWM (SPWM) switching concept is adopted and applied to control the switches of this converter. The ability of balancing





converter

1

c

2

Fig.19 single line diagram for FCMLI based power line conditioner.

unbalanced load is possible in addition to the reactive compensation and harmonic suppression capabilities. Due to the switching scheme, the resultant output voltage of this multilevel VSC has a very high equivalent switching frequency, even if the switching frequency of the individual switches is not very high. As a consequence, the values of the reactors are low. Thus Reactive Power Compensation, Harmonic Suppression, Balancing Unbalanced Load possible by using FCMLI. The Schematic for power line conditioner by using FCMLI shown in Fig 19.

## 6. CONCLUSION

In this paper, flying capacitor multilevel inverter FCMLI with IPD and APOD modulation schemes are studied in detail. The theoretical analysis, design, and Simulink implementation of flying-capacitor multilevel converters of 3<sup>rd</sup> and 5<sup>th</sup> level are represented. These simulation results along with FFT analysis for line voltage are presented and compared among various levels of FC converters and modulation schemes for different modulation index  $m_a$ , carrier frequency  $f_c$  and frequency modulation index  $m_f$ . Applications of FCMLI in power systems are summarized.

## REFERENCES

- [1] Jih-Sheng Lai, and Fang Zheng Peng  
 'Multilevel Converters-A New Breed of Power Converters'





**International Journal of Research**  
*eISSN: 2348-6848 & pISSN: 2348-795X Vol-5 Special Issue-13*  
**International Conference on Innovation and Research in  
Engineering, Science & Technology**  
Held on 23<sup>rd</sup> & 24<sup>th</sup> February 2018, Organized by Tulsiramji Gaikwad  
Patil College of Engineering & Technology, Nagpur,  
441108, Maharashtra, India.



*IEEE TRANSACTIONS ON  
INDUSTRY APPLICATIONS, VOL.32,NO.3,  
MAY,JUNE1996*

- [2] APandey,BSingh,BNSingh,ACHandra,KAl-Haddad,DPKothari 'AReviewofMultilevelPowerConverters' *IE(I)JournalEL*, August28,2003.
- [3] JoséRodríguez,Jih-ShengLai,FangZhengPeng 'MultilevelInverters:ASurveyofTopologies,Controls,andApplications' *IEEE TRANSACTIONSONINDUSTRIALELECTRONICS*, VOL.49,NO.4, AUGUST2002
- [4] Xiao-PingZhang,ChristianRehtanz,BikashPal 'FlexibleACTransmissionSystems:ModellingandControl' book.
- [5] AnshumanShukla,ArindamGhosh,AvinashJoshi 'StaticShuntandSeriesCompensationsofanSMIBSystemUsingFlyingCapacitorMultilevelInverter' *IEEE TRANSACTIONSONPOWERDELIVERY*, VOL.20,NO.4,OCTOBER2005
- [6] YiqiaoLiang,C.O.Nwankpa 'APower-LineConditionerBasedonFlying-CapacitorMultilevelVoltage-SourceConverterwithPhase-ShiftSPWM' *IEEE TRANSACTIONSONINDUSTRYAPPLICATIONS*, VOL.36,NO.4,JULY/AUGUST2000
- [7] L.XuandV.G.Agelidis 'FlyingcapacitormultilevelPWMconverterbasedUPFC' *IEEProceeding-ElectricPowerApplications* Vol.149,N0.4July2002.
- [8] Ir.StevenThielemans 'FlyingcapacitormultilevelconvertersforACmachines' *SystemsandAutomationjournal*, GhentUniversity (UGent),Gent,Belgium.
- [9] JalalAmini, 'FlyingCapacitorMultilevelInverterBasedShuntActivePowerFilterwithTriflingSusceptibilitytoDivisionalVoltagesDeregulation' *IEEE TRANSACTIONSONINDUSTRYAPPLICATIONS* AUGUST2011.