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Design And Control Of A Hybrid Multilevel Converter With Floating Dc-Links To Improve The Outputs

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***Abstract*— This paper proposes the design and control of a hybrid multilevel converter with floating DC-links to improve the outputs. An hybrid multilevel inverter designed by the series combination of a main three-level NPC converter and auxiliary floating H-Bridges (NPC-HBs) has been presented in. In this inverter, the NPC is used to supply the active power and the HBs is used as a series active filters,improving the voltage waveform quality by only handling reactive power. In this way the hybrid inverter reduces the need of bulky and expensive LCL passive filters and making it an attractive alternative for large power applications. Validations of results are provided in matlab simulink.**

***Keywords*—Cascaded multilevel inverter; Neutral point clamped multilevel inverter(NPC); Selective harmonic elimination (SHE).**

I. INTRODUCTION

The converters are designed to obtain a quality output voltage or a current waveform with a minimum amount of ripple content. In high power and high voltage applications the conventional two level inverters have some limitations in operating at high frequency mainly due to switching losses and constraints of the power device ratings. Series and parallel combination of power switches in order to achieve the power handling voltages and currents. The conventional two level inverters produce THD levels around sixty percent even under normal operating conditions which are undesirable and cause more losses and other power quality problems too on the AC drives and utilities.

In recent years, a relatively new type of inverters, multilevel Voltage source inverters, has attracted many researchers' attention [1]. Multilevel inverters can reach high voltage and reduce harmonics by their own structures without transformers, a benefit that many contributors have been trying to appropriate for high-voltage, high-power applications[2].When this inverter is compared with two level inverter it has advantage of improved output waveforms due, to its higher number of levels in the output voltage waveform. Similarly, an increased number of voltage levels will result in a reduced input filter size for grid connected applications. The use of this inverter also allows the device switching frequency to be reduced for a given current distortion.

The multilevel inverters can be classified into three main types: the neutral point clamped (NPC) [3], the flying capacitors (FC) [4], [5] and the cascaded H-bridge (CHB) converters [6], [7]. The three level NPC bridge is the most widely used inverter for medium voltage AC motor drives and PWM active rectifiers [8], [9]. NPC inverters with more levels are also possible, even though there are significant problems in the balancing of their dc-link capacitor voltages [10], [11], unless recent modulation technics [12] or extra circuitry [13] are used. The CHB converter is normally implemented with large number of levels but it has disadvantage is that become costly, complicated and bulky because of input transformers with multiple rectifiers [7], [14], or multi-winding three-phase output transformers [16].Hence CHB is widely used only where active power transformation is not required such as in reactive power compensation, and where the converter can operate without the rectifier front-end. [17], [18].

In some recent years hybrid inverters become more popular because it integrate more than one topology in a single converter. Some of the authors have proposed hybrid topologies in which cascaded H-bridges fed by multilevel dc-links implemented with another converter [19]–[21]. In [22], an hybrid topologies based on the combination of an active NPC and a flying capacitor cell has been proposed to implement a five level converter. An hybrid converter formed by the series connection of a main three-level NPC converter and auxiliary floating H-Bridges (NPC-HBs) has been presented in [23]–[25]. This topology has NPC which is used

to supply the active power and another converter the HBs operate as series active filters for improving the voltage waveform quality by only handling reactive power. Hence this topology reduces the need for bulky and expensive LCL passive filters and making it an attractive alternative for large power applications [24], [25].In this work, the control strategy for the NPC-HBs hybrid converter, previously introduced in [26], is experimentally verified. This includes: low frequency synchronous modulation of the NPC and the generation of the HBs voltage references for dc-link voltage control.

II. NPC-SHE TOPOLOGY

A.MODELLING AND SIMULATION DESIGN OF NPC/SHE TOPOLOGY

In the hybrid converter, the main purpose of NPC inverter is to provide active power flow.The high-power medium voltage NPC due to their lower losses and higher voltage blocking capability [23], [25], [27], imposing a restriction on the switching frequency. In this work, an NPC is considered operating at a low switching frequency (of 250Hz) where in contrast, the H-bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. The NPC inverter is, modulated by using Selective Harmonic Elimination (SHE).This method has the advantage of very low switching frequency and hence low switching losses, while eliminating the low order harmonics. The output voltage of NPC converter is synthesized by using SHE modulation and thus the series HBs will be used only to supply reactive power, allowing for operation with floating capacitor DC-links.

Fig .1. Neutral Point Clamped 3 level multilevel inverter

NPC type Multilevel inverters plays vital role in the field of power electronics and being extensively used in various industrial and commercial applications because it possess low electromagnetic interference and the efficiency is considerably high. NPC Multilevel inverters have become more favoured over the years in electric high power application with the affirmation of less disturbances and the contingency to operate at lower switching frequencies than typical two-level inverters This multilevel inverter will also be compared with two-level inverter in simulations to investigate the advantages of using multilevel inverters. It is observed that NPC multilevel inverter produce only 22% and 32% voltage THD whereas the two-level inverter for the same test produces 115% voltage THD. For other simulation, while practising lower switching frequency, it is observed that when the two-level inverter develops 25W.Switching losses, the experimented multilevel inverters only produce 2.1W and 2.2W switching losses.

B.SIMULINK MODEL OF 3 LEVEL NPC

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B.SIMULINK MODEL OF NPC 3 LEVEL INVERTER

The simulation model is shown in the figure below. The implementation of 3 phase Neutral Point Clamped Multilevel inverter in MATLAB software is done. In this model MOSFET is used as switching device, opto-isolator is used to give gate pulse to the thyristor. The output voltage is taken between line to line and phase to phase. The total THD counts up to 32%. The output current and voltage waveform is shown in the figure. A common neutral point is taken outside and grounded

Fig.2.Simulink model for 3 level NPC

The simulation model is shown in the figure above. The implementation of 3 phase Neutral Point Clamped Multilevel inverter in MATLAB software is done. In this model MOSFET is used as switching device, opto-isolator is used to give gate pulse to the thyristor. The output voltage is taken

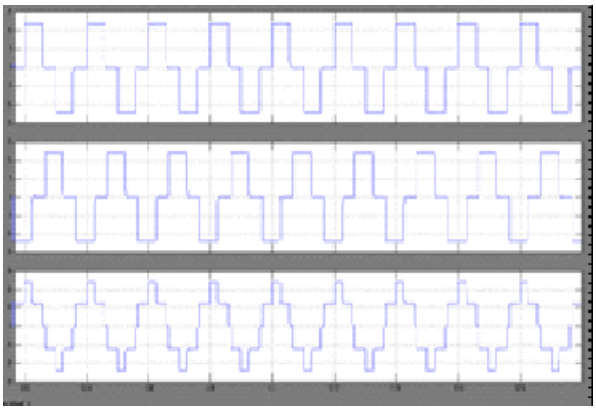


Fig.3. Waveform of output phase voltage and line voltage

between line to line and phase to phase. The total THD counts up to 32%. The output current and voltage waveform is shown in the figure. A common neutral point is taken outside and grounded

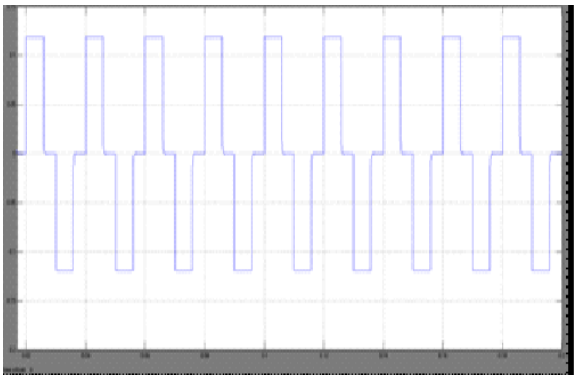


Fig.4. Waveform of output current

The NPC type multilevel inverter consists of three sections. Control circuit, Driven circuit and Power circuit. The control circuit is the controller of the inverter consisting of a PIC microcontroller which generates the appropriate gate pulses for the MOSFET. The control circuit gets an AC source supply for its functioning. The gate pulses which switch the MOSFET on or off are coded in MPLAB software. The Driven circuit is the driver of the inverter consisting of opto isolator TLP250 op-amp to provide amplified signal to MOSFET and regulator to give the required regulated supply. The third section is the Power circuit consisting of power MOSFET, diodes and load. The gate pulses is given to the gate terminal of the respective MOSFET through the opto isolator. The switching of the respective MOSFET is done by using PWM technique. The programming for PWM is stored in the PIC microcontroller. We get the stepped output in the steps of 0. –Vdc, +Vdc. By shifting the phase by 120o and 240o we can get 3 phase stepped output. The levels indicate the operation or ON time of a particular MOSFET or sometimes two.

C.SLECTIVE HARMONIC ELIMINATION METHOD

The popular selective harmonic elimination method is also called fundamental switching frequency method which is based on the harmonic elimination theory. The multilevel fundamental switching scheme inherently provides the opportunity to eliminate certain lower order harmonics by varying the times at which certain switches are turned ON and turned OFF. A staircase output voltage waveform is generated by switching ON and OFF the switching devices in the multilevel inverters once during one fundamental cycle. This diminishes the switching losses in the devices. In this method, each switch is turned ON and turned OFF once in a switching cycle and switching angles are usually chosen based on specific harmonic elimination or minimization of THD in the output voltage. Two ways to eliminate lower order harmonics are;

i) By increasing the switching frequency of SPWM and SVM in case of two level inverters or in multicarrier based phase shift modulation for multilevel inverters.

ii) By computing the switching angles using SHE techniques.

The first method of eliminating low frequency harmonics is limited by the switching losses and the availability of the voltage steps. SHE techniques comprises the mathematical modelling of output waveform and solving them for switching angles based on the amplitude of the fundamental wave of the

output voltage, the order and number of the eliminated harmonics.

Thus, the lower order harmonics are either eliminated or minimised while the higher order harmonics are filtered out in selective harmonic elimination method. Multilevel inverter can produce a quarter wave symmetric stepped voltage waveform synthesized from several DC voltages

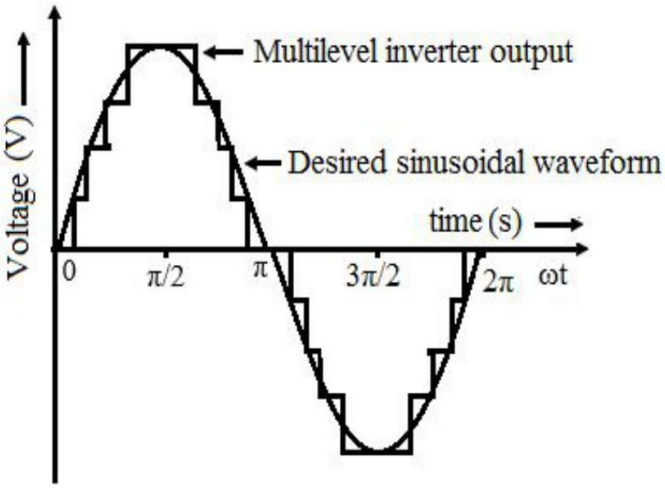


Fig.5. Stepped voltage waveform of multilevel inverter

By applying Fourier series analysis, the output voltage can be expressed as

$$V(\omega)=\frac{4}{n\pi}\sum_h[V1\cos(n\theta 1)+V2\cos(n\theta 2)+\ldots..+Vh\cos(n\theta h)]\sin(n\,\omega t)$$

where , n = 1, 3, 5…

'h' is the number of DC sources and V1, V2… Vh are the level of DC voltages. The switching angles must satisfy the condition $0< \theta 1< \theta 2 <.....< \theta_S < (\pi/2)$. However, if the switching angles do not satisfy the condition, this method no longer exists. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, upto h-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low frequency harmonics are chosen for elimination by properly selecting the triggering or switching angles and high frequency harmonic components can be readily removed by using additional filter circuits.

III.CASCADED H-BRIDGE INVERTER

Fig.6. Single-phase structure of a multilevel cascaded H-bridges inverter

A single-phase structure of an m-level cascaded inverter is illustrated in Figure.6.Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources.

The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$. For a stepped waveform such as the one depicted in Figure with s steps, the Fourier Transform for this waveform follows

$$V(\omega t)=\frac{4V_{dc}}{\pi}\sum_n\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right]\frac{\sin(n\omega t)}{n},\quad \text{where } n=1,3,5,7,\ldots$$

The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

The conducting angles, θ_1, θ_2, ..., θ_s, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency

$$H(n)=\frac{4}{\pi n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right], \quad \text{where } n=1,3,5,7,\ldots$$

harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated. Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure, or in delta. Peng has demonstrated a prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system

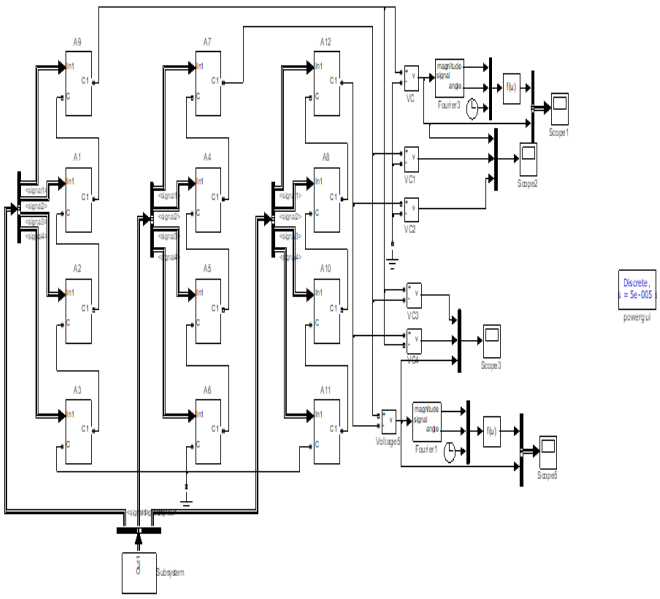


Fig.7. Simulink model for cascaded H-bridge

The simulation model is shown in the fig.7. for H-bridge The implementation of cascaded H-bridge Multilevel inverter in MATLAB software is done. In this model GTO with RC

Fig.9. Output waveform for the line voltage

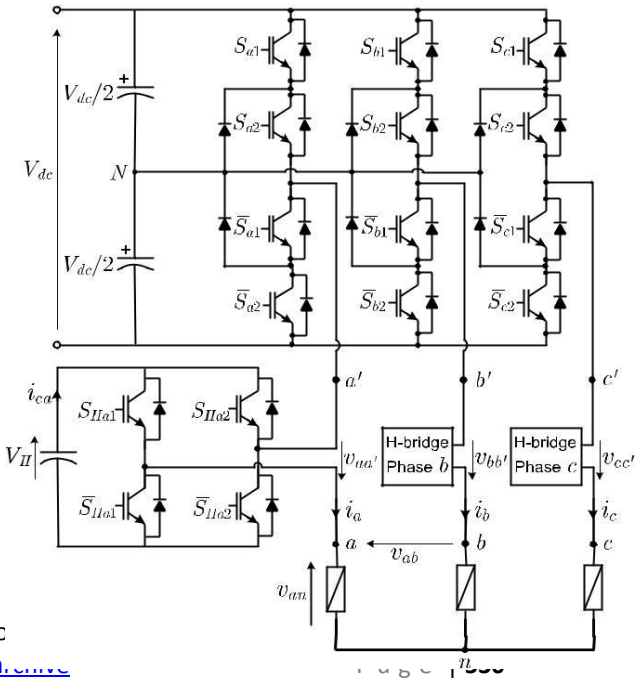
Fig.8. Output waveform for the phase voltage

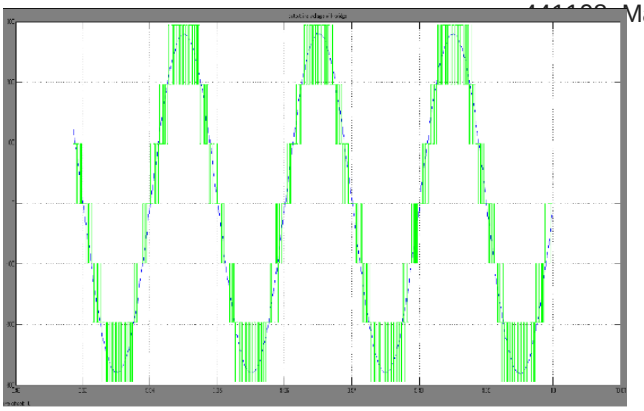
snubber circuit is used as switching device.For each phase four separate DC source is used.The output phase voltages and line voltages are measured on corresponding scopes.

IV HYBRID TOPOLOGY

A. Power Circuit

The proposed hybrid topology is made by a traditional three-phase, three-level NPC inverter, connected with a single phase H-bridge inverter in series with each output phase [23]–[25]. The power circuit is illustrated in Fig. ,with only the H-bridge of phase a shown in detail. To make sure as an inverter, the DC source for the NPC converter is provided by two series connected diode bridge rectifiers, connected in a twelve-pulse configuration. The H-bridge DC-links are not connected to an external DC power supply, and they consist only of floating capacitors kept at a constant voltage by the control strategy.
The implemented converter, shown in Fig., can be analyzed from two different points of view. The first interpretation is as a single hybrid multilevel inverter with a nine level phase voltage, obtained by the cascade connection of a three level NPC leg and an H-bridge per-phase. The second interpretation is as an NPC converter with a series active filter that compensates for the harmonic content produced by the low switching NPC stage





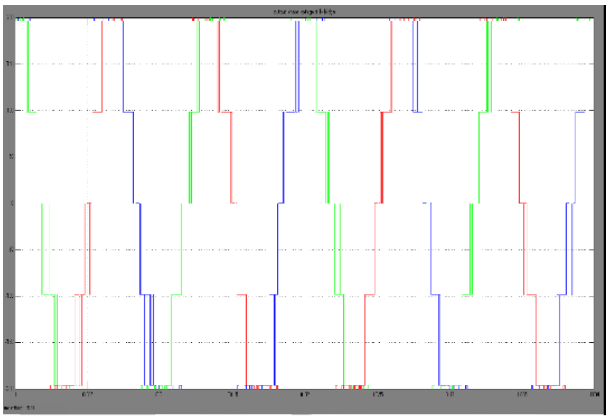


Fig. 10. Hybrid topology power circuit.

The connection of the series H-bridge results in more levels being added on the output voltage waveform of the converter v_{aN} . In particular, if the value of V_H is smaller than $V_{dc}/4$, no redundant switching states are created and the output voltage waveform of the converter will have the maximum number of levels (nine), generating similar waveforms to those achieved by cascade H-bridge inverters with unequal dc sources [1], [31].The increased number of output levels leads to a reduction in both the magnitude of voltage and the output voltage waveform and the harmonic content of the overall output voltage v_{aN}, enhancing the power quality of the hybrid converter. There is one solution to make V_H equal to a sixth of the NPC total dc-link voltage, i.e. $V_H = V_{dc}/6$, so that equally spaced output voltage levels would be created. we know that the NPC converter is modulated using the synchronous SHE method, the H-bridge should be modulated to compensate for the distortion created by the modulation of the NPC. This is done at a higher frequency using carrier based unipolar PWM. When deciding the value for the dc-link voltage of the H-bridges V_H , a sufficiently large value should be selected to obtain appropriate compensation of the remaining distortion, while at the same time the value of V_H should be kept as low as possible in order to minimize the additional switching losses.

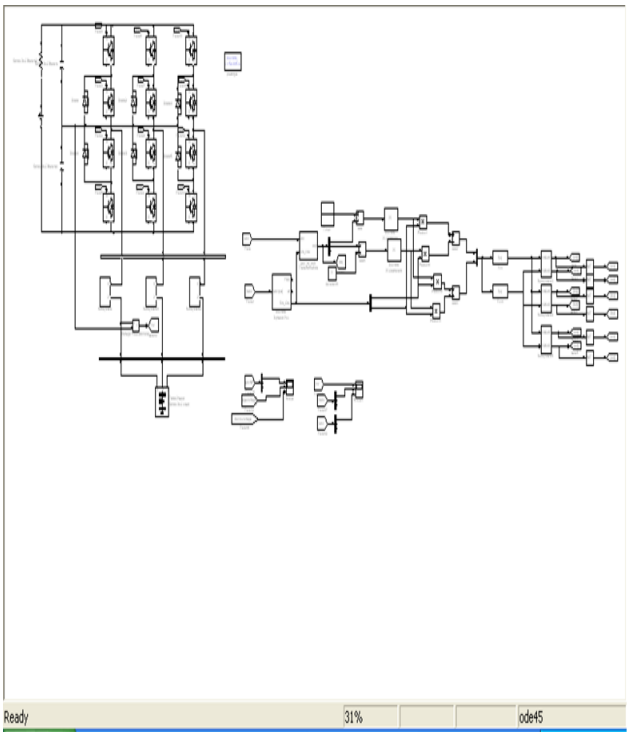


Fig.11. Simulink model for Hybrid topology

Figure 11 presents simulation results for the hybrid topology and control .It consists a combination of the 3 level NPC inverter and H-bridge inveter.The resulting waveform of this simulation model is shown in fig 12.

In comparison to the previous results, the full hybrid topology results are shown in Fig. 12.a) shows the three-level NPC output voltage, $v_{a0\ N}$, generated under the same conditions, while Fig. 12.b) shows the output voltage of the respective H-Bridge $v_{aa}0$ with the higher switching frequency compared with the NPC output. Some distortion can be created due to

the semiconductors drop, which will not be consider for higher voltage applications. The H-Bridge DC-link voltage is shown in Fig. 12.c), which is controlled to be the desired voltage of V_H = 0:167 V_{dc} .Also, it can be noted that in Fig.12. e) that 33 different voltage levels are applied to the load voltage, causing less distortion in the output inverter waveforms than in the NPC output waveforms of Fig. . This is seen clearly in the current waveform in Fig. 12.f), with a highly sinusoidal shape compared with the output current waveform without the H-Bridges harmonic compensation. is clear that current waveform improvement has been achieved with the hybrid inverter. Hence, comparing the results of Fig.3. with those of Fig.9., it is clear that current waveform improvement has been achieved with the hybrid inverter.

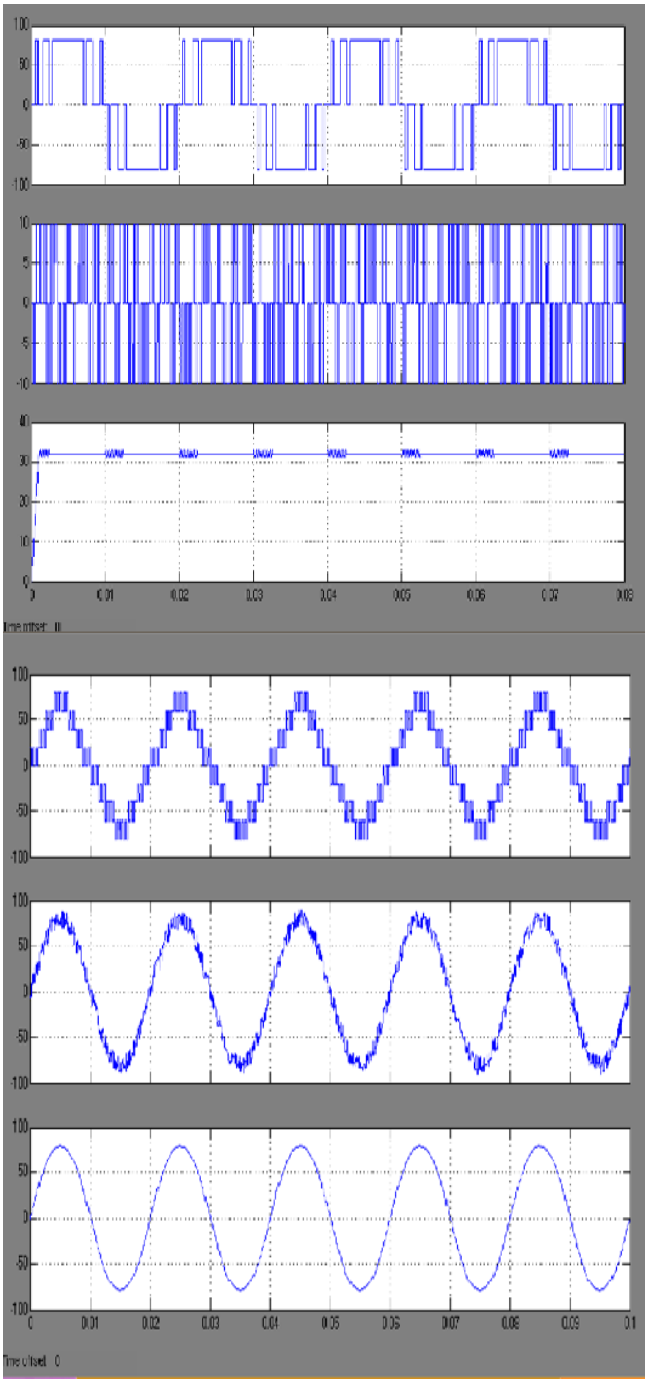


Fig.12-a) NPC output voltage b) H-bridge output voltage c)H-bridge dc-link voltage d) Inverter output voltage e) load output voltage f) output current

For this analysis, simulated data is used to overcome inaccuracies, caused by use of a low voltage prototype, in

particularly the effect of semiconductor drop. For the NPC converter, as expected, the spectrogram does not show the lower order harmonics. How-ever it does have more than 7% of the 17th and 19th harmonics and significant amplitude in higher order harmonics, resulting in a current THD of 12.9%. On the other hand, the operation. of the hybrid converter shows almost a complete elimination of these characteristic harmonics, resulting in a current THD of 2.4%.

Fig.12.show the controlled DC-link voltage of the H-bridge and the current waveform improvement for hybrid inverter.In comparison to previous results, the full bridge topology results are shown in fig above. Fig.12. a) shows the three level NPC output voltage Va'n, generated under yhe same condition, while fig.12. b) shows the output voltage of the respective H-Bridge.

V.CONCLUSION

This paper presents the Hybrid multilevel inverter consisting of 3 level NPC and H-bridge multilevel inverter. The H-bridge is added only as a series active filter it does not have any role in increasing power rating of the converter.The main purpose of this is to improve the power quality of the NPC bridge which have a relatively low switching frequency. By this method we got superior closed loop control. By using hybrid multilevel inverter the change in output voltage is considerably reduces and distortion in output waveform is reduces considerably and hence this method is superior.

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