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Solar Based Thirteen Level Inverter Towards Thd Reduction

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ABSTRACT

Multilevel inverter (MLI) is one of the most efficient power converters which are especially suited for high power applications with reduced harmonics. MLI not only achieves high output power and is also used in renewable energy sources such as photovoltaic, wind and fuel cells. Among various topologies of MLI, this paper mainly focuses on cascaded MLI with three unequal DC sources called asymmetric cascaded MLI which reduces the number of power switches.

In this paper we focus on sinusoidal (or) multicarrier pulse width modulation (SPWM) which improves the output voltage at lower modulation index for obtaining lower Total Harmonic Distortion (THD) level. The gating signal for the 13-level hybrid inverter using SPWM technique is generated using Field Programmable Gate Array (FPGA) processor.

The proposed modulation technique results in reduced percentage of THD, but lower order harmonics are not eliminated. So a new technique called Selective Harmonic Elimination (SHE) is also implemented in order to reduce the lower order harmonics. The optimum switching angles are determined for obtaining minimum THD.

INTRODUCTION

In recent years multilevel inverter plays an important role and attracts more attention in the conversion of medium power applications. It is simple in construction, better-quality in performance and produces lesser harmonics. Also it has lower switching losses, high dv/dt rating and reduced switching stresses and harmonics. The three commercial topologies of multilevel voltage source inverters are (i) the Neutral Point Clamped (NPC) or diode clamped multilevel inverter (DCMLI), (ii) flying capacitor multilevel inverter (FCMLI), and (iii) cascaded H-bridge (CHB) multilevel inverter. Unlike DCMLI and FCMLI the CMLI does not require voltage clamping diodes and voltage balancing capacitors.

This paper focuses particularly on cascaded hybrid multilevel inverter which requires independent DC sources *i.e.* for “n”

number of DC sources the number of levels obtained will be (2n + 1). In view of DC source, the CHB multilevel inverter is further divided into two topologies namely symmetric and asymmetric inverters. The values of all the voltage sources are equal in symmetric topology. In symmetric topology if the number of output voltage levels is increased, it results in rapid increase in number of switching devices. So in order to increase the number of output voltage levels with less number of switching devices the different value of DC sources are selected which is named as asymmetric topology. Among these two topologies, asymmetric cascaded MLI is explained in this paper and it requires three unequal DC sources to produce thirteen-level output. This new topology has been proposed to obtain 13-level output with minimum number of switches.

In addition to that the THD are reduced and specified harmonics are eliminated using selective harmonic elimination technique (SHE PWM). The problem of eliminating harmonics in switching converters has been the focus of research for many years. If the switching losses in an inverter are not a concern (i.e., switching on the order of a few kHz is acceptable), then the sine-triangle PWM method and its variants are very effective for controlling the inverter. This is because the generated harmonics are beyond the bandwidth of the system being actuated and therefore these harmonics do not dissipate power. On the other hand, for systems where high switching efficiency is of utmost importance, it is desirable to keep the switching frequency much lower. In this case, another approach is to choose the switching times (angles) such that a desired fundamental output is generated and specifically chosen harmonics of the fundamental are suppressed. This is referred to as harmonic elimination or programmed harmonic elimination as the switching angles are chosen (programmed) to eliminate specific harmonics.

Specifically, the harmonic elimination problem was formulated as a set of transcendental equations that must be solved to determine the times (angles) in an electrical cycle for turning the switches on and off in a full bridge inverter so as to produce a desired fundamental amplitude while eliminating, for example, the fifth and seventh harmonics. These transcendental equations are then solved using iterative numerical techniques to compute the switching angles. (See Here a method is presented that not only obtains these

solutions, but also another (different) set of the switching angles, and this other set of switching angles actually generates a smaller harmonic distortion due to the eleventh and thirteenth harmonics. The unipolar case is also considered (including the case where the fifth, seventh, eleventh, and thirteenth harmonics are eliminated) along with corroborative experimental results.

EXISTING SYSTEM

The basic architecture and switching of the converter switches are described. A laboratory prototype of the proposed architecture was implemented using MOSFETs and harmonic performance under different shading conditions was evaluated. It was found, that under shaded conditions, the 3rd harmonic content can increase and that it depends on the number of modules shaded and the loading condition.

The shading performance, losses and power utilization of the cascaded multi-level inverter are compared with that of a conventional Pulse Width Modulated (PWM) inverter architecture. The proposed inverter shows better immunity for shading than a PWM inverter. Furthermore, it was found that the switching losses of the proposed inverter are one 10th to one 20th of that of a PWM inverter. Additionally, by properly selecting the switches, it is also possible to reduce the conduction losses compared to that of a PWM inverter. Even though the power utilization is compromised at full isolation, the power utilization performance of the proposed inverter is superior under shading conditions, thus ideally suited for the selected application.

PROPOSED SYSTEM

A better voltage utilization and harmonics reduction, Multicarrier Phase Shift Pulse Width Modulation control technology is used.

The analysis of output voltage harmonics and the total power losses converging the switching power losses are carried out and compared with the cascaded neutral point clamped and conventional H-Bridge inverters. A new method to balance the system voltage in each source is developed and tested. For the verifications it is tested on three phase application systems.

From the results, the proposed inverter provides higher output quality with relatively less harmonics losses and THD as compared to the other conventional inverters.

CONCLUSION:

Multilevel inverter configuration based on a thirteen-level TCHB inverter

with multicarrier phase shifted PWM modulation technology, is analyzed and presented.

A new method hybrid cascaded multilevel inverter was developed and tested with balanced DC source for better voltage utilization. The output voltages of the proposed inverter were analyzed in various operating conditions.

The proposed inverter is found potential not only for medium-voltage drive application but also other applications like high voltage drives demanding higher output quality.

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