International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 12
April 2018

Delay-Dependent Stability Of Single-Loop Controlled Grid-Connected Inverters With Lcl Filters

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ABSTRACT

An *LCL*-filter draws much attention in grid-connected applications, but the design faces challenges. The *LCL* and controller parameters are interdependent and inter-restricted as the grid current quality and control stability rely on the parameters of them both.

In the past, researchers found that extra sensors or complex algorithms were required for the stability when the *LCL* parameters were designed independently. Consequently, the system cost and complexity were increased. Indeed, the *LCL*-filter with the delay-dependent single-loop current control can be stable if the *LCL* parameters are properly selected. Based on this thought, this study proposes to design the *LCL* parameters by considering their impact on the stability and dynamic of the inverter.

Extra sensors or complex algorithms are no longer required. Based on establishing the model of the single-loop inverter-side current controlled inverter, the criteria of *LCL* design are obtained in order to improve the stability and the rejections of low-order and switching current harmonics. Based on those design criteria, a step-by-step procedure is proposed. Selected results have been provided to demonstrate the effectiveness of the proposed design.

INTRODUCTION

A grid-connected inverter is playing an important role in improving the power quality and reliability of distributed power generations. Thus, the design of filter and controller parameters is of great importance. The less than container load (LCL)-filter is widely adopted. However, the LCL design meets challenges because the design of two inductors and one capacitor has to make a trade-off among many practical factors. Besides, the LCL-filter may cause the inverter unstable if the control with one current feedback is adopted. In the last decade, many researchers tried to fix the problems associated with the adoption of LCL-filter. In the view of some practical factors including the switching ripples, the resonance frequency and the reactive power absorbed by the capacitor, some basic LCL design principles. Then, some design approaches were proposed to minimize the filter energy, the size of filters and the power losses. The design helped to cut the filter cost; however, the capacitor voltage feedback with a lead-lag compensator was needed for stability.

EXISTING SYSTEM

This paper describes relationship between the time delay and stability of single-loop controlled grid-connected inverters with LCL filters. It is found that the time delay is a key factor that affects the system stability. The stable ranges of the time delay (the ranges of the time delay within which the system can be made stable) are deduced in the continuous s-domain as well as the discrete z-domain, applicable for any LCL parameters. To improve the stability of the single-loop control systems, time delay compensation methods are proposed. For ICF, a linear predictor based time delay reduction is used. A simple PI tuning method without simplification is proposed. To design the controller, the LCL filter is often simplified as an L filter.

PROPOSED SYSTEM

The LCL parameters by considering their impact on the stability and dynamic of the inverter. Extra sensors or complex algorithms are no longer required. Based on establishing the model of the single-loop inverter-side current controlled inverter, the criteria of LCL design are obtained in order to improve the stability and the rejections of low-order and switching current harmonics. Based on those design criteria, a step-by-step procedure is proposed. Selected results have been provided to demonstrate the effectiveness of the proposed design. Single-loop controlled LCL-filtered inverter Udc is the dc-link voltage, uinv is the inverter output voltage, iL1 and ig are the inverter-side current and grid current separately, iref is the current reference generated by the dc-link control, uc is the capacitor voltage and ug is the grid voltage.

Both ug and iL1 are used to generate the PWM reference um. The transfer function from uinv to iL1 is:

$$G_{u_{\text{inv}}}^{i_{L1}}(s) = \frac{L_2 C_1 s^2 + 1}{L_1 L_2 C_1 s^3 + (L_1 + L_2)s}$$

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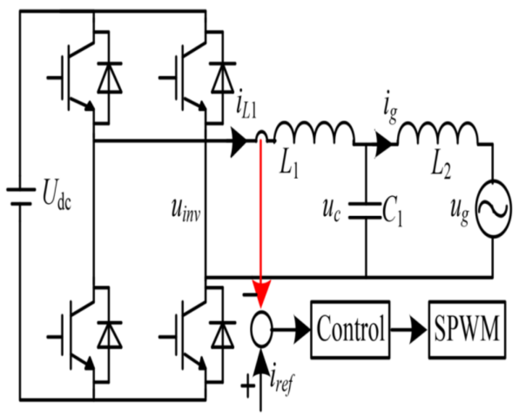
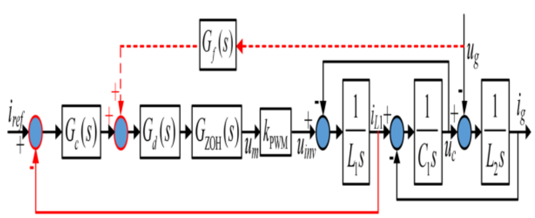
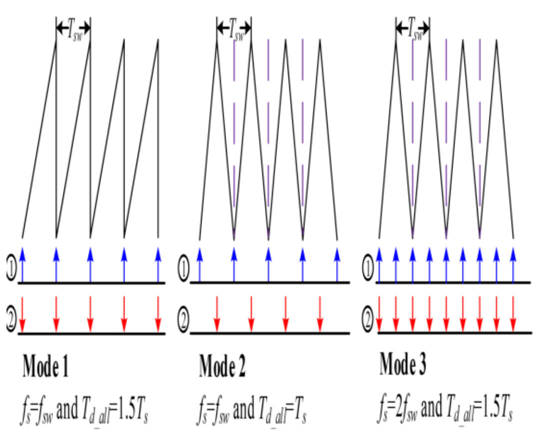


Fig:3.1 Descriptions of single-loop controlled LCL-filtered inverter.



Single inverter-side current feedback control



Typical sampling and PWM modes at the same switching frequency (①: sampling instant of iL1; ②: reloading instant of um)

The inverter-side current control, where *G*f(*s*) is the grid voltage feed-forward, *k*PWM denotes the PWM gain, and *G*c(*s*) is a proportional-integral (PI) or proportional-resonant (PR) controller. The total delay *G*d_all(*s*) includes the sampling and computation delay *G*d(*s*) and zero-order holds *G*ZOH(*s*)

$$G_{\mathrm{d\_all}}(s) = G_{\mathrm{ZOH}}(s)\cdot G_{\mathrm{d}}(s)$$
$$= \frac{1-e^{-sT_s}}{sT_s}\cdot e^{-sT_d}$$
$$\simeq e^{-s(T_s/2+T_d)} = e^{-sT_{\mathrm{d\_all}}}$$

Where *T*s is the control (sampling) period, *T*d is the delay time relying on the sampling and PWM mode, and *T*d_allis the total delay time. As depicted in Fig. 1*c*, in Mode 1, the sampling is located at the valley and the PWM is reloaded at the peak. The switching frequency *f*sw (1/*T*sw) equals the control frequency *f*s (1/ *T*s). Then, *T*d is *T*s, and *T*d_all is 1.5*T*s. In Mode 2, the carrier is symmetrical so that *T*d equals 0.5*T*s and *T*d_all equals *T*s. In Mode 3, *T*d_all is 1.5*T*s. However, unlike Mode 1, *f*s is 2*f*sw so that *T*d_all in Mode 3 is the shortest, i.e. 0.75*T*sw.

CONCLUSION

In the proposed design, because the filter and controller cooperate properly, the system achieves a high robustness, good steady-state performance and fast transient while extra high-precision sensors or complex algorithms for suppressing harmonics are avoided. This paper analyses and proposes the design of *LCL*-filter and controller aiming to improve the stability, dynamic and grid current harmonics rejection of the single-loop inverter-side current controlled inverter. This study reveals the relations among the *LCL*-filter, stability margin and rejections of grid current harmonics induced by the grid voltage distortion. It is found that the capacitance should be designed as small as possible to suppress the current harmonics caused by the grid voltage distortion, but the excessive reduction is unpractical. In the proposed design, because the filter and controller cooperate properly, the system achieves a high robustness, good steady-state performance and fast transient while extra high-precision sensors or complex algorithms for suppressing harmonics are avoided.

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