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Minimizing the Usage of Electrolytic Capacitors and Smoothening the Dc Bus Voltage Ripples By Using Eliminators to Improve Power Quality

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ABSTRACT- *In this paper the control strategies for elimination of DC bus voltage ripples are proposed and usage of electrolytic capacitors is minimized by pulse width modulation (PWM) based rectifying approach and continuous conduction mode(CCM). The control strategies could improve the performance of ripple eliminators. The voltage/current ripples has become a primary power quality issue for dc systems. In this paper, a single-phase Pulse width modulation-controlled rectifier is taken as an example to investigate how active control strategies can improve the power quality of dc systems, reduce voltage ripples, and, at the same time, reduce the usage of electrolytic capacitors. The concept of ripple eliminators recently proposed in the literature is further developed, and the ratio of capacitance reduction is analyzed. An advanced controller on the basis of the repetitive control is proposed for one possible implementation of ripple eliminators in the continuous current mode (CCM). By using the simulation results we can verify the effectiveness of the strategy with comparison to another ripple eliminator operated in the discontinuous current mode.*

Key words: Instantaneous diversion of ripple currents, CCM, DCM, ripple eliminators, voltage ripples, repetitive control, reliability, electrolytic capacitors

INTRODUCTION

Now a days, the end use devices require high quality, sensible power otherwise would result in the serious malfunction of the devices. The simplest way of eliminating DC ripples is to connect a capacitor bank in parallel with the output of the converter circuit. But these large electrolytic capacitors are costly, bulky and more over require continuous maintenance which results in the extra cost and time. The life time of the electrolytic capacitors are is also less. Hence in order to optimize the performance a novel DC compensation circuit is developed which would eliminate the ripples & improve the quality of supply.

The harmonic components in the voltages and the resulting ripple currents, ripple power has become a major power quality issue in DC systems. For systems powered by photovoltaic panels, batteries and fuel cells, large ripple currents and ripple voltages could considerably reduce the lifetime and long-term reliability of photovoltaic panels, batteries and fuel cells. During the charging mode of a battery, an external voltage with large ripples could lead to an immoderate chemical reaction. In order to reduce the ripple current and smooth the external voltage on batteries and fuel cells, bulky capacitors or ultracapacitors are often connected in parallel with them [11].

In principle, this power quality issue in DC systems stems from energy fluctuation, which can come from sources and/or loads of systems. Four main approaches have been developed in the literature to reduce or compensate energy fluctuation so that the voltage ripples can be reduced and the power quality in DC systems can be improved.

The analysis in these papers is based on the fact that decreased pulsating input power leads to decreased ripple power and capacitor volume on the DC bus, which can be achieved by controlling the input current.

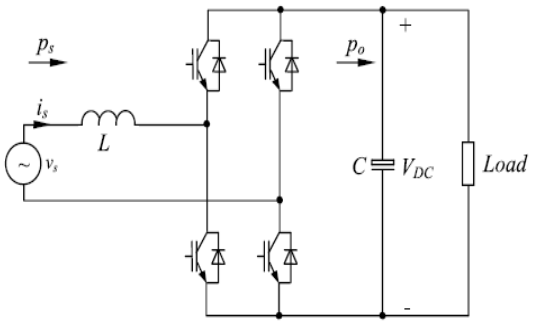

Fig 1: Single-phase H-bridge PWM-controlled rectifier.

The main focus of this paper is to investigate how advanced control strategies could improve the performance of shunt ripple eliminators for DC systems. The new contributions of this paper include 1) analyzing and revealing how active control strategies can help reduce voltage ripples and reduce total capacitance, 2) quantifying the level of capacitance reduction, which is independent from applications and topologies; 3) optimizing the

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controller for ripple eliminators in which only one instead of two repetitive controllers are now required without affecting the system performance;
4) By using the simulation results we can verifying the performance of the active control strategies.

ANALYSIS OF RIPPLE ENERGY AND RIPPLE VOLTAGE

In order to facilitate the analysis in this paper, a single-phase H-bridge PWM-controlled rectifier as shown in Figure 2 is used as an example, with all the components assumed to be ideal to simplify the analysis in the sequel.

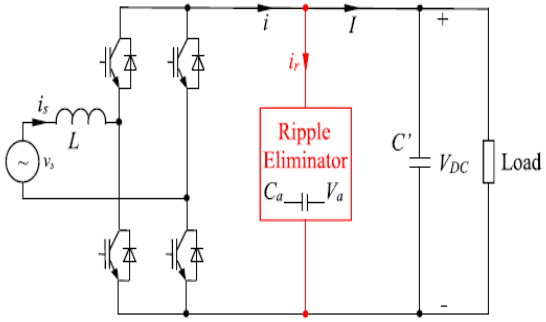

Fig 2: The concept of ripple eliminators

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If the input current of the rectifier is regulated to be sinusoidal as $i_s = \sqrt{2}I_s \sin(\omega t)$ and in phase with the input voltage $v_s = \sqrt{2}V_s \sin(\omega t)$, then the input power is

$$i_s = v_s i_s = V_s I_s - V_s I_s \cos(2\omega t) \qquad (1)$$

where Vs and Is are the RMS values of the input voltage and current, respectively, and ! is the angular line frequency. Note that the power drawn from the AC source consists of a constant VsIs and a second-order ripple component VsIs cos(2ωt).

In order to analyze the voltage ripples of the DC bus, the net change of the energy stored in the DC-bus capacitor over a charging period (i.e. a quarter cycle of the supply), called the ripple energy, can be calculated as [10]

$$E_r = \frac{V_s I_s}{\omega} \qquad (2)$$

As demonstrated in [10], the voltage ripple (peak-peak) on the capacitor C can be given as

$$\Delta V_{DC} \approx \frac{E_r}{C V_{DCO}} \qquad (3)$$

where VDC0 is the average value of the voltage VDC. It is clear that, when increasing the capacitor C, the DC-bus voltage ripple is decreased but this increases the weight, volume and cost of the system and decreases the reliability of the system, which should be avoided if possible.

RIPPLE ELIMINATORS AND THE LEVEL OF CAPACITANCE REDUCTION

In order to break the deadlock between minimizing the required capacitors and reducing voltage ripples, another design degree of freedom, called the ripple eliminator, can be introduced to replace the bulky DC-bus capacitor, as shown in Figure 3.

The basic idea is to introduce an auxiliary capacitor Ca in the ripple eliminator so that the ripples on the DC bus can be transferred onto Ca.

Since the ripple eliminator is operated to divert the ripple energy on the DC bus to the auxiliary capacitor, there is no need to use a large electrolytic capacitor on the DC bus and the ripple energy on the auxiliary capacitor should be the same as the DC-bus ripple energy in the ideal case. Applying (3) to the auxiliary capacitor, there is

$$C_a \approx \frac{E_r}{\Delta V_a V_{ao}} \qquad (4)$$

where ΔVa and Va0 are the peak-peak and average voltages of the auxiliary capacitor. Note that the ripple energy Er is determined by theDCbus and not affected by the added ripple eliminator. Note also that the auxiliary capacitor is designed to allow large voltage ripples. Assume the ripple voltage ratio of the auxiliary capacitor is

$$r_a = \frac{\Delta V_a}{V_{ao}} \qquad (5)$$

Then (4) can be re-written as

$$C_a \approx \frac{E_r}{r_a V^2_{ao}}$$

It is clear that for the same ripple ratio r_a, the capacitance is in inverse proportion to the square of the voltage across it, which means the auxiliary capacitance can be significantly reduced via increasing its operating voltage.

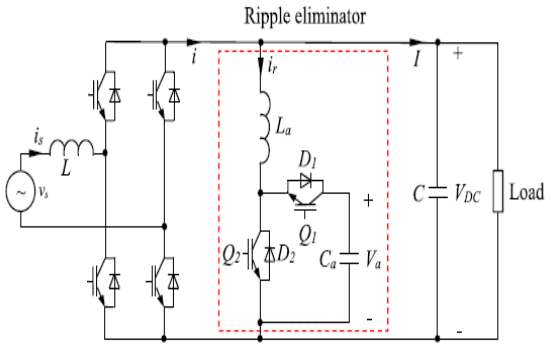

Fig 3: The ripple eliminator under investigation.

If the same ripple energy E_r needs to be taken care of by a DC-bus capacitor C, as shown in

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Figure 2, then, according to (3), the voltage ripple ratio r of the DC bus is about

$$r \approx \frac{E_r}{CV_{DCO}^2} \quad (6)$$

This means the auxiliary capacitor needed can be reduced to

$$C_a \approx \frac{r}{r_a}\left(\frac{V_{DCO}}{V_{ao}}\right)^2 C \quad (7)$$

By a factor of

$$R_d = \frac{r_a}{r}\left(\frac{V_{ao}}{V_{DCO}}\right)^2 = \frac{\Delta V_a V_{ao}}{\Delta V_{DC} V_{DC0}} \quad (8)$$

The capacitance Ca can be reduced by 1) allowing the voltage ripple ratio higher than that of the original DC bus, 2) adopting an operating voltage Va0 higher than VDC0 for Ca. The basic guidelines for designing different ripple eliminators. Some other guidelines include: 1) a ripple eliminator needs to be able to provide bi-directional current path so that the ripple current can ow through; 2) the remaining level of DC-bus voltage ripples is determined by the performance of the ripple eliminator so the ripple eliminator needs to be controlled properly; 3) The hold-up time requirement, voltage stress and current stress should be considered to choose suitable capacitors.

THE RIPPLE ELIMINATOR UNDER INVESTIGATION

Operation principles of the ripple eliminator

In this paper, a practical implementation of the ripple eliminator concept to be studied is shown in the dashed box of Figure 4, which is actually a bi-directional boost-buck converter. In order to track the ripple current, switches Q1 and Q2 can be controlled in two different switching modes. One is only to control Q2 (Q1, resp.) in the positive (negative, resp.) half cycle of the ripple current, which corresponds to the charging (discharging) mode.

In the charging mode, Q2 is controlled by a PWM signal and Q1 is always OFF, which provides the path for the positive half cycle of the ripple current ir , and hence, the ripple eliminator is operated as a boost converter. In the discharging mode, Q2 is always OFF and Q1 is controlled by a PWM signal, which provides the path for the negative half cycle of the ripple current ir , and the circuit is operated as a buck converter. Therefore, the direction of the current owing through the auxiliary inductor can only be negative or positive in one switching period.

In one PWM period, if Q1 is ON, Q2 is controlled by an inverse signal to keep OFF and vice versa. Different from the previous operation mode, the inductor current can be positive or negative even during one switching period. In this paper, in order to fully use the ripple eliminator under different working conditions, Q1 and Q2 are operated complementarily to track the ripple current.

Selection of the auxiliary inductor

Inductor La, that affects the performance of the ripple eliminator. In this subsection, how to select the La is discussed.

Apart from the auxiliary capacitor Ca, there is another passive component, i.e., the auxiliary Here, the duty cycle and the PWM period time are denoted as dr and Tr , respectively. In other words, the current ripple Δir is

$$\Delta i_r = \frac{V_{DC}}{L_a} d_r T_r = -\frac{V_{DC}-V_a}{L_a}(1-d_r)T_r \quad (9)$$

Therefore, the duty cycle dr can be obtained as

$$d_r = 1 - \frac{V_{DC}}{V_a} \quad (10)$$

The substitution of (11) into (10) leads to

$$\frac{L_a \Delta i_r}{V_{DC}} = (1 - \frac{V_{DC}}{V_a})T_r \quad (11)$$

which can be re-written as

$$f_r L_a \Delta i_r = V_{DC}\left(1 - \frac{V_{DC}}{V_a}\right) \quad (12)$$

As expected, the product of the switching frequency fr , the inductance La and the current ripple 4ir is a constant, which is determined by the DC-bus voltage and the auxiliary voltage.

In this work, in order to ensure the inductor is operated in the critical continuous current mode, the amplitude of 4ir is designed to satisfy

$$\Delta i_r \le 2I_{rm} \quad (13)$$

where Irm is the peak value of ir . Considering (12), the auxiliary inductance should be selected to satisfy

$$L_a \ge \frac{V_{DC}\left(1-\frac{V_{DC}}{V_a}\right)V_{DC}}{2I_{rm} f_r} \quad (14)$$

On the other hand, the rising rate of the auxiliary inductor current should be greater than the maximum rising rate of the reference ripple current which appears at the zero-crossing point. If the reference ripple current is expressed as

$$i_r = I_{rm} \sin(2\omega t) \quad (15)$$

then the maximum rising rate of ir can be obtained as

$$\frac{di_r}{dt}|t = 0 = 2\omega I_{rm} = 4\pi f I_{rm} \quad (16)$$

CONTROL OF THE RIPPLE ELIMINATOR

Formulation of the control problem

As discussed before, the DC voltage ripple is caused by the pulsating input energy. After the ripple eliminator is introduced to divert the ripple current from the capacitor C, the DC-bus voltage then

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becomes ripple free, apart from switching ripples, and equal to the DC-bus voltage. Hence, the current to be diverted should be

$$i_r = -\frac{V_s I_S}{V_{DCO}} \cos(2\omega t) \quad (17)$$

In this paper, the CCM operation is chosen because of its high performance for current tracking. The ripple current tracking can be achieved in two steps: 1) to generate a reference ripple current and 2) to track the reference ripple current.

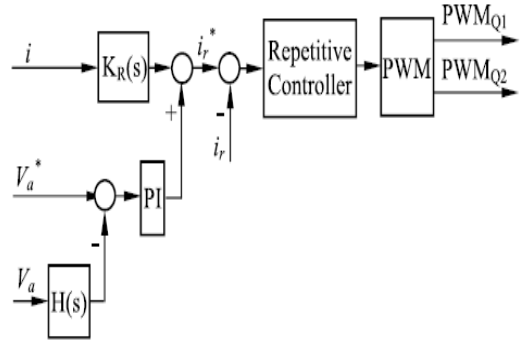

Fig 4: Control of the ripple eliminator

Regulation of the auxiliary capacitor voltage

The operation of the ripple eliminator relies on a properly regulated the voltage across the auxiliary capacitor, which is designed to allow a significant amount of ripples. For the purpose of maintaining the average DC component at a certain value, a low-pass filter can be adopted to remove ripples. Here, the following low-pass filter

$$H(S) = \frac{1-e^{-\tau s/2}}{\tau s/2} \quad (18)$$

in which is chosen as the system fundamental period, is used.

Generation of the reference ripple current i_r^*

The second-order harmonic current of the current i between the rectifier and the ripple eliminator can be extracted by using the following resonant filter tuned at the second harmonic frequency with D 0:01, h D 2, and ! D 2f . If the harmonic current has components at other frequencies, then KR(s) can be designed to include the corresponding term. For example, if there is a 3rd-order harmonic current, then KR(s) can include a term with h D 3. The extracted current can be added to the output of the PI controller that regulates the auxiliary capacitor voltage to form the reference ripple current ir ; see Figure 6.

$$K_R(S) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2}$$

Design of a current controller to track the second-order ripple current

As explained before, the control problem is essentially a current tracking problem. Since the reference ripple current is periodic, the repetitive control strategy [29], [30] can be adopted to achieve excellent tracking performance with a xed switching frequency, as shown in Figure 6.

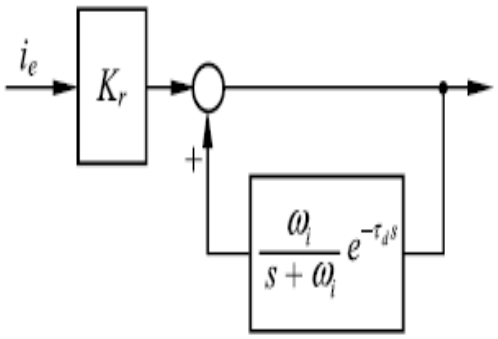

Fig 5: The repetitive controller.

A repetitive controller contains an internal model, which is a local positive feedback loop involving a delay term and a low-pass lter, as shown in Figure 7.

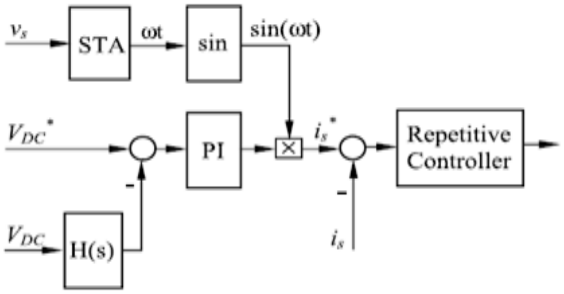

Fig 6: Controller for a single-phase PWM-controlled rectifier.

System parameters

Parameters	Values
AC voltage (RMS)	230 V
System fundamental frequency	50 Hz
Switching frequency	10 kHz
Inductor L	2.2 mH
Inductor L_a	2.2 mH
Capacitor C	110 μF
Auxiliary capacitor C_a	165 μF
Voltage V_{DC}	400 V

Control of the single-phase pwm-controlled rectifier

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The PWM rectifier is adopted as an example for generating voltage/current ripples in a DC system. This can be achieved with the controller shown in Figure 8, which mainly consists of three parts: 1) a synchronization unit to generate a clean sinusoidal current signal that is in phase with the source so that the reactive power drawn from the supply is controlled to be zero;

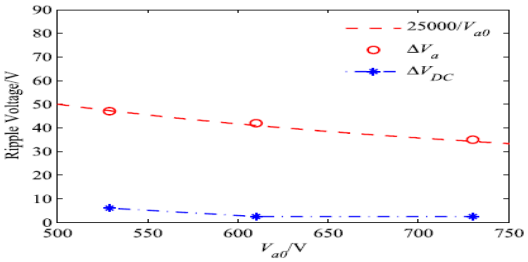

Fig 7: Voltage ripples on the DC bus (ΔV_{DC}) and the capacitor Ca (ΔVa) of the proposed ripple eliminator tested over a wide range of V_{a0}.

2) a PI voltage controller that maintains the voltage VDC according to the DC-bus reference voltage V DC to generate the right amplitude for the current reference; and

3) a current controller to track the reference current that is formed according to the PI voltage controller and the synchronization signal.

Validation without the ripple eliminator

Figure 9 shows the experimental results of the single-phase PWM-controlled rectier without the ripple eliminator.

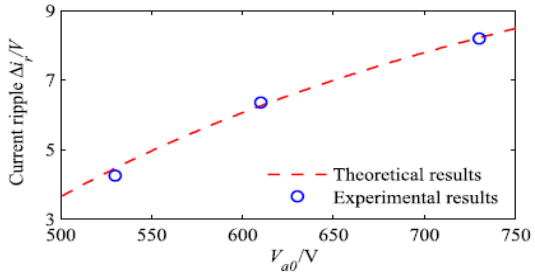

Fig 8: Current ripples 1ir on the inductor La over a wide range of Va0

The input current was well regulated to ben phase with the source voltage to achieve the unity power factor. However, the ripple of the VDC is around 90 V, which is often not acceptable in practice.

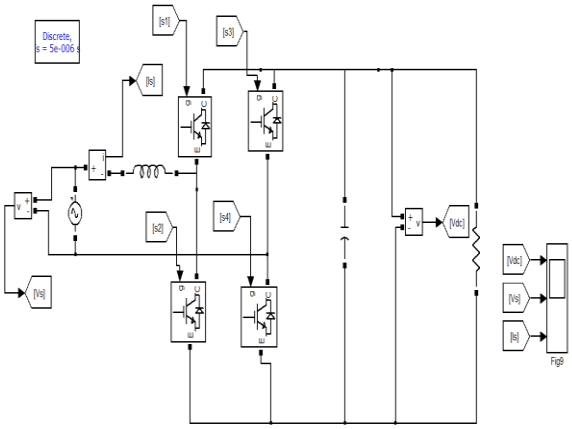

Fig 9: Simulink diagram Single-phase H-bridge PWM-controlled rectifier with out ripple eliminator.

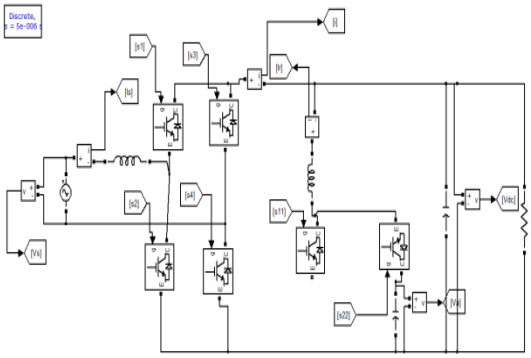

Fig 10: Simulink diagram Single-phase H-bridge PWM-controlled rectifier with ripple eliminator.

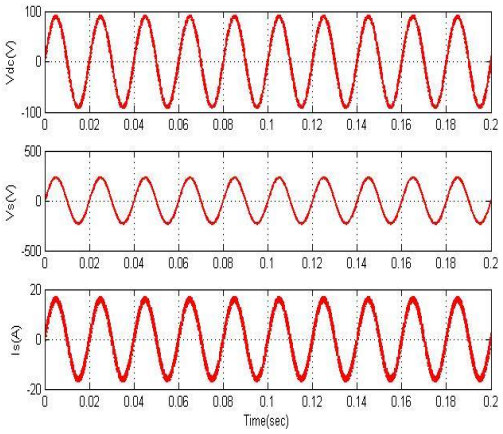

Fig 11: Simulation results when the ripple eliminator was not activated: DC-bus voltage V_{DC}, input voltage V_S and input current I_S with the ripple eliminator is not activated

When ripple eliminator activated

Figure 13 shows the results with the ripple eliminator activated. In order to investigate how the voltage Va

affects the reduction of the voltage ripple, different levels of the Va at 500 V, 600 V and 700 V were tested. Generally, it can be seen that the DC-bus voltage ripple was signicantly reduced for all these three voltages.

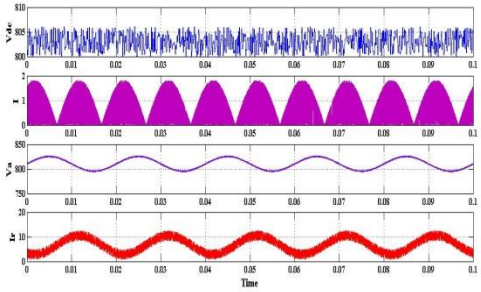

Fig 12(a): Simulation results with different auxiliary capacitor voltage of Va* 800 V.

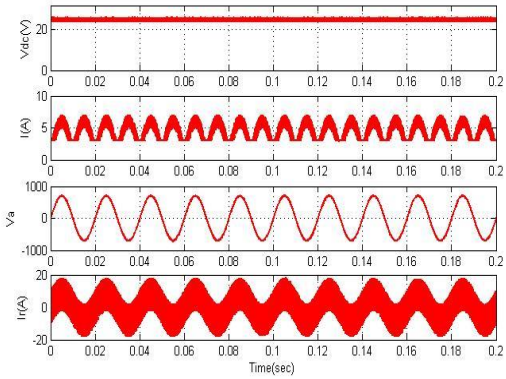

Fig 12(b): Simulation results with different auxiliary capacitor voltage of Va* 700 V.

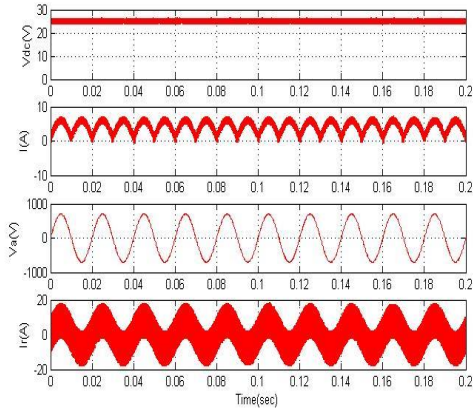

Fig 12(c): Simulation results with different auxiliary capacitor voltage of Va* 600 V.

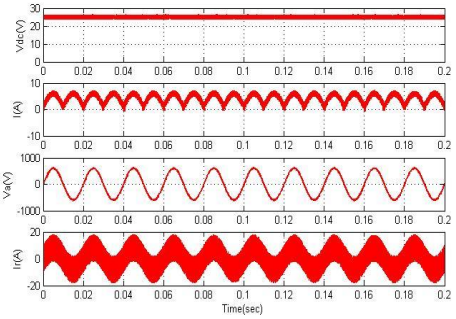

Fig 12(d): Simulation results with different auxiliary capacitor voltage of Va* 500 V.

CONCLUSION

In this paper the concept of ripple eliminators has been further developed to improve the power quality and reduce the voltage ripples in DC systems and, at the same time, reduce the capacitance needed and the usage of electrolytic capacitors. This paper has the following unique contributions: 1) It has been revealed that the capability of instantly diverting the ripple current away from the DC bus is the key to improve the performance. As a result, ripple eliminators that can be operated in CCM to instantaneously divert ripple currents are preferred; 2) the repetitive control strategy is proposed to control one exemplar ripple eliminator, with the ripple energy provided by a single-phase PWM-controlled rectifier. It instantaneously compensates the ripple current on the DC bus so that the voltage ripples on the DC bus can be significantly reduced. By using the simulation results we can demonstrated that the proposed strategy is valid and offers several times of performance improvement with comparison to a DCM ripple eliminator.

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