International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 12
April 2018

# Design an Fir Filter Using Modified Elm Adder

[1] Adapala.Gnana Lakshmi, [2] Govathoti.Kamala, [3] Gottam Triveni,
[4] Thota.Mahesh Babu
[1,2,3]B.Tech-Scholar, Dept of ECE, ST. Mary's Women's Engineering College, Guntur, India.
[4]Assistant Professor, Dept of ECE, ST. Mary's Women's Engineering College, Guntur, India.

**ABSTRACT:** *In this brief, we present a digital based reconfigurable finite impulse response (FIR) filter architecture. It provides flexible and low power consumption to the FIR filters with wide range of accuracy and tap length. The approach is well suited when the filter order is fixed and not changed for particular applications, and efficient trade-off between power savings and filter performance can be made using the proposed architecture. Generally, FIR filter has large amplitude variations in input data and coefficients. Considering the amplitude of the filter coefficients and inputs, the proposed FIR filter dynamically changes the filter order.*

**Key words:** Canonical signed digit (CSD), finite-impulse response (FIR) digital filters, reconfigurable architectures.

## I.INTRODUCTION

Finite impulse response (FIR) filters play a crucial role in many in signal processing applications in communication systems. A wide variety of techniques such as spectral shaping, matched filtering, channel equalization, interference cancellation etc. can be performed with these filters. Generally we use wired and wireless communication system for FIR architectures. Now software radio has gained much attention from the researchers from worldwide. This have strong demand for reconfigurable communication systems capable of multi-standard operations .here we consider programmability and reconfigurable for filter designing. It is well known as canonical signed digit (CSD) is used to reduce the complexity of FIR digital filter implementation. Encoding the filter coefficients using the CSD .partial products which saves the silicon area and power consumption in hardware implementation. By using CDS representations to implement programmable, rather than fixed coefficient, FIR filter. Mostly filters require few taps for high-precision coefficients .valuable hardware resources are wasted if all taps are implemented with high precision .To reduce hardware complexity, FIR filter implementation and they all limit the number of allowable non zero CSD s in every tap.

This can be applicable for lower the coefficient precision which can reduce the frequency response of the filter. A 32 –tap linear –phase filter, with two nonzero CSDs in each tap, is implemented. For example binary pseudorandom number (PN) code matched filter, this is the important block in CDMA receivers, which requires only 1-bit coefficient precision. 16-bit coefficient precision is required for pulse –shaping filter. Finite impulse response (FIR) filters play a crucial role in many signal processing in communication systems. We use various methods for better performance of FIR filters such as spectral shaping, matched filtering channel equalization, interference cancellation etc. The above methods are used to improve the speed of the filters.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 12
April 2018

In this brief, we adopt the finest granularity for filter implementation and reconfigurable FIR filter architecture with more flexibility. In this architecture, both the tap number and the number of nonzero digits in each tap hard ware resource is available .minimum total number of CSD for a given frequency response specification can be found. Filter implementation with this architecture can be easily configured as a matched filter, a pulse shaping filter. Furthermore FIR architecture also has modularity, and cascadability to VLSI implementation. Critical path delay is in proposed architecture stays quite invariant in different filter configurations.

## II.BLOCK DIAGRAM OF A RECONFIGURABLE FIR CHIP

In order to reduce the area and the latency required for implementing the addition in the filtering process, eight adders are combined to form one single big adder with nine inputs. Finally, the addend output of 8 DPUs, the output of the sing extension generator.

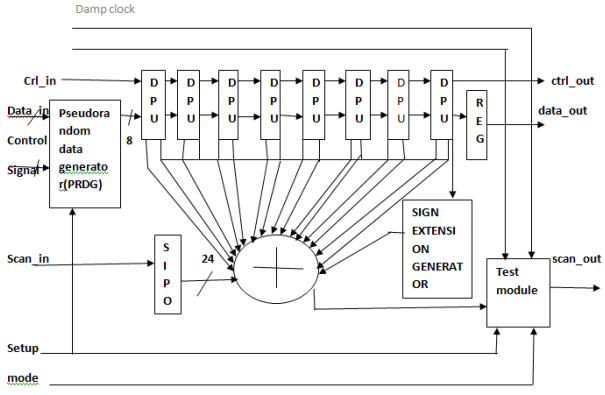


**Fig: 1. Block diagram of the reconfiguration filter chip**

The reconfigurable FIR chip consists of one PE, one pseudorandom data generator (PRDG) and one test module. There are two clock signals: CLK and Dump CLK. CLK controls the operating speed of the filter, while Dump CLK is used to initialize the chip parameters and to output the results. So, the REG in the PE that is used to store the accumulated sum is replaced by a 24 –bit SIPO REG array.

A PRDG is designed to provide the input test patterns for full-speed testing. The data fed into the first DPU can be just the data-in signal or from the PRDG. Finally, a test module accumulates the 24-bit output of the adder in PE with a 32-bit carry –save adder.

## III.CIRCUIT DESIGN

**A. Multiplier and Shifter:** The multiplier is used to multiply the input data which as three possible values: 1, 0, and -1. if the CSD coefficient is “1” the plus signal is “1” and the multiplier output is the same as the input. If the CSD coefficient is “-1” the plus signal is “0” and the multiplier output is set to the one’s complement of the input data.

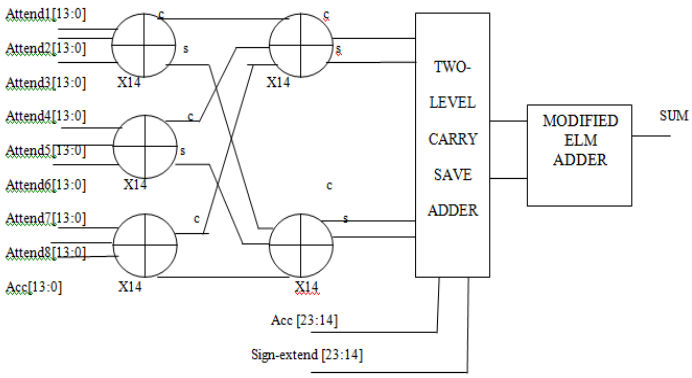

**Fig: 2. Adder structure in the reconfiguration filter chip**

**B. Sign Extension Generation:** A signal extension generator is designed to evaluate the sum of sign extension bits based on eight sign signals. Seven most significant bits can be determined by examining if there exits at least one "1" valued sign signal. It is also easy to see that the three LSBs are identical to the three LSBs of the binary representation of the number of non-negative sign signals. So, it can be implemented directly by complementing eight sign signals first, summing them together, and then taking the three LSBs of the sum.

**C. Adder:** The adder is used to sum eight 14-bit addend signals from DPU's, one 24-bit acc signal, and one10-bit Sign-extend signal from the extension generator. Signals adder1~adder8 corresponding to eight adder signals and the signal sign~ extend corresponds to the 10-bit signals from sign extension generator. The acc signal is split into two parts where its fourteen LSBs and eight addend signals are compressed into four 14-bit signals by five 14-bit carry save adders in a two-level arrangement. Finally, a modified ELM adder with reduced critical path delay is used to computer the final sum.

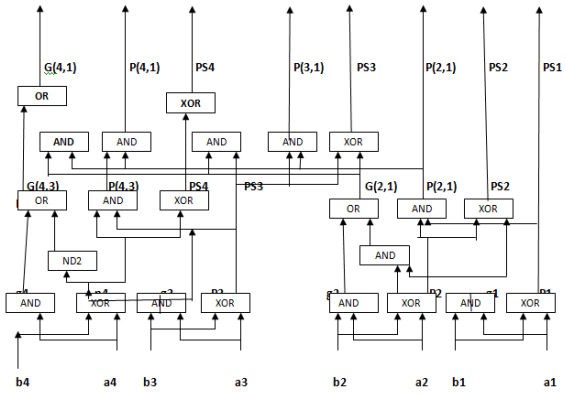


**Fig: 3(a). 4-bit ELM adder**

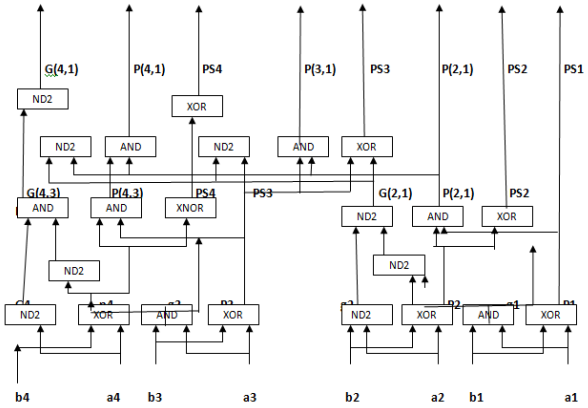


**Fig: 3(b). Modified 4-bit ELM adder**

The ELM adder is a kind of parallel adder first presented. Fig. 3(a) illustrates a 4-bit ELM adder and also the critical path is indicated in dashed lines. First, we can replace the OR gate and its two input AND gates by three NAND gates as shown in Fig. 3(b). Also, as can be seen in Fig. 3(a), the critical path includes an XOR gate and an AND gate. We can further reduce the critical path delay by inverting the two inputs of the XOR gate as shown in Fig. 3(b). These modifications reduced not only the critical path delay but also the transistor count and thus give a faster and smaller 4-bit parallel adder.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 12
April 2018

## IV. RESULTS

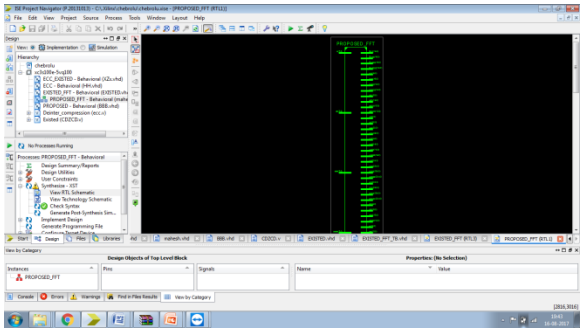

**Fig: 4. RTL Schematic**

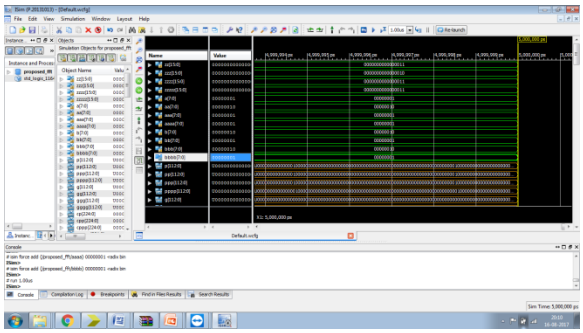

**Fig: 5. Output Waveform**

## V.CONCLUSION

In brief, a reconfigurable FIR filter architecture is proposed. The design concepts of the architecture and the circuit are presented. In this project the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply canceled. The filter performance degradation can be minimized by controlling the error bound as small as the quantization error or signal to noise power ratio (SNR) of given system.

## VI.REFERENCES

[1] J. Mitola, "The software radio architecture," *IEEE Commun. Mag.*, vol. 33, pp. 26–38, May 1995.

[2] M. Isohookana, T. Kokkonen, P. Leppanen, A. Nykanen, J. Pyhtila, J. Reinila, J. Sillanpaa, and V. Tapio, "Software radio-an alternative for the future in wireless personal and multimedia communications," in *Proc. IEEE Int. Conf. Personal Wireless Commun.*, 1999, pp. 364–368.

[3] E. Buracchini, "The software radio concept," *IEEE Commun. Mag.*, vol. 38, pp. 138–143, Sep. 2000.

[4] R. M. Hewlitt and E. S. Swartzlantler, Jr., "Canonical signed digit representation for FIR digital filters," in *Proc. IEEE Worksh. Signal Process. Syst.*, 2000, pp. 416–426.

[5] M. Tamada and A. Nishihara, "High-speed FIR digital filter with CSD coefficients implemented on FPGA," in *Proc. ASP DAC'01*, 2001, pp.7–8.

[6] Y. M. Hasan, L. J. Karem, M. Falkinburg, A. Helwig, and M. Ronning, "Canonic signed digit Chebyshev FIR filter design," *IEEE Signal Process. Lett.*, vol. 8, no. 6, pp. 167–169, Jun. 2001.

[7] T. Zhangwen, Z. Zhanpeng, Z. Jie, and M. Hao, "A high-speed, programmable, CSD coefficient FIR filter," in *Proc. 4th Int. Conf. ASIC*, 2001, pp. 397–400.

[8] K. T. Hong, S. D. Yi, and K. M. Chung, "A high-speed programmable FIR digital

filter using switching arrays," in *Proc. IEEE Asia Pacific Conf. Circuits Syst.*, 1996, pp. 492–495.

[9] T. Rissa, R. Uusikartano, and J. Niittylahti, "Adaptive FIR filter architectures for run-time reconfigurable FPGAs," in *Proc. 2002 IEEE Int. Conf. Field Programm. Technol.*, Dec. 2002, pp. 52–59.

[10] K. Y. Khoo, A. Kwentus, and A. N.Willson, Jr., "A programmable FIR digital filter using CSD coefficients," *IEEE J. Solid-State Circuits*, vol. 31, no. 6, pp. 869–874, Jun. 1996.

ADAPALA. GNANA LAKSHMI pursuing B.Tech final year in St.Mary's women's engineering college, Budampadu. Her area of interest is communications.

GOVATHOTI. KAMALA pursuing B.Tech final year in St.Mary's women's engineering college, Budampadu. Her area of interest is communications.

GOTTAM. TRIVENI pursuing B.Tech final year in St.Mary's women's engineering college, Budampadu. Her area of interest is communications.

THOTA MAHESH BABU, M.tech in Embedded Systems and Working as Assistant professor in St.Marry's womens EngineeringCollege,Budampadu