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A Novel 5-level front-end bidirectional diode clamped AC-DC-AC converter

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Abstract- *This project proposes novel multilevel AC/DC/AC converters with reduced number of semiconductor devices to achieve light weight, efficiency and better input current quality. The proposed three-phase front-end bidirectional five-level (5L) rectifier and rear-end 5L-inverter are constructed based on multiple-pole multilevel diode-clamped approach (M^2DCC), which consist a total number of 24 diode components clamped. Based on M^2DCC concept, the number of switching devices can be further reduced to construct a new unidirectional front-end rectifier (M^2SCR). Comparative studies are conducted to analyze the performances of the two proposed front-end rectifiers with supportive mathematical derivations. In this project a single-stage converter was proposed for integrating Wind system with Grid by reducing the number of switches. Due to incident wind speed, maximum output power of wind turbine is obtained in different speed of the turbine. The generator speed must be adjusted according to instantaneous wind speed to obtain incident maximum power. Tip speed ratio (TSR) technique is used for MPPT. This MPPT method will generate the reference speed for speed controller of PMSG. The comparative analysis has been done for steady and transient state wind speeds.*

I. INTRODUCTION

Multilevel AC/DC/AC converters (which consists of front-end rectifier and rear-end inverter) for medium-high power motor drives are widely employed in many industrials. This configuration is favorable for many applications such as heat, ventilation and air conditioning (HVAC) systems, pump/blower/traction drives and even permanent-magnet synchronous generator wind turbine with grid-connected [1]. Due to the advantage of decoupling both front-end source and rear-end load through a dc-link, and simple control techniques can be implemented to achieve optimum performance [2]. The general trend in power electronics has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses which become significant at high power levels [3]. Several methods for decreasing switching losses and, at the same time improving power quality, have been proposed including constructing resonant converters and multilevel converters.

Three-Phase diode rectifiers are widely employed in common ac–dc power conversion or as an input stage for conventional rectifier-inverter based ac motor drives. However, such topology exhibits low input power factor (PF) and injects large current harmonics into utilities, resulting in increased distortion of supply voltage, malfunction of sensitive electronic equipment, increased losses contributing to inefficient use of electric energy [4-6]. In recent years, many promising PF correction techniques have been proposed. Among them, the three-phase three-level topology was found to be very attractive. This topology reduces the voltage stress on the power switches and only half of dc link voltage is applied across them, allowing the use of low loss and low cost power devices. This three-phase three-level rectifier was proposed initially by Kolar in [1], and was typically controlled with the conventional hysteresis current control. Further work on this control strategy promises the advantages of easy implementation,

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good accuracy, and high robustness. However, it was found later that a conventional hysteresis current controller with a fixed hysteresis band has the drawbacks that the modulation frequency varies throughout the fundamental period, and the instantaneous error can reach double the value of the hysteresis band due to interference between the three phases. Subsequent research by Zhao et al., and Ide et al. showed that a space vector control and double ramp comparison control can overcome the above shortcomings and show a high performance [7]. However, these methods all need well ascertained complex space vectors necessitating a complex control circuit and are much too uneconomical to implement. As an alternative, Maswood et al. proposed a single equidistant firing control for the front-end rectifier bidirectional switches in a three-phase rectifier-inverter structure [8]. However, this topology required large input inductors to achieve unity PF.

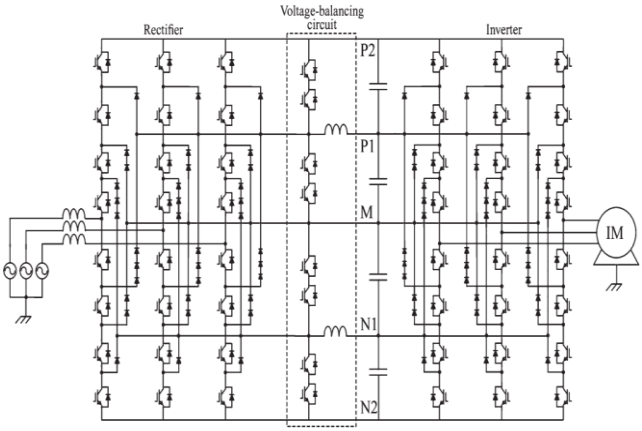

Fig 1: Proposed five-level bidirectional AC/DC/AC drive based on multiple-pole multilevel diode-clamped converter (5L-M^{2}DCC) approach

Two proposed combinations of 5L multiple-pole AC/DC/AC drives are the front-end bidirectional (5L-M^{2}DCR in Fig. 1) and unidirectional (5L-M^{2}SCR) rectifiers connected to the same rear-end (5L-M^{2}DCI in Fig. 1) inverter. To yield a fair analysis, the performances of both the proposed front-end rectifiers with the 5L-M^{2}DCI are evaluated with the proposed power factor correction technique.

II. FIVE-LEVEL AC/DC/AC TOPOLOGIES

M^{2}DCI topology: The output voltage Va can generate any voltage level from node p3, p2, p1, m, q1, q2 and q3 for the combination of seven level voltage steps. The interconnection point of two series connected dc capacitors is associated with the diodes clamping and connected to the center node of two series connected switching devices to synthesis seven-level voltage steps. However, this technique requires number of diodes to generate the desired output voltage levels. To simplify the classical MDCI topology into a less number of components count.

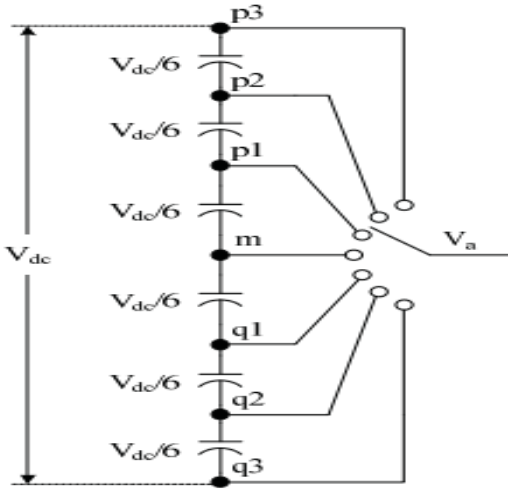

Fig. 2: Circuit diagram of per-phase single-pole classical 7L-MDCI topology with ideal switching device

The basic function block diagram of multiple-poles per-phase leg nthL-M2 DCI topology is shown in fig. 2 and this concept can be derived from fig. 1. Each sub-cell circuit diagram of 3L-NPC inverter can be presented as an ideal switching element with the similarity concept of fig. 1. The operating voltage level of the output terminal is depending on the individual cell 3L_NPC circuit's connection point, which is corresponding to the midpoint m.

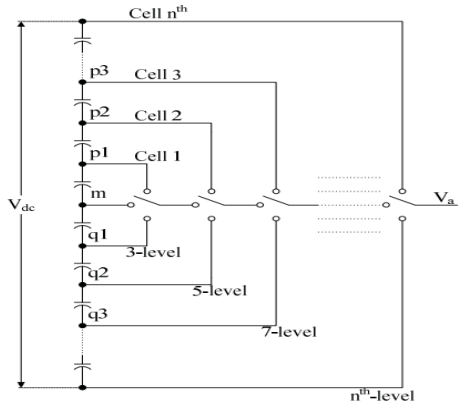

Fig 3: Circuit diagram of per-phase leg multiple-poles multilevel diode-clamped inverter (M2DCI) topology with ideal switching device

Classical Bidirectional Front-End 5L-MDCR with Rear –End 5L-MDCI Topologies:

The classical 5L-MDCC AC/DC/AC converter is a back-to-back (BTB) configuration based on a front-end bidirectional rectifier (Fig. 3) and a rear-end five-level diode-clamped inverter. A total of sixteen IGBTs and twelvediodes in each phase-leg are required in this topology to synthesize the five-level input and output voltage waveforms.The five-level voltage stepped waveform is obtained with the switching positions based on a single-pole circuit configuration as shown in Fig. 5.

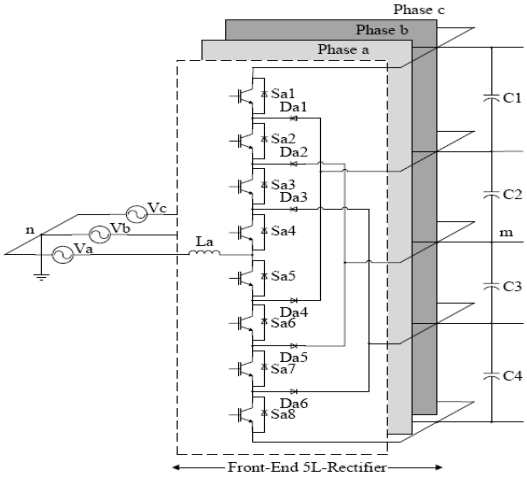

Fig 4: Classical front-end five-level bidirectional rectifier (5L-MDCR)

Proposed Bidirectional Front-End 5L-M^{2}DCR with Rear-End 5L-M^{2}DCI Topologies:

The proposed 5L-M^{2}DCC AC/DC/AC drive presented in Fig. 4 consists of a front-end bidirectional 5L-M^{2}DCR and a rear-end 5L-M^{2}DCI. This BTB topology requires only eight power diodes in each phase-leg to achieve the same input and output quality as the classical 5L-MDCC. However, when the number of cells in this proposed topology increases, a total number of 6(n-3) diode components are reduced.

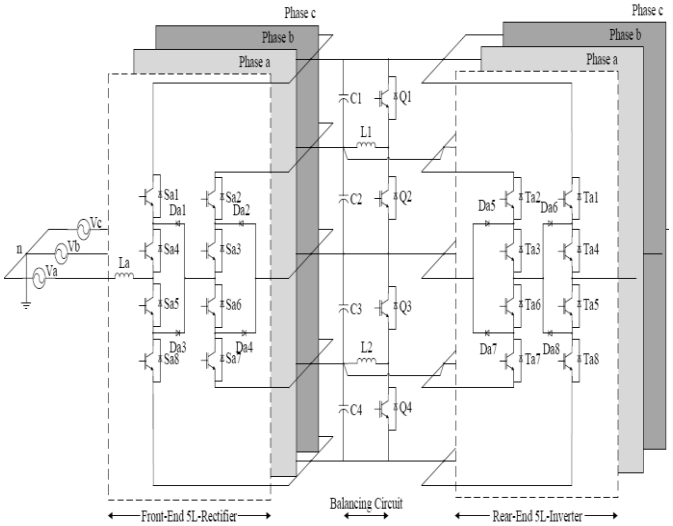

Fig 5: Proposed five-level bidirectional AC/DC/AC drive based on multiple-pole multilevel diode-clamped converter (5L-M2DCC) approach

The five-level voltage stepped waveform of M^{2}DCC topology is achieved with the switching positions based on the multiple poles hierarchy. The proposed 5L-M^{2}DCC topology is configured with two classical 3L-MDCCcells (Outer cell – Cell 2 and Inner cell – Cell 1) in each phase-leg, which is constructed based on the multiple-pole concepts.

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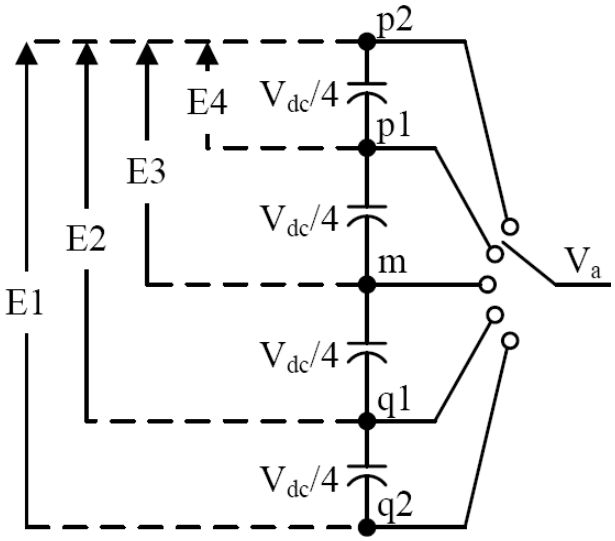

Fig 6: Circuit diagram of per-phase leg single-pole classical 5L-MDCC topology with switching position

Vom / Switch	Vdc/2 (Sector II)	Vdc/4 (Sector I & III)	0 (Sector I, III, IV & VI)	-Vdc/4 (Sector IV & VI)	-Vdc/2 (Sector V)
Sa1, Ta1	1	0	0	0	0
Sa2, Ta2	1	1	0	0	0
Sa3, Ta3	1	1	1	0	0
Sa4, Ta4	1	1	1	1	0
Sa5, Ta5	0	1	1	1	1
Sa6, Ta6	0	0	1	1	1
Sa7, Ta7	0	0	0	1	1
Sa8, Ta8	0	0	0	0	1

Table 1: Switching logic for respective igbt in 5l-m2dcc topology

Proposed Unidirectional Front-End 5L-M²SCR with Rear-End 5L-M²DCI Topology:

A bidirectional power flow in the front-end rectifier is not required for certain AC/DC/AC drive applications such as propulsion, compressor or any non-regenerative braking system. Thus, a proposed transformer-less front-end unidirectional rectifier is re-constructed in Fig. 6 with the arrangement of the semiconductor devices in the bidirectional M²DCR configuration (Fig. 4). Hence, the unidirectional 5L rectifier in Fig. 6 is named as multiple-pole multilevel switch-clamped rectifier (M²SCR) instead.

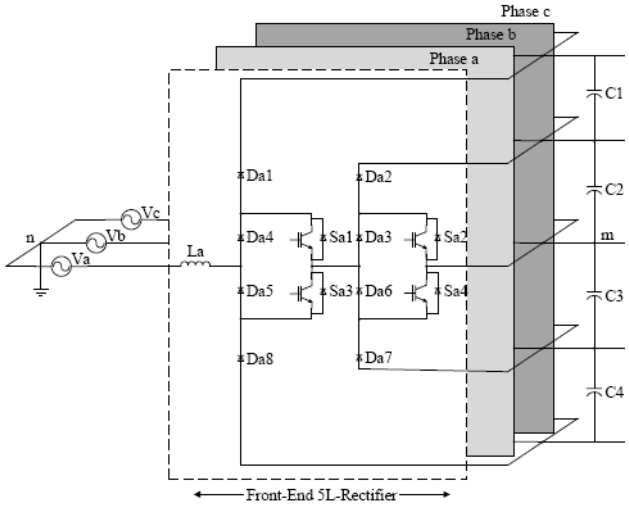

Fig 7: Proposed front-end five-level unidirectional rectifier (5L-M²SCR)

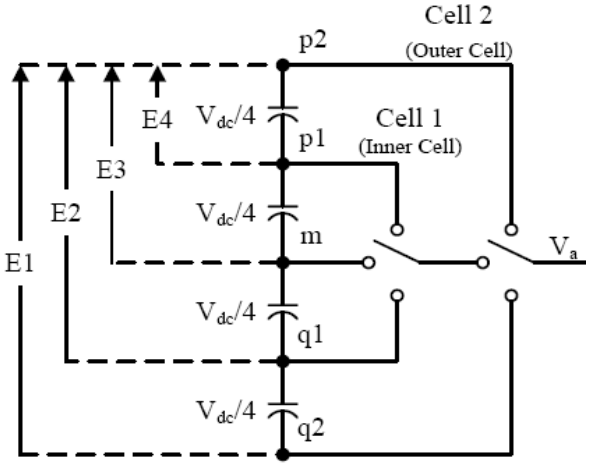

Fig 8: Circuit diagram of per-phase leg multiple-pole 5L-M2DCC topology with switching position

Each phase-leg of the proposed unidirectional 5L-M²SCR also requires two cells as shown in Fig. 5 to achieve five-level input voltage stepped waveform. The states selection of the top and bottom diodes of a M²SCR is dependent on 1-Sa1 and 1-Sa2 for the outer cell and similarly for the inner cell. Hence, only two switching devices are required in each cell with four series diodes connected to the terminals of the capacitors in the dc-link.

III. CONTROL OF THE FIVE-LEVELRECTIFIER AND INVERTER

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The control system is based on a fully digital control circuitusing DSPs and field-programmable gate arrays. Each datasampling of the source voltages and currents and the four dc capacitor voltages are performed at every top and bottom ofthe four carrier signals with different dc-bias voltages. Fig. 12shows the control block diagram of the rectifier. It consists ofa decoupled current control and dc-link voltage control. The five-level rectifier and inverter use the fourcommon carrier signals, as shown in Fig. 13

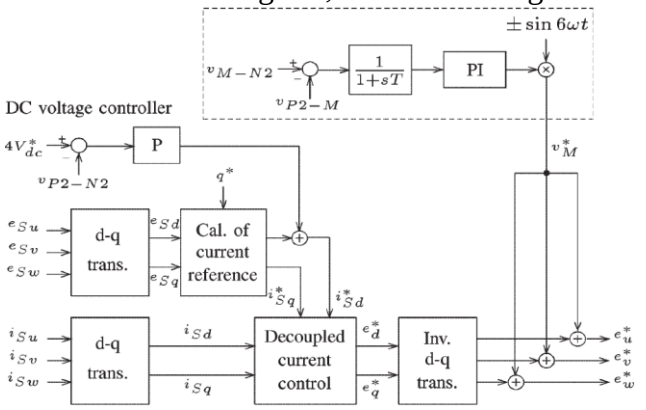

Fig 9: Control block diagram of the five-level converter

Voltage-Balancing Circuit:

The voltage-balancing circuit is installedon the dc side of the five-level converter. It consists oftwo positive and negative buck-boost choppers that are operatedindependent of each other; one is used for voltage balancing ofthe positive two capacitors and the other for voltage balancingof the negative two capacitors. Fig. 8 shows the control blockdiagram of the positive chopper with a proportional gain of1.4 A/V and an integral gain of 0.1 A/(V·s) in the voltageregulator and with a proportional gain of 0.2 V/A in thecurrent regulator. The voltage reference V_{CP}^{*} is compared to atriangle-carrier signal with a frequency of 3 kHz, to determinethe PWM gate signals for the positive chopper.

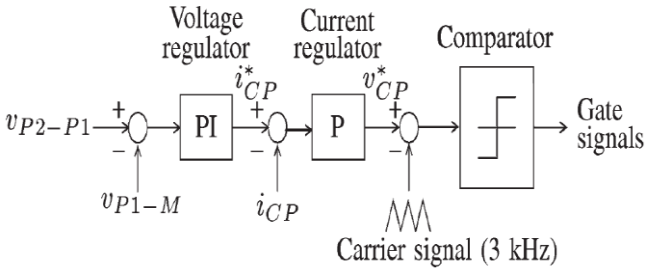

Fig 10: Control block diagram of the positive chopper in the voltage-balancing circuit

Synchronous-Reference-Frame Current Control Scheme

The proposed control algorithm with power factor correction technique is shown in Fig. 16. Two control loops, i.e. Synchronous-Reference-Frame Current Control and Constant Switching Frequency Modulation are implemented to regulate the dc-link voltage and mitigate the current distortions. Due to the simplicity of the control strategy, low cost integrated control circuit can be designed.

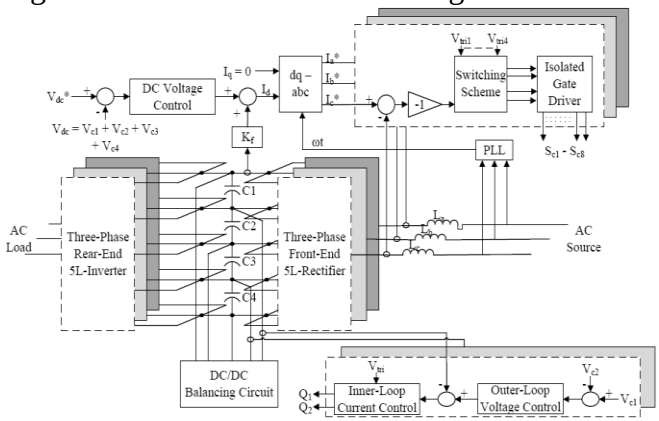

Fig 11: Proposed front-end rectifier controller for 5L-AC/DC/AC converter

IV. SIMULATION RESULTS

In this section, simulation results are presented to verify the validity of operations of the proposed system under steady- state and transient conditions. The simulated system parameters are listed in Table T. These simulations were performed using control systems mentioned in Section TV. The variable frequency mode of six switch AC/AC converter is selected since two three phase terminals of the converter work with different frequency.

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Furthermore, the DC-link capacitor sizes have been calculated according to the method proposed in [9].

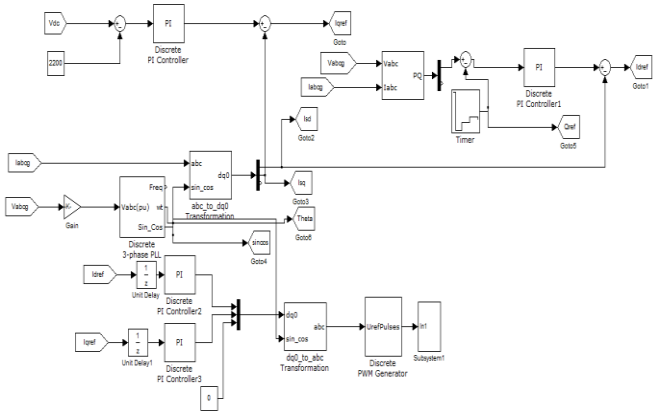


Fig.12: Block diagram of control of power delivered to the grid

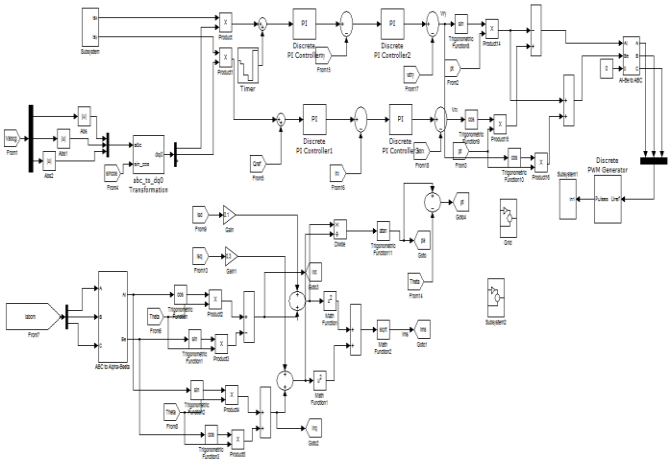


Fig.13: Block diagram of vector control for PMSG

Operation of Constant Wind Speed:

In this section, the steady state operation of the proposed system is verified through simulation results. For this purpose the wind speed is considered a constant value which is equal to 13 m/s. Another function of the grid side control system is to set the reactive power injected to the grid.

In this paper the unity power operation of wind energy system is desirable. As it is obvious in the figure, these two values are different from each other. It is because that a small portion of the mechanical power extracted from wind is dissipated in electrical and mechanical parts of WECS. In order to always track MPP, the reference value of PMSG rotor speed is set using TSR method and compared with the estimated rotor speed. This figure clearly shows the ability of proposed sensor less system to accurately estimate the rotor speed.. As is reflected in the figure, extracted mechanical power is tracking the maximum mechanical power after a short time.

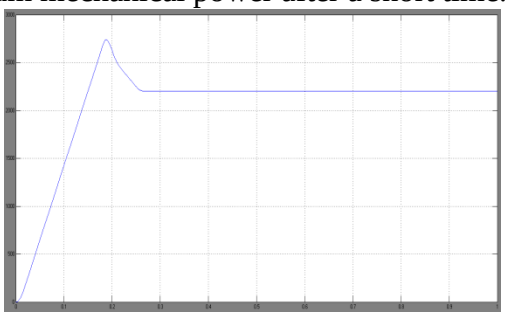


Fig.14: Capacitor voltage

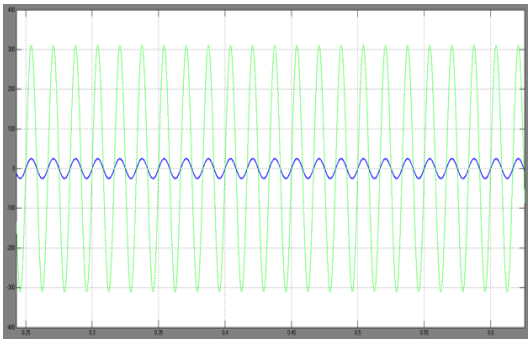
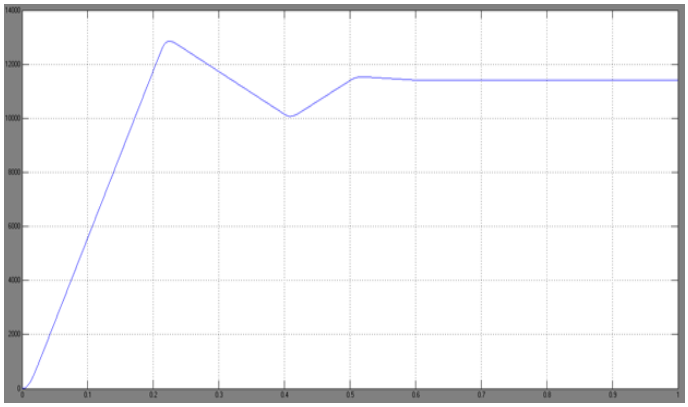


Fig.15: The grid voltage and the input current



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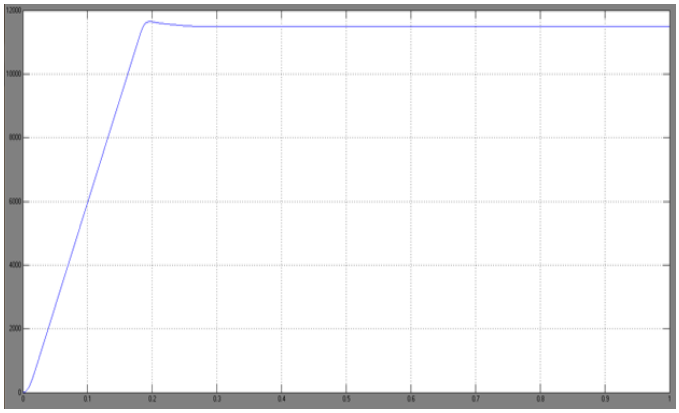

Fig.16: Power delivered to the grid and extracted mechanical power

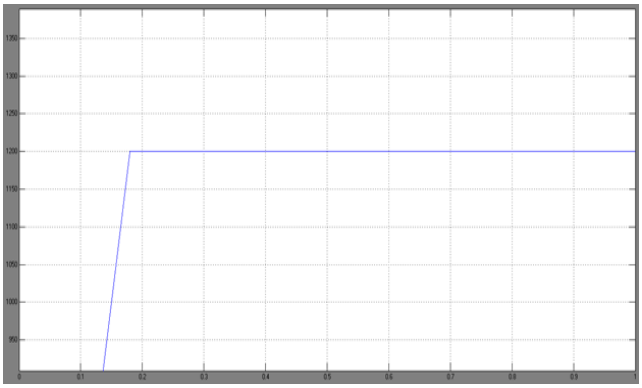

Fig.16 (a)

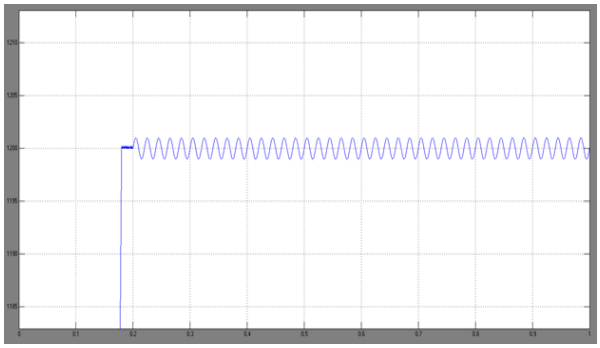

Fig.16 (b)

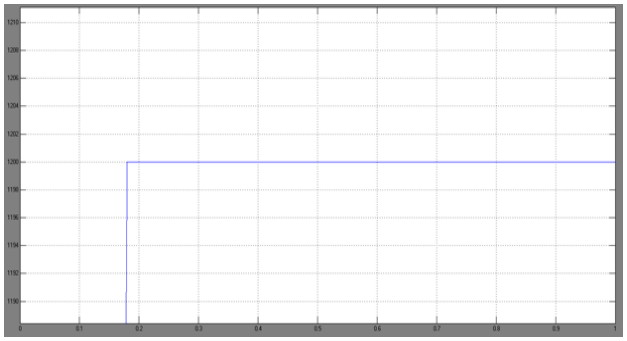

Fig.16 (c)

Fig.16: (a) Real rotor speed, (b) estimated rotor speed and the (c) obtained rotor speed from MPPT

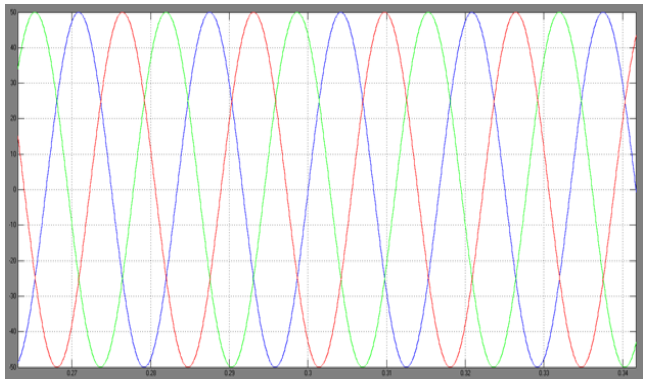

Fig.17: Injected three phase currents to the Grid

Operation of Variable Wind Speed:

In order to examine the proposed system performance under the transient condition, wind speed has been varied from 13 mls to 9 mls in t=0 . 6 sec and then from 9 mls to 11 mls in t=0.9 sec. The previous simulation is rerun in this transient condition and the simulation results are shown in Fig. 17 to Fig. 20. DC-link voltageis displayed in Fig. 17 which is almost constant although the wind speed undergoes two transient changes. Figs. 18-20 show active power injected to the grid, PMSG rotor speed, maximum possible of turbine mechanical power and the extracted mechanical power from the wind. Again under transient condition, the proposed sensorless system can effectively extract the maximum possible of mechanical power form wind turbine.

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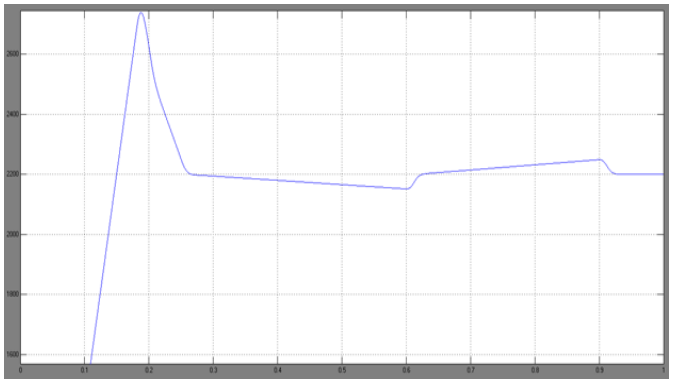

Fig.18: Capacitor voltage, transient condition

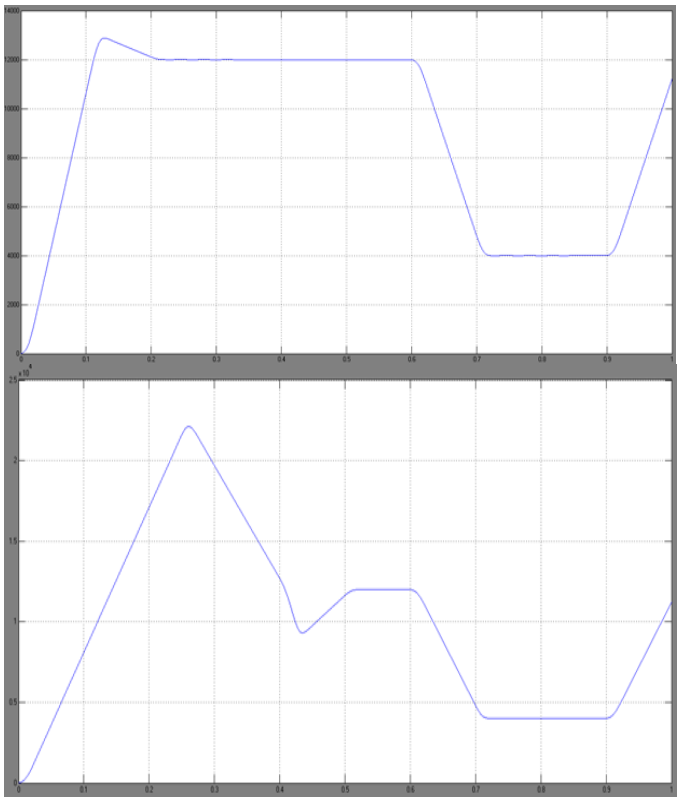

Fig.19: Active power delivered to the grid and extracted mechanical power, transient condition

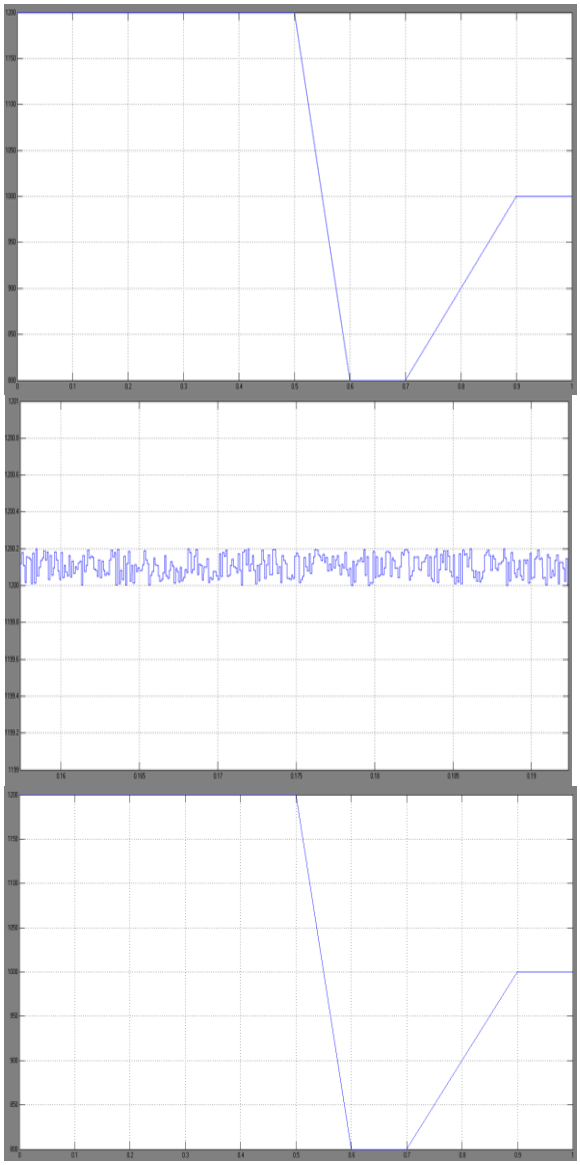

Fig.20: Real rotor speed, estimated rotor speed and the obtained rotorspeed from MPPT, transient condition

Wind energy conversion systems with doubly fed induction generator: With the increase in population and industrialization, the energy demand has increased significantly. However, the conventional energy sources such as coal, oil, and gas are limited in nature. Now, there is a need for renewable energy sources for the future energy demand. The other main advantages of this renewable source are eco-friendliness and unlimited in nature. Due to technical

advancements, the cost of the wind power produced is comparable to that of conventional power plants. Therefore, the wind energy is the most preferred out of all renewable energy sources.

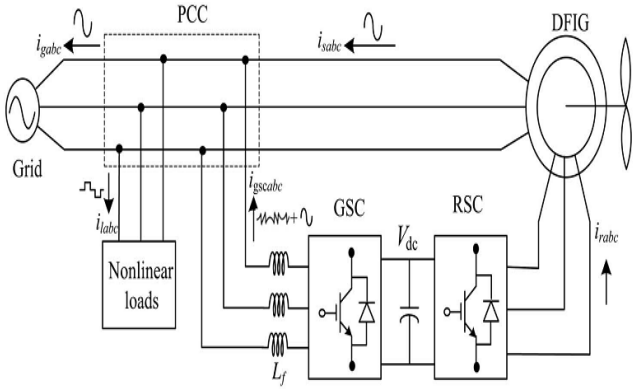

Fig. 21: Proposed system configuration.

Design of DFIG-based WECS:

Selection of ratings of VSCs and dc-link voltage is very much important for the successful operation of WECS. The ratings of DFIG and dc machine used in this experimental system are given in Appendix. In this section, a detailed design of VSCs and dc-link voltage is discussed for the experimental system used in the laboratory A. Selection of DC-Link Voltage Normally, the dc-link voltage of VSC must be greater than twice the peak of maximum phase voltage. The selection of dclink voltage depends on both rotor voltage and PCC voltage. While considering from the rotor side, the rotor voltage is slip times the stator voltage.

Selection of VSC Rating:

The DFIG draws a lagging volt-ampere reactive (VAR) for its excitation to build the rated air gap voltage. It is calculated from the machine parameters that the lagging VAR of 2 kVAR is needed when it is running as a motor. In DFIG case, the operating speed range is 0.7 to 1.3 p.u. Therefore, the maximum slip (smax) is 0.3. For making unity power factor at the stator side, reactive power of 600 VAR (Smax∗ Qs= 0.3 ∗ 2 kVAR) is needed from the rotor side (Q rmax). The maximum rotor active power is (Smax∗ P).

Maximum line current depends upon the maximum power and the line voltage at GSC. The maximum possible power in the GSC is the slip power. In this case, the slip power is 1.5 kW. Line voltage (VL) at the GSC is 230 V (the machine is connected in delta mode). So, the line current is obtained as I gsc = 1.5 kW/(√3 ∗230) = 3.765 A.

Control strategy:

The main purpose of RSC is to extract maximum power with independent control of active and reactive powers. Here, the RSC is controlled in voltage-oriented reference frame.

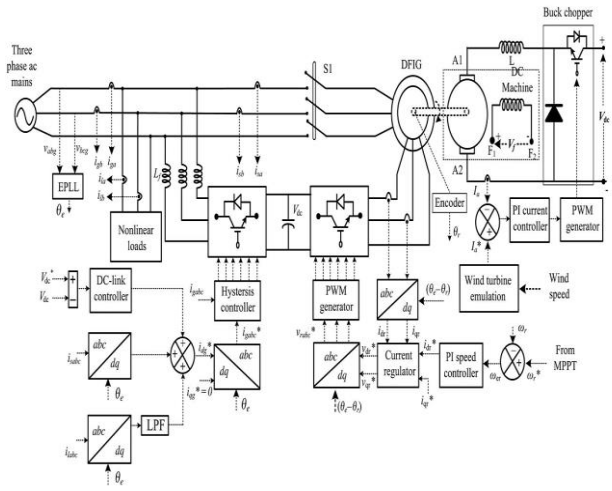

Fig 22: Control algorithm of the proposed WECS

The tuning of PI controllers used in both RSC and GSC are achieved using Ziegler Nichols method. Initially, kid value is set to zero and the value of k pd was increased until the response stars oscillating with a period of Ti. Now, the value of kpd is taken as 0.45 k pd and kid is taken as 1.2 kpd/Ti. Normally, the quadrature axis reference rotor current (i∗qr) is selected such that the stator reactive power (Q s) is made zero. In this DFIG, quadrature axis reference rotor current (i∗qr) is selected for injecting the required reactive power.

Control of GSC

The novelty of this work lies in the control of this GSC for mitigating the harmonics produced by the nonlinear loads.

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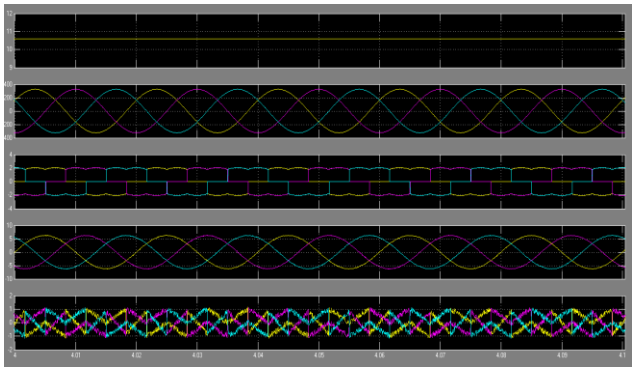
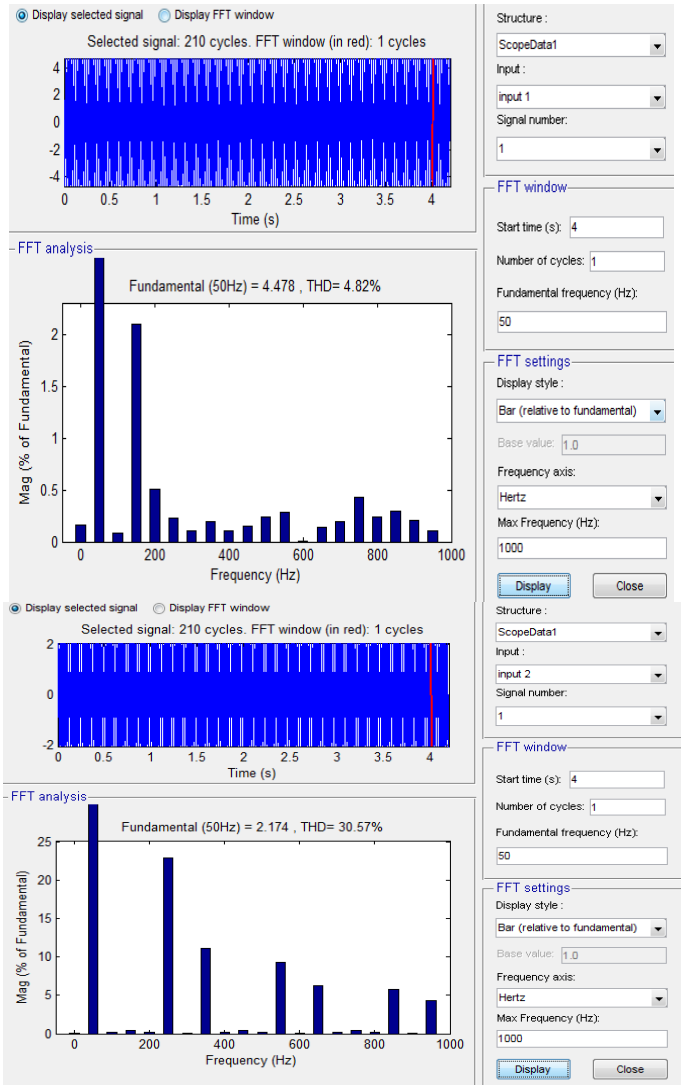


Fig. 23: Simulated performance of the proposed DFIG-based W ECS at fixed



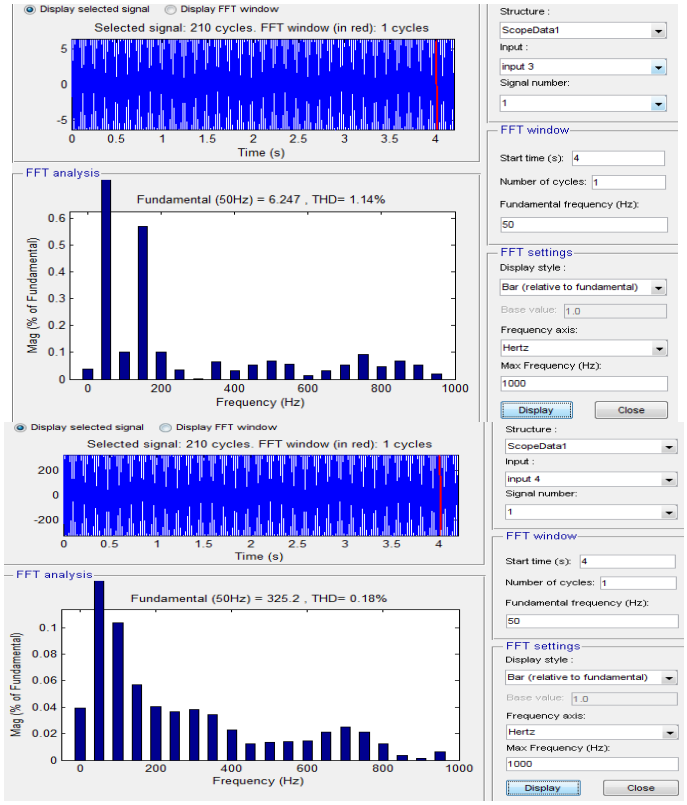


Fig 24. Simulated waveform and harmonic spectra of (a) grid current (i g a), (b) load current (i l a), (c) stator current (i s a), and (d) grid voltage for phase "a" (v g a) at fixed wind speed of 10.6 m/s (rotor speed of 1750 rpm)

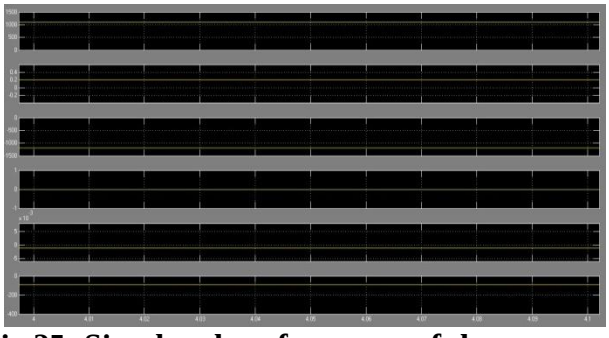


Fig 25: Simulated performance of the proposed DFIG-based WECS working as a STATCOM at zero wind speed

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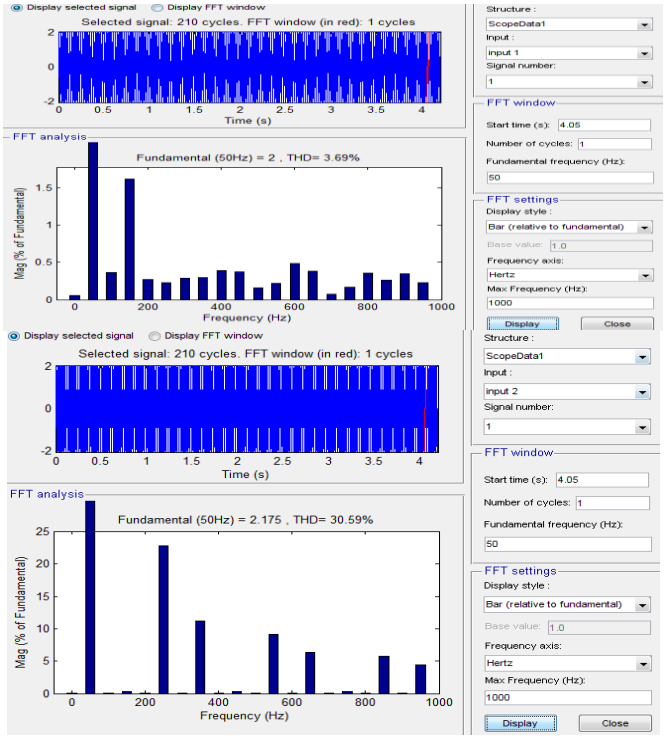

Fig 26: Simulated waveforms and harmonic spectra of (a) load current (i l a) and (b) grid current (i g a) working as a STATCOM at wind turbine shut down condition.

Fundamental active load current (ild) is obtained using SRF theory [33]. Instantaneous load currents (ilabc) and the value of phase angle from EPLL are used for converting the load currents in to synchronously rotating dq frame (ild). In synchronously rotating frames, fundamental frequency currents are converted into dc quantities and all other harmonics are converted into non-dc quantities with a frequency shift of 50 Hz. DC values of load currents in synchronously rotating dq frame (ild) are extracted using low-pass filter (LPF).

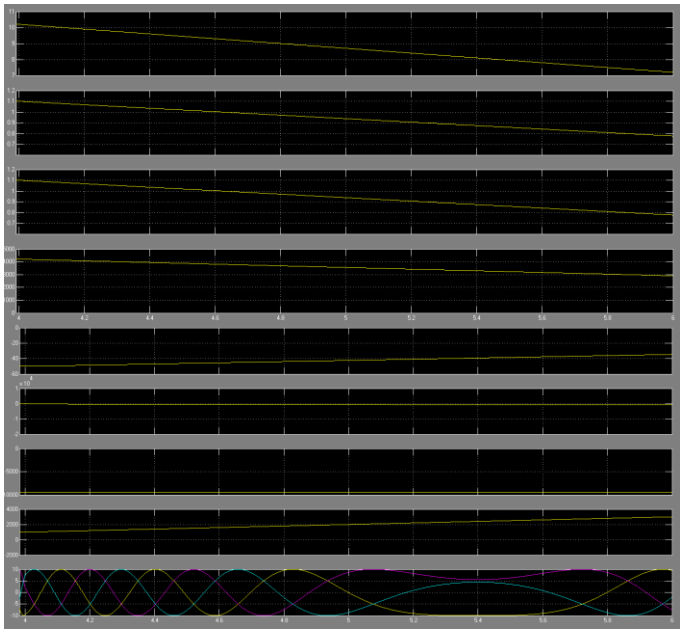

Fig 27: Simulated performance of proposed DFIG for fall in wind speed.load current (ild) in synchronously rotating frame and the loss component of GSC current (igsc)

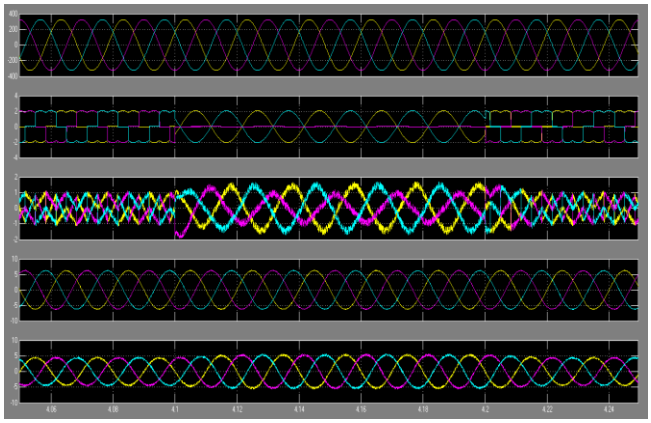

Fig 28: Dynamic performance of DFIG-based WECS for the sudden removal and application of local loads

V. CONCLUSION

The execution and low input current distortion with high power factor is accomplished with low operational switching frequency of 1 kHz without the guide of any bulky LC passive channel. Therefore, the general converter effectiveness is additionally

made strides. The extent of input reactors is significantly diminished too due to the incremental voltage balancing waveforms combined at low switching frequency. This is at the little cost of having an extra voltage adjusting hardware in the dc-connection to adjust the capacitor voltages. In this manner, alternative dc-link balancing systems or control calculations can be actualized to replant the extra balancing circuit. These will give a more cost effective and energy proficient solution for a more elevated amount AC/DC/AC drive and can particularly be reasonable for sustainable power source change where high effectiveness is vital.

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