# 3-Ph 3-Level Zvs Dc-Dc Converter 

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#### Abstract

This paper proposes development of soft switching scheme for three phase three level DC-DC converter for different duty cycles to achieve ZVS for all switches. The ZVS is achieved with output inductor and leakage inductor of transformer. This paper describes the main operational modes of proposed converter for different duty cycle and simulation results are observed and compare the switching losses of proposed converter with and without ZVS.


KEYWORDS—Zero Voltage Switching (ZVS), Three Phase Three Level (TPTL),DC-DC converter ,Pulse width modulation ,Duty cycle ,Soft switching.

## I. INTRODUCTION

In high voltage high power applications the ordinary converters exists many problems like stress on switches, switching losses, EMI etc.... These problems can be eliminated by using ZVS and ZCS converters. In ZVS, the switches are turned on and off at zero voltages and in ZCS, the switches are turned on and off at zero currents. As a result power reduces almost to a least value, by which the stress on the switches can be reduced .Full-bridge dc/dc converters have been widely used in medium to high power applications to further reduce the stress on switches for high power application TPTL was proposed. With three phase architecture the converter has the superior features including lower current rating of switches reducing input output current ripple allowing small size filter requirement. Although predominant characteristics exist in TPTL soft switching has not been achieved which limits the switching frequency and power loss. The use of Asymmetrical duty cycle in the three phase three level dc/dc converter was proposed in order to achieve ZVS commutation over a wide load range.

Fig. 1 shows the circuit configuration of TPTL converter in which, a three-phase transformer with $\Delta-Y$ connection is employed for the smaller turns ratios and transformer VA rating . As shown, Lra, Lrb and Lrc are the additional resonant inductances to widen the ZVS commutation load range. Llka, Llkb, and Llkc are the equivalent primary leakage inductances of each phase. Df1 and Df2 are freewheeling diodes. Css is the flying capacitor, which is in favor of decoupling the switching transition of Q1,Q3,Q4, and Q6 . DR1 - DR6 are rectifier diodes. The output filter is composed of Lf and Cf, and RLd is the load. Fig. 2 shows the control strategy of proposed converter. To realize the softswitching for switches, the original interleaved switches should be designed in a complementary manner, and a short delay time td is necessary to be introduced between the two complementary switches to provide an interval for the ZVS commutation, which is similar to the control strategy of asymmetrical half-bridge converter .Accordingly, the duty cycles of Q1,Q3, and Q5 are served to regulate the output voltage, while the drive signals of Q4,Q6 , and Q2 are complementary to that of the Q1, Q3 , and Q5 , respectively

## II. PROPOSED TPTL DC/DC CONVERTER FOR DIFFERENT DUTY CYCLES



International Journal of Research
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 12
April 2018

Fig. 1. Topology configuration of TPTL dc/dc converter.


Fig. 2. Asymmetrical duty cycle control.

## III. OPERATION OF PROPOSED TPTL CONVERTER

This section will analyze the operation principles of the TPTL converter under the modified control scheme. The following assumptions are made for the simplicity before the analysis:

1) all power devices and diodes are ideal;
2) all capacitors and inductances are ideal;
3) the output filter inductance is large enough to be treated as a constant current source during a switching period; its value equals to output current
4) the inductances of each phase are identical, i.e.,

Llka=Llkb= Llkc= Llk, Lra= Lrb= Lrc= Lr;
5) $\mathrm{C} 1=\mathrm{C} 2=\mathrm{C} 3=\mathrm{C} 4=\mathrm{C} 5=\mathrm{C} 6=\mathrm{C}$.

Fig. 3 shows the key waveforms of the TPTL converter with asymmetrical duty cycle control, as seen, the operation of the TPTL converter can be classified by different modes, according to the duty cycle range and the load current. The corresponding operation modes are defined as the small duty cycle mode (SDCM), and the large duty cycle mode (LDCM),respectively,


Fig. 3. Key waveforms of the TPTL converter with asymmetrical duty cycle control with SDCM.

The basic equations of the voltages and currents of the transformer are listed as follows:

$$
\begin{array}{r}
\mathrm{VAB}+\mathrm{VBC}+\mathrm{VCA}=0 \\
\mathrm{isa}+\mathrm{isb}+\mathrm{isc}=0 \\
\frac{d i a}{d t}=\frac{k(d i s a)}{d t}=\frac{v L l k a}{L l k}, \frac{d i p b}{d t}=\frac{k(d i s b)}{d t} \tag{3.3}
\end{array}
$$

Where $k$ represents the secondary-to-primary turns ratios of the transformer. The voltage across the leakage inductance of transformer can be derived from (3.2) and (3.3) and is given as follows

$$
\begin{equation*}
\mathrm{V}_{\mathrm{Llka}}+\mathrm{V}_{\mathrm{Llkb}}+\mathrm{V}_{\mathrm{Llkc}}=0 \tag{3.4}
\end{equation*}
$$

Operational mode 1: $\mathrm{t}_{\mathbf{0}} \leq \mathrm{t} \leq \mathrm{t}_{\mathbf{1}}$


Fig 3.4.4 Operation mode1 of the proposed converter

Fig.3.4.4 Shows $Q_{1}, Q_{2}, Q_{6}$, and $D_{f 2}$ are conducting at the primary side, and $D_{R 1}$ and $D R 6$ are conducting at the secondary side. $V_{\mathrm{AB}}=V_{\mathrm{in}} / 2, V_{\mathrm{BC}}=0$, and $V_{\mathrm{CA}}=-V_{\mathrm{in}} / 2$. From (3.1), (3.2), (3.4), and other constraints between voltages and currents of transformers, the following expressions can be obtained.

$$
\begin{align*}
& V p a=\frac{V i n}{2}, V p b=0, V p c=-\frac{V i n}{2}  \tag{3.5}\\
& \text { Vrect }=V s a-V s c . k . V \mathrm{in} \tag{3.6}
\end{align*}
$$

Where $V_{\text {pi }}$ and $V_{\text {si }}$ are the primary voltage and secondary voltage of transformers, $I$ represents the subscripts $a, b$, and c.

Operational Mode 2: $\mathrm{t}_{1} \leq \mathbf{t}<\mathrm{t}_{\mathbf{2}}$


Fig 3.4.5 Operation mode2 of the proposed converter
Fig.3.4.5 shows at $t_{0}, Q_{1}$ is turned off, the line current $i_{\mathrm{A}}$ charges $C_{1}$ and discharges $C_{4}$ linearly, and the rectified voltage decreases. As $C_{1}$ limits the rising rate of the voltage across $Q_{1}, Q_{1}$ is zero-voltage turn-off. The voltages across $C_{1}$ and $C_{4}$ are

$$
\begin{gather*}
V c 1(t)=\frac{1}{c p} k I o(t-t o)  \tag{3.7}\\
V c 4(t)=\frac{V i n}{2}-\left(\frac{1}{c p} k \cdot I o(t-t o)\right) \tag{3.8}
\end{gather*}
$$

At $t_{1}, V_{C 1}$ rises to $V_{\text {IN } / 2}$, and $V_{C 4}$ decays to zero; therefore, $D 4$ conducts naturally, and Vrect decreases to zero.

## Operation Mode 3: $\mathrm{t}_{\mathbf{2}} \leq \mathrm{t}<\mathrm{t}_{\mathbf{3}}$



Fig 3.4.6 Operation mode3of the proposed converter
Fig.3.4.6 Shows after $C 1$ is fully charged, the current flowing through $C 1$ transfers to $C$ ss and begins to charge Css. The voltage across Css will increase and block $D f 2$ to be off. During this stage, $V A B=V B C=V C A=0$. $D 4$ conduct
sand clamps the voltage across $Q 4$ at zero, so $Q 4$ can be turned on at zero-voltage condition. $D R 1$ and $D R 6$ conduct, and Vrect is still zero.

Operation Mode 4: $\mathbf{t}_{\mathbf{3}} \leq \mathbf{t}<\mathrm{t}_{\mathbf{4}}$


Fig 3.4.7 Operation mode4of the proposed converter
Fig.3.4.7 shows at $t_{2}, Q_{6}$ is zero-voltage turned-off and $V_{A B}$ increases reversely. If $v_{\text {pa }}$ keeps constant, the polarity of the voltage applied on $L_{\mathrm{lka}}$ will be non-associated with the current flowing through $L_{\mathrm{lk} a}$; as a result, $i_{\mathrm{pa}}$ will decrease and cannot provide the load current, then $D_{R 3}$ begins to conduct, and the current commutation between $D_{R 1}$ and $D_{R 3}$ occurs. In the primary stage, $C_{3}$ and $C_{6}$ resonate with the leakage inductances and the resonant inductances, and the following expressions will be obtained.

$$
\begin{align*}
& \mathrm{Vc} 6(\mathrm{t})=\frac{1}{2} \cdot \mathrm{k} \cdot I \mathrm{Io} \cdot \mathrm{Zr} \cdot \sin \left[\omega \mathrm{r}\left(\mathrm{t}-\mathrm{t}_{2}\right)\right]  \tag{3.10}\\
& \mathrm{i}_{\mathrm{A}(\mathrm{t})}=\frac{3}{2} k \cdot I o+\frac{1}{2} k \cdot I o \cos [\omega r(t-\mathrm{t} 2)] \tag{3.11}
\end{align*}
$$

During this stage, $V_{\text {rect }}$ remains at zero. When $V_{c 3}$ decays to zero, $D_{3}$ conducts naturally.

Operational Mode 5: $\mathbf{t}_{\mathbf{4}} \leq \mathbf{t}<\mathbf{t}_{\mathbf{5}}$


Fig 3.4.8 Operation mode5of the proposed converter
Fig.3.4.8 Shows $\operatorname{As} D_{3}$ is conducting, the voltage across $Q_{3}$ is clamped at zero; therefore, $Q_{3}$ is turned on at zerovoltage condition. During this stage, $Q_{2}, Q_{3}$, and $Q_{4}$ conduct in the primary stage, $V_{\mathrm{AB}}=-V_{\mathrm{in} / 2}, V_{\mathrm{BC}}=V_{\mathrm{in} / 2}$, and $V_{\mathrm{CA}}=0$. $D_{R 1}, D_{R 3}$, and $D R 6$ conduct in the secondary stage, and $V_{\text {rect }}=0$. From (3.1), (3.2), (3.4), and other constraints between voltages and currents of transformers, the expressions of the phase currents are given in (3.14)-(3.16)

$$
\begin{align*}
& \mathrm{i}_{\mathrm{pa}(\mathrm{t})}=\mathrm{i}_{\mathrm{pa}(\mathrm{t} 3)}-\frac{V i n}{2 L p} \cdot(\mathrm{t}-\mathrm{t} 3)  \tag{3.12}\\
& \mathrm{i}_{\mathrm{pb}(\mathrm{t})}=\mathrm{i}_{\mathrm{pb}(\mathrm{t} 3)}+\frac{\mathrm{Vin}}{2 \mathrm{Lp}} \cdot(\mathrm{t}-\mathrm{t} 3)  \tag{3.13}\\
& \mathrm{i}_{\mathrm{p}(\mathrm{t})}=\mathrm{kI}_{0} \tag{3.14}
\end{align*}
$$

Therefore, the line currents can be obtained from (3.14) to (3.16)

$$
\begin{equation*}
\mathrm{i}_{\mathrm{A}(\mathrm{t})}=\mathrm{i}_{\mathrm{A}(\mathrm{t} 3)}-\frac{V i n}{2 L p} \cdot(\mathrm{t}-\mathrm{t} 3) \tag{3.15}
\end{equation*}
$$

At the secondary stage, $I_{\mathrm{sa}}$ flows through $D_{R 1}$ and decreases with ipa from (3.12). When Isa decreases to zero, $D_{R 1}$ turns off and $D_{R 2}$ conducts. It should be noted that the rectified voltage is lost during the interval $t_{34}$, compared with the primary line voltage. Therefore, the duty cycle loss in SDCM is defined as

$$
\begin{equation*}
D \operatorname{loss} 1=\frac{t 34}{\frac{T s}{3}}=\frac{6 \mathrm{k} . \mathrm{Io} . \mathrm{Lp}}{\text { Vin.Ts }} \tag{3.16}
\end{equation*}
$$

Where Ts is the switching period.

## Operational Mode 6: $\mathbf{t}_{\mathbf{5}} \leq \mathbf{t}<\mathrm{t}_{\mathbf{6}}$

Fig.3.4.9 Shows During this stage, $V_{A B}=-V_{\text {in } / 2}, V_{\mathrm{BC}}=V_{\text {in } / 2}, V_{\mathrm{CA}}=0 . I_{s c}$ flows through $D_{R 6}, i_{\mathrm{sc}}$ and decreases with $i_{p c .}$ When $i_{\text {sc }}$ decreases to zero, $D_{R 6}$ turns off, the primary and secondary currents of transformer $T_{\text {rc }}$ are both zero. The time interval of this stage is given by

$$
\begin{equation*}
\mathrm{t} 45=\frac{4 k \cdot I o . L p}{\operatorname{Vin}} \tag{3.17}
\end{equation*}
$$


e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 12 April 2018

Fig 3.4.9 Operation mode6 of the proposed converter
Operational Mode 7: $\mathbf{t}_{6} \leq \mathrm{t}<\mathrm{t}_{7}$


Fig 3.4.10 Operation mode7 of the proposed converter

Fig.3.4.10 Shows $Q_{2}, Q_{3}$, and $Q_{4}$ conduct at the primary side, while $D_{R 2}$ and $D_{R 3}$ conduct at the secondary side, and the rectified voltage is kVin , which is similar to the stage1.

## IV. SIMULATION RESULTS FOR THREE PHASE THREE LEVEL DC/DC CONVERTER

In fig. 5 Simulink model of a $200 \mathrm{~V} / 16 \mathrm{~V}$ DC-DC converter has been proposed .In fig. 6 .output waveforms of the proposed converter is shown. In the proposed converter there is total six switches out of it Q1, Q3, Q5 are given with same duty cycle and Q2,Q4,Q6 are same having same duty cycle. Though the switches have same duty cycle all the switches not on for the same time In the proposed converter there are total six switches in which all are under goes soft switching for different duty cycles Fig. 7 \& Fig. 8 shows the simulation results for D=20\%.


Fig.5.Simulink diagram of Three phase Three-Level DC-DC converter.

As the duty cycle increases the output voltage will increases is shown in Table 1 . In which the output voltage will increases form $\mathrm{D}=20 \%$ to $46 \%$ and efficiency also increases.Fig6 represents output waveforms of the converter and three phase output voltage also observed in which all the phases are shifted by $120^{\circ}$. Fig7 represents soft switching of the proposed converter for Q1 and Q4 switches. Which is also same for Q2,Q3,Q5,Q6.Fig.7a shows voltage across Q1,fig 7b.shows the ZVS for Q1 from off to on \&fig7c shows on to off of Q1 under the ZVS .Fig 8a. shows voltage across Q4,fig 8b.shows the ZVS for Q4 from off to on \&fig 8c.shows on to off of Q4 under the ZVS.Fig9 shows graph between efficiency and load current at duty cycle $D=20 \%$, which will also represents the efficiency is high for with soft switching than without soft switching.
 International Journal of Research
e-ISSN: 2348-6848 p-ISSN: 2348-795X Available at https://edupediapublications.org/iournals


Fig 6 output waveform
Simulation results for Duty cycle 20\% Voltage across Q1





Fig.4.2.3.shows voltage across switch Q4 and ZVS is observed across switch Q4.In fig.4.2.3 (b) shows zvs for turn off to on and fig.4.2.3(c) shows zvs during on to off. ZVS is also observed in switches $\mathrm{Q}_{2}, \mathrm{Q}_{6}$.

### 4.2.1. SDCM with soft switching scheme ( $D=15 \%$ )

| Load <br> current(Amps) | Input <br> power(watts) | Output power <br> (watts) | Per switch <br> power <br> loss(watts) | Efficiency (\%) |
| :--- | :--- | :--- | :--- | :--- |
| 15.79 | 218.4 | 49.24 | 37.64 | 51.78 |
| 13.76 | 206.9 | 61.25 | 53.1 | 64.67 |
| 12.44 | 223.2 | 115.6 | 99.42 | 69.81 |
| 11.38 | 233.3 | 150.9 | 47.48 | 71.45 |
| 10.43 | 238.5 | 166.5 | 44.94 | 81.87 |



Fig. 9 Load current Vs Efficiency at D=20\%

## V. CONCLUSION

Soft switching scheme is achieved in each and every switch. Voltage stress across each switch was reduced. By increasing the voltage levels the size of the filter elements may also reduced. The switching losses in the proposed converter are
reduced. The proposed control scheme features the following characteristics: A. Compared with the hard switching technique the losses in switches predominately reduced B. The input capacitors can realize automatic and inherent voltage balancing, which ensures that all the
switches sustain only onehalf of the input voltage. C. The TPTL converter will operate in different duty cycles.

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