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Low power and high speed optimized 4-bit array multiplier using GDI technique

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Abstract:

Multipliers are the most commonly used elements in today's digital devices. It plays a very important role in some applications such as Digital Signal Processing and Image Processing applications. One of the basic multiplier is Array Multiplier. This multiplication is based on basic mathematic multiplication. Array multiplier can be implemented by using many techniques like CMOS,PTL,DPL etc. To overcome the limitations of these techniques a new technique is implemented in this paper, called Gate Diffusion Input (GDI). This paper aims at design of an optimized low power and high speed 4-bit array multiplier by using GDI Technique. With this technique total propagation delay, power consumption and transistor count are decreased compared to CMOS technology. The results give comparative analysis of CMOS and GDI techniques about power, transistor count and time delay parameters.

Keywords – CMOS, propagation delay, Multipliers, low-power design, performance, VLSI.

1. Introduction

In Digital Signal Processing applications, the applications include the operations like FIR filtering, IIR filtering, multi sampling rate conversion, linear convolution, circular convolution, DFT and FFT etc. All these operations require a number of multiplications to be perform. In order to achieve high data throughput, hardware multiplication is an important factor and also time is also an important factor in case of DSP applications. So by developing a multiplier, which performs the multiplication operation with less time, we can achieve high data throughput. One of the basic multiplier is the Array multiplier. Array multiplier can be implemented by using many techniques like CMOS [3],PTL,DPL etc. However, most of the PTL implementations have two basic problems. First, the threshold drop across the single-channel pass transistors results in reduced current drive and hence slower operation at reduced supply voltages; this is particularly important for low-power design since it is desirable to operate at the lowest possible voltage level. Second, since the "high" input voltage level at the regenerative inverters is not , the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant.

There are many sorts of PTL techniques that intend to solve the problems mentioned above .

1) Transmission gate CMOS (TG) uses transmission gate logic to realize complex logic functions using a small number of complementary transistors. It solves the problem of low logic level swing by using pMOS as well as nMOS.

2) Complementary pass-transistor logic [2] (CPL) features complementary inputs/outputs using nMOS pass-transistor logic with CMOS output inverters. CPL's most important feature is the small stack height and the internal node low swing, which contribute to lowering the power consumption. The CPL suffers from static power consumption due to the low swing at the gates of the output inverters. To lower the power consumption of CPL circuits, LCPL and SRPL circuit styles are used. Those styles contain pMOS restoration transistors or cross-coupled inverters (respectively).

3) Double pass-transistor logic (DPL) uses complementary transistors to keep full swing operation and reduce the dc power consumption. This eliminates the need for restoration circuitry. One disadvantage of DPL is the large area used due to the presence of pMOS transistors.

In this paper an Array multiplier is designed by using GDI (Gate Diffusion Input) technique which consumes less power and also less time to perform multiplication operation. This method is suitable to design fast and low power consumption circuits.

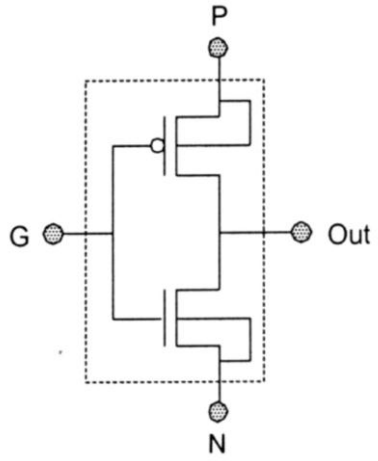
2. Basic GDI Functions

The functionality of GDI method [1] can be understand based on the use of a simple cell as shown in below figure. The cell is look like standard CMOS inverter, but there are some important differences.

1. The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).

2. Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter

The basic cell for GDI is as shown below



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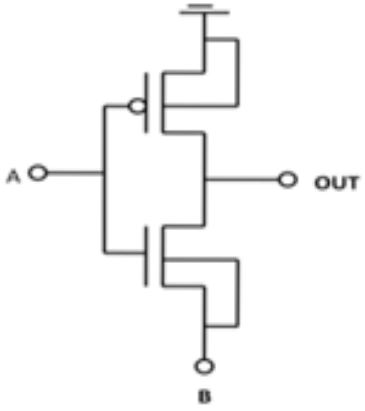
As shown in above figure GDI-Technique has three inputs and those are G,P and N. By simply changing the different input configurations GDI cell corresponds to a number of Boolean functions can be implemented.

2.1. AND GATE



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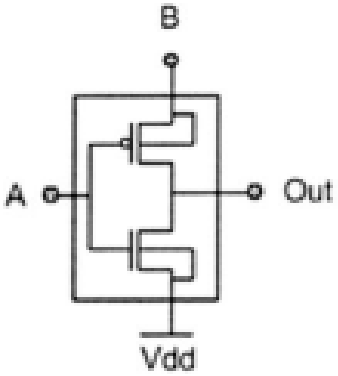
With G=A, P=0 AND N=B the GDI cell will work as 2-input AND gate. The operation table is shown in below.

Table1: operation table for GDI AND gate

A	B	PMOS	NMOS	OUT
0	0	ON	OFF	0
0	1	ON	OFF	0
1	0	ON	OFF	0
1	1	OFF	ON	1

To implement 2-input AND gate, CMOS technology needs 6 transistors (3-PMOS,3-NMOS), where as GDI technique needs only 2-transistors (1-PMOS, 1-NMOS).

2.2. OR GATE



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With G=A, P=B AND N=1 the GDI cell will work as 2-input OR gate. The operation table is shown in below.

Table2: operation table for GDI OR gate

A	B	PMOS	NMOS	OUT
0	0	ON	OFF	0
0	1	ON	OFF	1
1	0	OFF	ON	1
1	1	OFF	ON	1

To implement 2-input OR gate, CMOS technology needs 6 transistors (3-PMOS,3-NMOS), where as GDI technique needs only 2-transistors (1-PMOS, 1-NMOS).

The below table describes implementation of various Boolean functions by altering the inputs.

Table3:Various functions of GDI for different inputs

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

B’	B	A	A’B+AB’	XOR
B	B’	A	AB+A’B’	XNOR

3. Array Multiplier using CMOS Technology

Array multiplier [7] is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added.

Multiplication Algorithm:

If the LSB of Multiplier is ‘1’, then add the multiplicand into an accumulator.

- Shift the multiplier one bit to the right and multiplicand one bit to the left.
- Stop when all bits of the multiplier are zero.
- From above it is clear that the multiplication has been changed to addition of numbers.

If the Partial Products are added serially then a serial adder is used with least hardware. It is possible to add all the partial products with one combinational circuit using a parallel multiplier. However it is possible also, to use compression technique then the number of partial products can be reduced before addition .is performed. The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length.

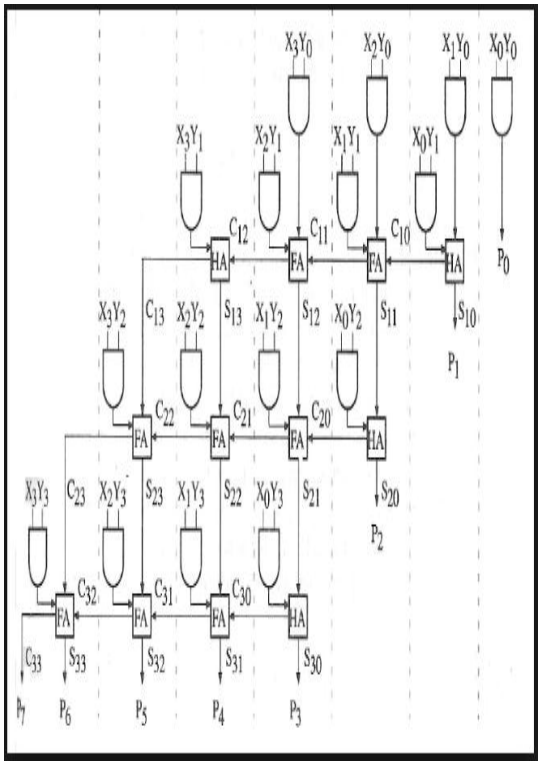

Figure3. Array multiplier

The figure4 shows the 4-bit array multiplier using CMOS technology. The circuit was designed using DSCH Tool.

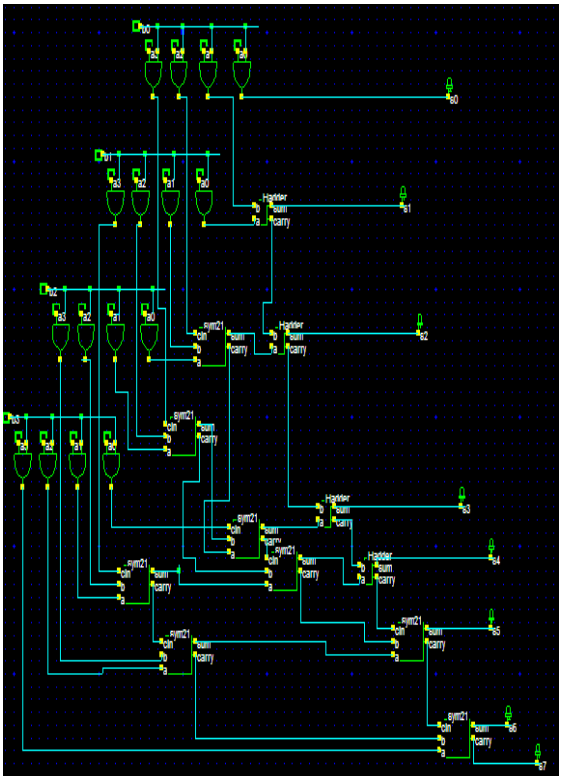

Figure4. Array multiplier using CMOS Technology

4. Proposed Array Multiplier

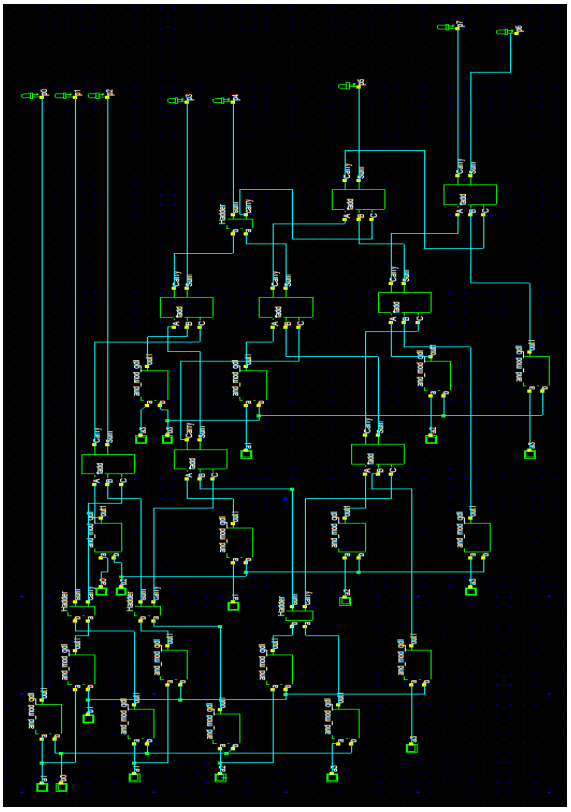

Figure5. Array multiplier using GDI Technology

The above multiplier is designed using GDI Technology[1] which is described in section-2 that is the AND gates and full and half adders are designed using GDI technology. This 4-bit array multiplier using requires less number of transistors when compared with CMOS technology. Since number of transistors are less, this multiplier (Figure5) consumes less power and also the delay is less. This can be proved by following results.

5. Results and Analysis

The circuits in figure4 and figure5 are designed using DSCH tool. The following simulation results are done in MICROWIND tool. The simulation results of figure4 and figure5 are shown in below.

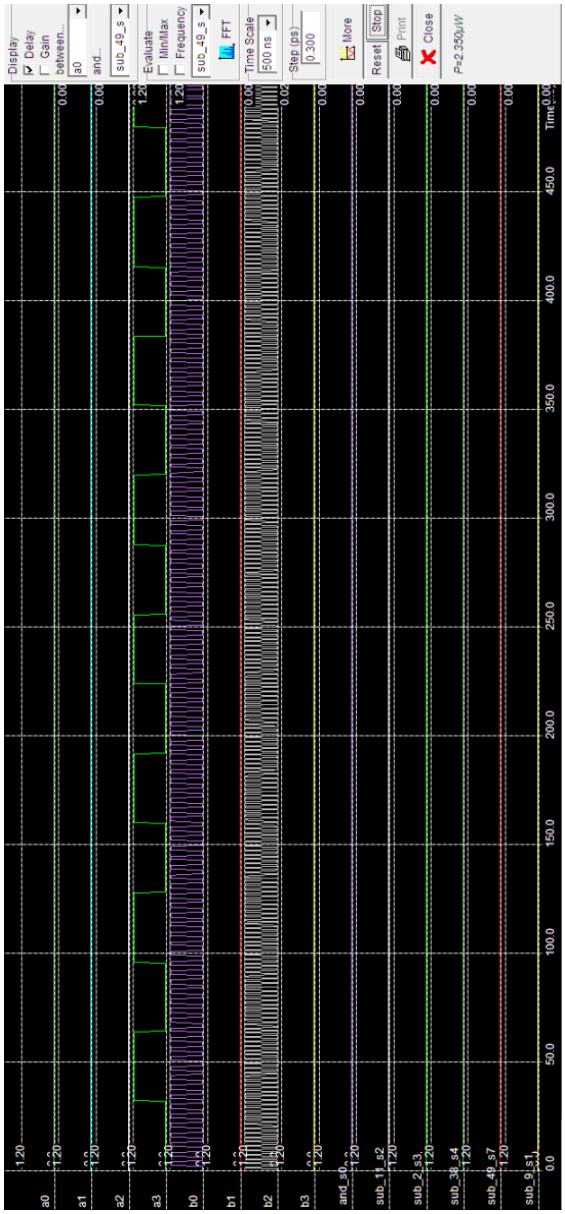

Figure6. Simulation result of Array multiplier using CMOS Technology

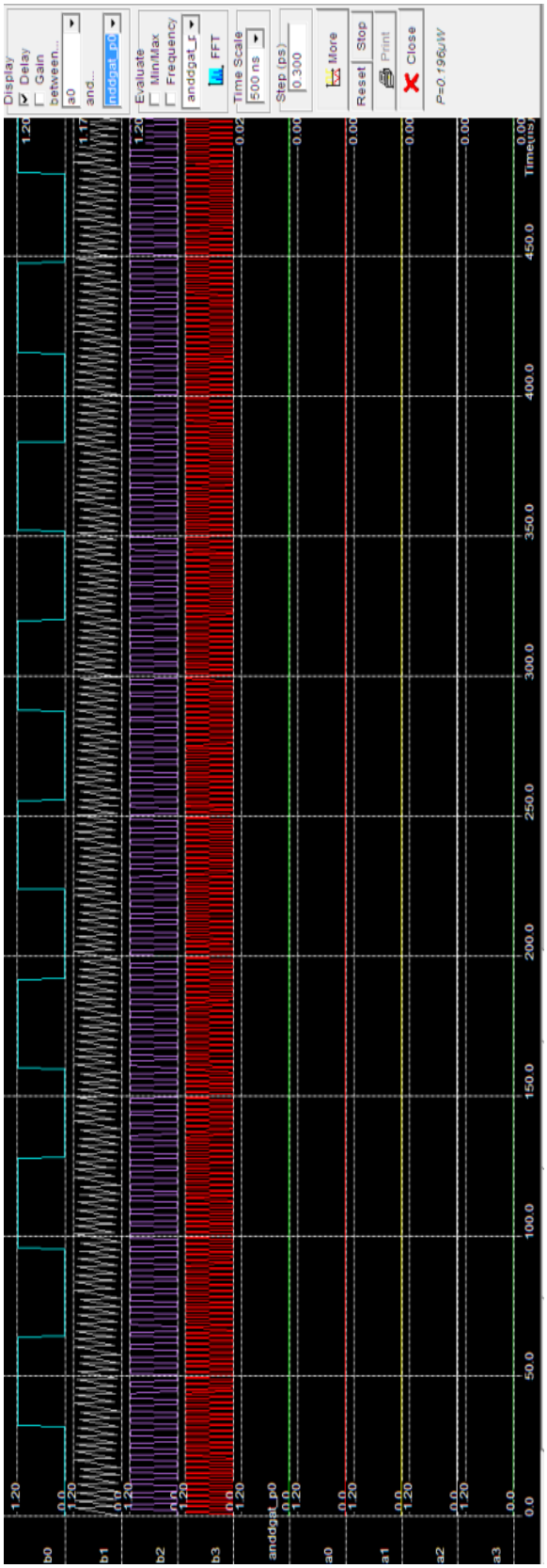

Figure7. Simulation result of Array multiplier using GDI Technology

From the circuits and simulation results of CMOS and GDI technologies the comparative analysis is described in below table

Table4:Comparative analysis of CMOS &GDI Technologies

Type of Adder	Parameter	CMOS	GDI
4-bit Array Multiplier	Total Power dissipation	2.35µw	0.195µw
	Propagation delay	0.30ns	0.265ns
	Transistor count	392	144

By observing the above table, it is clear that GDI Technology reduces the transistor count, propagation delay and total power dissipation compared with CMOS Technology.

6. Conclusion

In this paper, We designed and verified the 4-bit array multiplier using CMOS and GDI techniques. GDI gives better performance compared to CMOS. GDI technique achieves less power consumption, reduced propagation delay and transistor count without losing the functionality of an ideal array multiplier. GDI Technique consumes 0.195µwatts power, produces 0.265nsec and needs 144 transistors for an Array multiplier. Most of the circuits were implemented in regular p-well CMOS process, which casts a limitation on a GDI cell library. Implementations of GDI circuits in SOI or twin-well CMOS processes are expected to supply more power delay efficient design, due to the use of a complete cell library with reduce transistor count.

7. References

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