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Reliable Low Power Multiplier Design Using Reduced Precision Redundancy by Wallace Architecture

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ABSTRACT

In this paper, we have a tendency to propose a reliable low-power multiplier design by adopting Wallace multiplier design to make the reduced precision replica redundancy block (RPR). The projected Wallace multiplier factor design will meet the demand of high precision, low power consumption, and space efficiency. The partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexness of error compensation circuit may be simplified. In a very 12 ×12 bit Wallace multiplier factor, total real time delay and power consumption in our Wallace style may be saved by 22% as compared with the state-of-art ANT Design.

Key Words: *Wallace multiplier, reduced-precision replica (RPR), voltage over scaling (VOS).*

1. INTRODUCTION

The rising of moveable and wireless computing systems in recent years drives the necessity for ultralow power systems. To lower the facility dissipation, offer voltage scaling is wide used as a good low-power technique since the ability consumption in CMOS circuits is proportional to the sq. of offer voltage [1]. However, in deep-sub micrometer method technologies, noise interference issues have raised difficulty to style the reliable and efficient electronics systems; thus, the planning techniques to boost noise tolerance are wide developed [2]–[10]. an aggressive low-power technique, observed as voltage over scaling (VOS), was planned in [4] to lower offer voltage on the far side crucial provide voltage while not sacrificing the outturn. However, VOS ends up in severe degradation in signal-to-noise (SNR). A unique Wallace tree multiplier technique [2] combined VOS main block with reduced-precision duplicate (RPR), that combats soft errors effectively whereas achieving significant energy saving. Therefore

the Wallace tree style idea is more extended to system level in [10]. Another improvement within the multiplier is made by reducing the quantity of partial product generated.

The Wallace tree multiplier factor is one such multiplier; it scans the 3 bits at a time to scale back the quantity of partial product. These 3 bits are: the 2 bit from this pair, and a 3rd bit from the high order little bit of an adjacent lower order try. when examining every triplet of bits, the triplets square measure born-again into a collection of 5 management signals employed by the adder cells within the array to manage the operations performed by the adder cells. to hurry up the multiplication Wallace tree secret writing performs many steps of multiplication directly. From the fundamentals of Wallace Multiplication it is verified that the addition operation is skipped if the ordered bits within the number square measure same. If three consecutive bits square measure same then addition operation is skipped, so in most of the cases the delay related to Wallace Multiplication square measure smaller than that with Array multiplier factor. The rationale is sizable amount of adder cells needed that consumes massive power. However, the RPR styles within the Wallace tree styles of [5]–[7] measure designed in an exceedingly manner, that aren't simply adopted and continual. The RPR styles within the Wallace tree styles of [8] and [9] will operate in an exceedingly in no time manner, however their hardware quality is simply too complicated. As a result, the RPR style within the Wallace style of [2] continues to be the foremost standard style due to its simplicity. However, adopting with RPR in [2] ought to still pay additional space overhead and power consumption. in this paper, we have a tendency to more planned a straightforward approach using the Wallace tree design to exchange fastened -width RPR block in [2].The Wallace methodology, the computation error is corrected with lower power consumption and lower space overhead so as to not increase the crucial path delay, As a result, we are able to understand the design with smaller circuit space, lower power consumption, and lower crucial offer voltage.

2. EXISTING TECHNIQUE

The existing fixed-width RPR to interchange the full-width RPR block within the ant design [2], as shown in Fig. 2, which may not solely give higher computation exactitude, lower power consumption, and lower space overhead in RPR, however additionally perform with higher SNR, a lot of space efficient, lower operative offer voltage, and lower power consumption in realizing the ANT design. We have a tendency to demonstrate our fixed-width

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RPR-based ANT design in Associate in an ANT multiplier. The fixed-width styles square measure typically applied in DSP applications to avoid infinite growth of bit dimension. alienating n-bit least significant bit (LSB) output could be a standard answer to construct a fixed-width DSP with n-bit input and n-bit output. The hardware complexness and power consumption of a fixed-width DSP is sometimes concerning half the full-length one. However, truncation of LSB half ends up in rounding error that has to be compensated exactly. Several literatures [13]–[22] are conferred to cut back the truncation error with constant correction worth [13]–[15] or with variable correction worth [16]–[22]. The circuit complexness to compensate with constant corrected worth will be easier than that of variable correction value; but, the variable correction approaches are typically a lot of to precise.

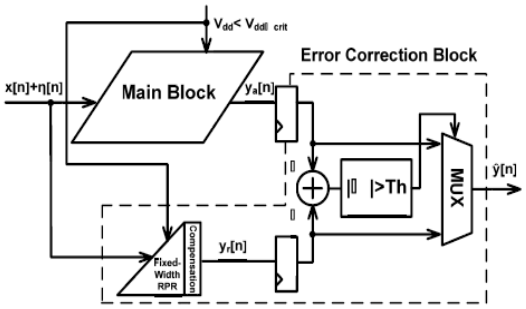

Fig.2.1 Existing ant design with fixed-width RPR.

In [6]–[10], their compensation technique is to compensate the truncation error between the full-length multiplier and therefore the fixed-width multiplier. However, within the fixed-width RPR of an ant multiplier, the compensation error we need to correct is that the overall truncation error of MDSP block. In contrast to [6]–[10], our compensation technique is to compensate the truncation error between the full-length MDSP multiplier and therefore the fixed-width RPR multiplier. In today, there measure several fixed-width multiplier factor styles applied to the full-width multipliers. The error compensation formula makes use of chance, statistics, and simple regression analysis to find the approximate compensation worth [09]. to save hardware complexness, the compensation vector within the partial product terms with the most important weight within the least significant phase is directly inject into the fixed-width RPR, that doesn't need additional compensation logic gates [10]. To further lower the compensation error, we have a tendency to conjointly contemplate the impact of truncated product with the second most significant bits on the error compensation As compared with the full-width RPR style in [10], the projected fixed-width RPR multiplier factor not only performs with higher SNR however conjointly with lower electronic equipment space and lower power

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consumption. Precise Error Compensation Vector for Fixed-Width RPR design within the ant style, the operate of RPR is to correct the errors occurring within the output of MDSP and maintain the SNR of whole system whereas lowering offer voltage., however conjointly accelerate the computation speed as compared with the traditional full-length RPR. However, we need to compensate large truncation error as a result of isolating several hardware components within the LSB a part of MDSP, within the MDSP of n-bit ant Baugh–Woolley array multiplier, its 2 unsigned n-bit inputs of X and Y. Under VOS, there are variety of input-dependent soft errors in its output y_a[n]; but, RPR output y_r[n] continues to be correct since the crucial path delay of the Replica is smaller than T_{samp} [4]. Therefore, y_r[n] is applied to discover errors within the MDSP output ya[n]. Error detection is accomplished by comparison the difference of $|y_a[n]]-\ y_r$[n]| against a threshold Th. Once the difference between y_a[n] and y_r[n] is larger than Th, the output ˆ y[n] is y_r[n] rather than y_a[n]. As a result, ˆ y[n] is expressed as

$$\hat{y}[n] = \begin{cases} y_a[n], & if\ |y_a\,[n] - y_r\,[n]| \le \text{Th} \\ y_{r[n]}, & if\ |y_a\,[n] - y_r\,[n]]| > Th \end{cases}$$

Th is determined by

$$\text{Th} = max_{\forall input}\ |y_o\,[n] - y_r\,[n]|$$

Where y_o[n] is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation

The (n/2)-bit unsigned full-width Baugh–Woolley partial product array will be divided into four subsets, that square measure most significant part (MSP),input correction vector[ICV(β)], minor

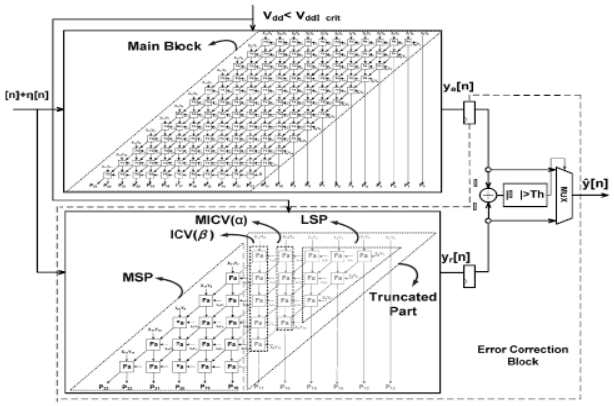

Fig.2.2. 12x12 bit ANT multiplier is implemented with the six-bit fixed width replica redundancy block.

2.1 MAIN BLOCK

FIXED-WIDTH MODIFIED BOOTH MULTIPLIERS:

To reduce the truncation error, first slightly modify the partial product matrix of Booth multiplication and then derive an effective error compensation function that makes the error distribution be more symmetric to and

centralized in the error equal to zero, leading the fixed-width modified Booth multiplier to very small mean and mean square errors. The Baugh-Woolley 12×12 array multiplier is further replace by a signed booth multiplier. Booth's algorithm examines adjacent pairs of bits of the N-bit multiplier Y in signed two's complement representation, including an implicit bit below the least significant bit, y-1 = 0. For each bit y_i, for i running from 0 to N-1, the bits y_i and y_{i-1} are considered. Where these two bits are equal, the product accumulator P is left unchanged. Where y_i = 0 and y_{i-1} = 1, the multiplicand times 2i is added to P; and where y_i = 1 and y_{i-1} = 0, the multiplicand times 2i is subtracted from P. The final value of P is the signed product.

The multiplicand and product are not specified; typically, these are both also in two's complement representation, like the multiplier, but any number system that supports addition and subtraction will work as well. As stated here, the order of the steps is not determined. Typically, it proceeds from LSB to MSB, starting at i = 0; the multiplication by 2i is then typically replaced by incremental shifting of the P accumulator to the right between steps; low bits can be shifted out, and subsequent additions and subtractions can then be done just on the highest N bits of P. There are many variations and optimizations on these details.

FIXED WIDTH RPR

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP and lowering the required s power. In the case of using Fixed-width RPR to realize ANT architecture. This method not only lower Circuit area and power consumption, but also accelerate the computation speed.

The fixed width RPR uses a replica of MDSP output with reduced precision operands. In the MDSP of n-bit ANT Baugh–Woolley array multiplier, its two unsigned n-bit inputs of X and Y can be expressed as

$$X = \sum_{i=0}^{n-1} x_i . 2^i \text{ , } Y = \sum_{j=0}^{n-1} y_j . 2^j$$

The multiplication result P is the summation of partial products of$x_{i,}y_j$, which is expressed as

The (n/2)-bit unsigned full-width Baugh–Woolley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV (β)], minor ICV [MICV (α)], and LSP. Therefore, the other three parts of ICV (β), MICV (α), and LSP are called as truncated part. The truncated ICV (β) and MICV (α) are the most important parts

because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm. To evaluate the accuracy of a fixed-width RPR, the difference between the (n/2)-bit fixed-width RPR output and the 2n-bit full-length MDSP output, which is expressed as

$$\varepsilon = P - P_t$$

Where, P is the output of the complete multiplier in MDSP and P_t is the output of the fixed-width multiplier in RPR. It is noted that β is the summation of all partial products of ICV. By statistically analyzing the truncated difference between MDSP and fixed-width RPR with uniform input distribution, is used to find the relationship between f (EC) and β.

The statistical results show that the average truncation error in the fixed-width RPR multiplier is approximately distributed between β and β+1. More precisely, as β = 0, the average truncation error is close to β +1. As β>0, the average truncation error is very close to β.

For the β>0 case, select β as the compensation vector Where, P is the output of the complete multiplier in MDSP and P_t is the output of the fixed-width multiplier in RPR. It is noted that β is the summation of all partial products of ICV. The statistical results show that the average truncation error in the fixed-width RPR multiplier is approximately distributed between β and β+1. More precisely, as β = 0, the average truncation error is close to β +1. As β>0, the average truncation error is very close to β.

3.PROPOSED METHOD

3.1. INTRODUCTION OF WALLACE MULTIPLIER

Wallace multiplier is extracted form of parallel multiplier [5]. It is slightly faster and requires fewer gates. Different types of schemes are used in parallel multiplier. The Wallace scheme is one of the parallel multiplier schemes that essentially minimize the number of adder stages required to perform the summation of partial products. This is achieved by using full and half adders to reduce the number of rows in the matrix number of bits at each summation stage. Even though the Wallace multiplication has regular and less complex structure, the process is slower in manner due to serial multiplication process. Further, Wallace multiplier is less expensive compared to that of Wallace tree multiplier. Hence, in this paper, Wallace multiplier is designed and analyzed by considering different methods using full adders involving different logic styles.

3.1.1 Implementation of Wallace Multiplier.

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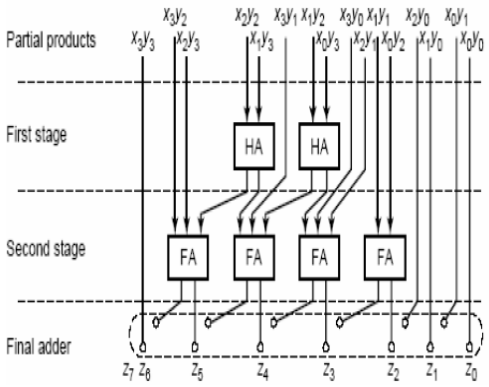
The algorithm of Wallace multiplier is shown in Fig.3.1. The partial product matrix is formed in the first stage by stages which is

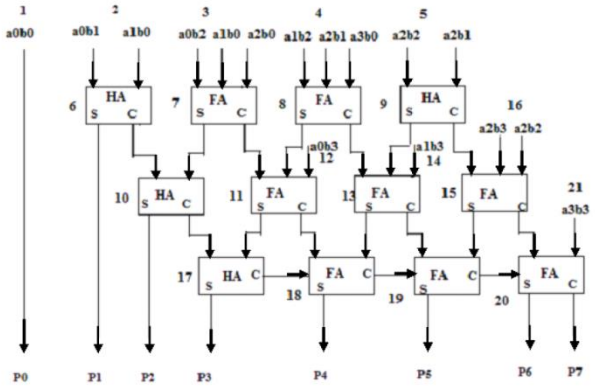


illustrated in Fig.3.2

Fig.3.1 Conventional Wallace tree multiplier

3.1.2 Wallace Tree Multiplier Using Ripple Carry Adder

Ripple Carry Adder is the method used to add more number of additions to be performed with the carry in sand carry outs that is to be chained. Thus multiple adders are used in ripple carry adder. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a C_{in}, which is the Cout of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder. The proposed architecture of Wallace multiplier algorithm using RCA, Take any 3 values with the same weights and gives them as input into a full adder. Partial product obtained after multiplication is taken at the first stage. The data is taken with 3 wires and added using adders and the carry of each stage is added with next two data's in the same stage. At the final stage, same method of ripple carry adder method is performed and thus product terms p1 to p8 is



obtained.

Fig.3.2 generation of product terms

3.2 PROPOSED WALLACE 12 x 12 MULTIPLIER

A reliable low-power multiplier design by adopting Wallace tree multiplier architecture to build the reduced precision replica redundancy block (RPR). The Wallace architecture to replace the fixed-width RPR block in the design using reduced precision redundancy, which can not only provide higher

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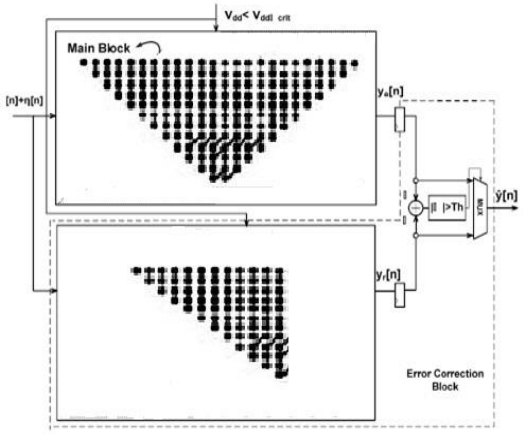
computation precision, lower power consumption, and lower area overhead in RPR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the Wallace architecture.

The main difference between the existing and proposed methods are, replaced the ANT architecture with an Wallace tree architecture with an error compensation circuit. Since the proposed design with error compensation circuit possess less hardware complexity than the ANT multiplier.

In compensation method is to compensate the truncation error between the full-length MDSP multiplier and the Wallace tree multiplier. To further lower the compensation error, also consider the impact of truncated products with the second most significant bits on the error compensation. An error compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, locate the compensation circuit in the noncritical path of the Wallace multiplier. As compared with the fixed-width RPR design, the proposed Wallace tree multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption.

Fig.3.3. implementation of 12x12 bit Wallace multiplier



3.2.1 MAIN BLOCK

It comprises of 12x12 block Wallace multiplier engineering to fulfill ultralow control request, VOS is utilized in MDSP. In any case, underneath the VOS, once the critical way defer prime of the framework ends up bigger than the inspecting sum T_{samp}, the delicate blunders can happen. It brings about serious corruption in flag exactness. Inside the subterranean insect procedure [2], a copy of the MDSP however with decreased exactness operands and shorter calculation delay is utilized as EC square. Under VOS, there are assortment of info subordinate delicate blunders in its yield $y_a[n]$; be that as it may, RPR yield ,keeps on being right since the urgent way postponement of the Replica is littler

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than T_{samp} [4]. Consequently, $y_r[n]$ is connected to find blunders inside the MDSP yield ya[n]. Mistake identification is proficient by correlation the distinction of $|y_a[n]] - y_r[n]|$ against a limit Th. Once the contrast amongst $y_a[n]$ and $y_r[n]$is bigger than Th, the yield ˆ y[n] is $y_r[n]$ instead of $y_a[n]$. Therefore, ˆ y[n] is communicated as

$$\hat{}y[n]= \begin{cases} y_a[n], & if\ |y_a\ [n] - y_r\ [n]| \leq \text{Th} \\ y_{r[n]}, & if\ |y_a\ [n] - y_r\ [n]]| > Th \end{cases} \quad (3)$$

Th is determined by

$$\text{Th}= max_{\forall input} |y_o\ [n] - y_r\ [n]| \quad (4)$$

Where $y_o[n]$ is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation. Along these lines, the power utilization can be incredibly brought down while the SNR can in any case be kept up without extreme corruption. The Wallace tree outlines are typically connected in DSP applications to evade unbounded development of bit width. Cutting off n-bit slightest noteworthy piece (LSB) yield is a well known answer for build a settled width DSP with n-bit info and n-bit yield. The equipment many-sided quality and power utilization of a Wallace tree multiplier in DSP is more often than not about portion of the full-length one. Be that as it may, truncation of LSB part brings about adjusting mistake, which should be remunerated correctly. Numerous writings have been introduced to decrease the truncation mistake with steady adjustment esteem or with variable rectification value.

3.2.2. ERROR CORRECTION BLOCK

In compensation technique is to remunerate the truncation blunder between the full-length MDSP multiplier and the Wallace tree multiplier. To additionally bring down the remuneration blunder, likewise think about the effect of truncated items with the second most critical bits on the mistake pay. A mistake pay circuit utilizing a straightforward minor info revision vector to pay the blunder remained. All together not to expand the basic way delay, find the remuneration circuit in the noncritical way of the Wallace multiplier. As contrasted and the settled width RPR outline, the proposed Wallace tree multiplier performs with higher SNR as well as with bring down hardware region and lower control utilization.

The error correction hunk which comprise of multiplexer, RPR square compensates circuits and registers. In mistake remedy hinder the data sources are given to the

RPR square. The capacity of the RPR piece is to remedy the mistakes happening in the yield. The RPR hunk takes the contribution as halfway items. In the event that the info is 12x12 bits it takes half of the halfway terms or MSB sections. The RPR just takes 6 bits for preparing. Blunder in the yield is limited or truncated. After that the pay circuit to repay the truncated blunders lastly create the information we utilize RPR technique. Commonly the yields are taken to the choice piece. This hunk is utilized for choosing the mistake free creation. Common esteems are contrasted and edge esteem a definitive esteem is shown. In the event that the esteem is more prominent than the edge esteem the RPR esteem is shown or else primary square yield is shown. This yield is considered as a blunder free yield. With the assistance of choice line the multiplier pick the right yield. The variable accuracy esteem is utilized to accomplish great exactness esteem. The information amendment vector is utilized as a part of blunder remuneration circuit for repaying the mistakes. The mistake in the yield is limited.

MULTIPLICATION LOGIC

Considering a case of 12 bit duplication in which 12 bit input is X11X10X9X8X7X6X5X4X3X2X1X0and multiplier 11Y10Y9Y8Y7Y6Y5Y4Y3Y2Y1Y0. The increase procedure is there is the necessity of AND rationales. To start with Y0 is increased with X11X10X9X8X7X6X5X4X3X2X1X0 and results X0Y0, XIY0, X2Y0, X3Y0, X4Y0, X5Y0,X6Y0,X7Y0,X8Y0,X9Y0,X10Y0,and X11Y0. After it Y1 is duplicated with X11X10X9X8X7X6X5X4X3X2X1X0 and results X0Y1, X IY1, X2Y1, X3Y1, X4Y1, X5Y1, X6Y1, X7Y1 X8Y1,X9Y1,X10Y1,and X11Y1,.Similarly all increases are occurred. In each progression there is one parallel move in the resultant rationale. In the process the whole yield of middle of the road compressors is the contribution for next compressors in a similar segment and the created convey for the comparing adders are engendered to next segment adders. A few mainstream and well - known plans, with the goal of enhancing the speed of the parallel multiplier. Wallace presented a critical iterative acknowledgment of parallel multiplier.

The benefit of the Wallace tree is that there are only reduction layers, and each layer has propagation delay. As making the partial products is and the final addition is, the multiplication is only, not much slower than addition (however, much more expensive in the

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gate count). By adding partial products with regular adders would require time. These computations only consider gate delays and don't deal with wire delays, which can also be very substantial. Compare to normal multiplication delay is very low in Wallace multiplication.

Power consumption in the Wallace multiplier is low. Speed is very fast i.e delay and power is inversely proposals to each other.

The advantages and results by considering Wallace multiplier in place of ANT multiplier is given below.

ADVANTAGES

- Delay is very low in Wallace multiplication when compared to normal multiplication.
- Power consumption is low in the Wallace multiplier.
- Very Efficient speed and it is inversely proportional to delay.
- Reduced delay.

3.3 DESIGN SUMMARY

3.3.1 Design summary of ANT multiplier

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	207	768	26%
Number of 4 input LUTs	361	1536	23%
Number of bonded IOBs	132	124	106%

Fig. 3.4. Design Summary of existed 12x12 ANT architecture technique

3.3.2 Design summary of Wallace multiplier

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	200	768	26%
Number of 4 input LUTs	349	1536	22%
Number of bonded IOBs	132	124	106%

Fig. 3.5 .Design Summary of proposed 12x12 Wallace architecture technique

4. SIMULATION RESULTS

This section describes the performance of the proposed design with RTL schematic and output waveforms.

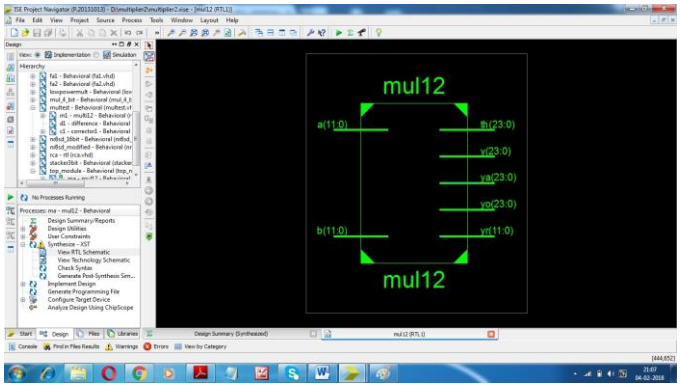

Fig. 4.1. Block Diagram of testing using 12x12 ANT multiplier

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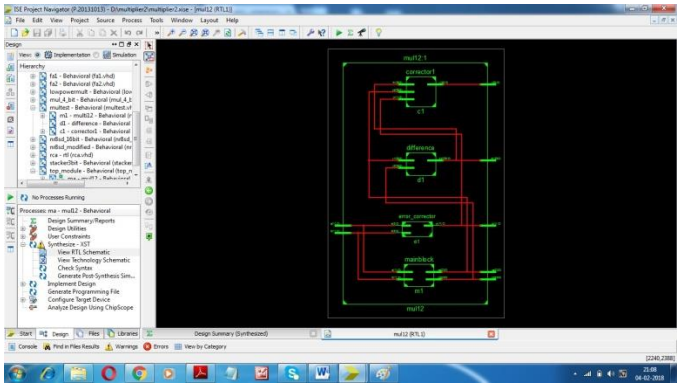

Fig.4.2.RTL Schematic of testing using 12x12 ANT architecture

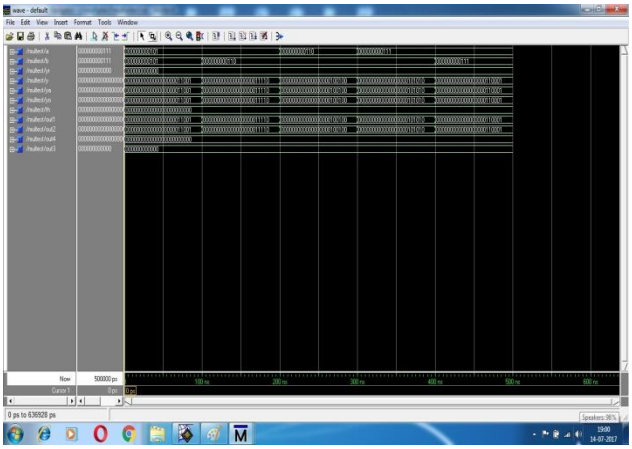

Fig. 4.3 output of testing using 12x12 ANT architecture

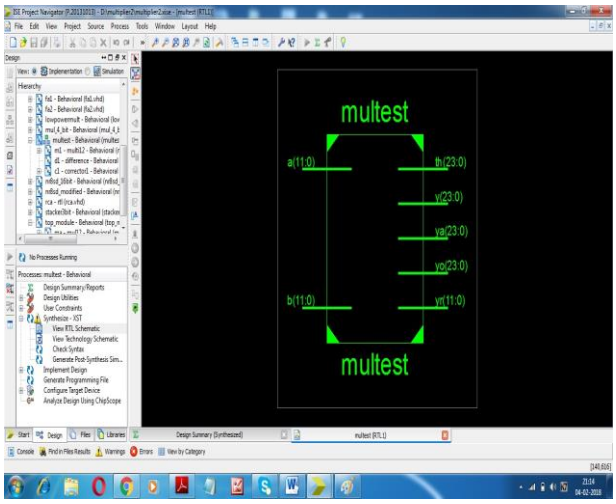

Fig. 4.4. Block Diagram of testing using 12x12 Wallace multiplier

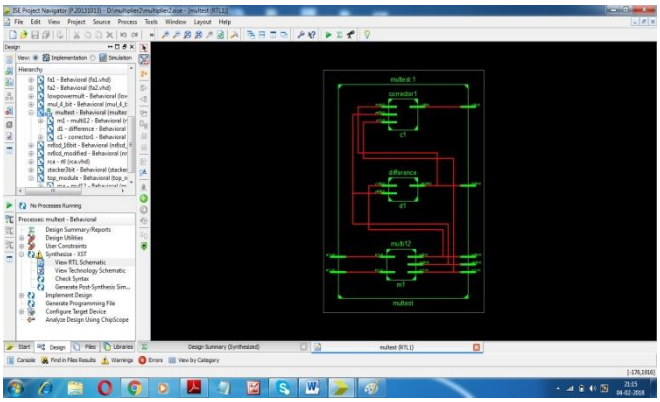

Fig. 4.5. RTL schematic of testing using 12x12 Wallace multiplier

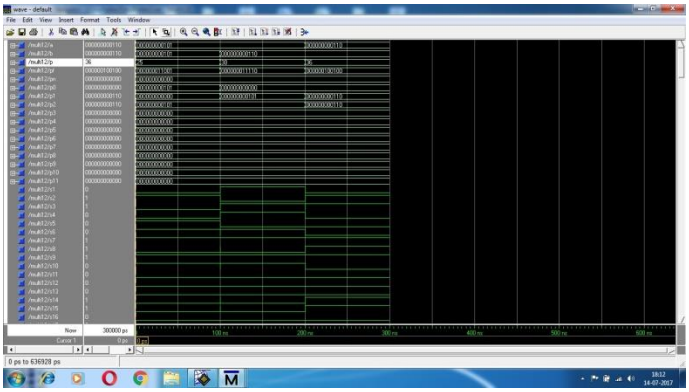

Fig 4.6.output of testing of 12x12 Wallace multiplier

4.1. Table. RESULT ANALYSIS

4.1.1 performance summary of ANT multiplier

4.1.2 performance summary of Wallace multiplier

Parameter	testing using Wallace multiplier
No. of lookup tables	349 out of 1536 - 22%
Total real time delay	13 Sec

5. CONCLUSION

This paper provides a reliable Low power multiplier design RPR using Wallace multiplier design is presented. In proposed system, it also performs error reduction in signed numbers. In reduction phase, 12-bit Wallace tree multiplier was proposed and circuit was implemented and the circuit area and consumption of power in method is saved and the error is also reduced compared to previous methods respectively. The obtained synthesis result confirms that low power and small area applications were found suitable by proposed Wallace tree multiplier. These designs are usually applied in DSP applications, This technique helps in reduction in power delay product may be greatly useful in processing units specifically, digital signal processors.

Parameter	testing using ANT multiplier
No. of lookup tables	361 out of 1536 - 23%
Total real time delay	21sec

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