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A Cascaded Modular Multilevel Inverter Topology Using Novel Series Basic Units with a Reduced Number of Power Electronic Elements

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ABSTRACT

In this investigation, another sort of cascaded modular multilevel inverters (CMMLIs) is exhibited which can create a significant number of output voltage levels with a sensible number of segments. In like manner, every arrangement phase of the proposed CMMLI is contained two same fundamental units that are associated with each other through two unidirectional power switches without pointing any of the full H-bridge cells. Also, since the probability for producing a higher number of output voltage levels in CMMLIs depends on the greatness of the dc voltage sources utilized as a part of every arrangement unit, in whatever is left of this paper, four unique calculations for deciding a fitting an incentive for the dc sources' size are additionally introduced. In the accompanying, a far reaching topological investigation between some CMMLI structures revealed in the writing and proposed structure along with a few reproduction and trial results will be likewise given to approve the lucrative advantages and practicality of the proposed topology.

Key words: Cascade multilevel inverter, Determination of dc voltage sources, Modular multilevel inverter topologies, and reduced number of components.

1. INTRODUCTION

In the field of mechanical power electronic utilities, multilevel voltage source inverters (MLVSIs) offer the promising potential for use in medium and high power applications because of their different notable highlights, for example, low voltage weights on switches, low total harmonic distortion (THD) of the output waveforms, no requirement for vast output filters or transformers, and minimal effort [1].

When all is said in done there are three sorts of MLVSIs. These are the diode clamped MLVSIs [5], flying capacitor MLVSIs also, fell H-bridge MLVSIs. Notwithstanding, these customary composes dependably

experience the ill effects of requiring a substantial number of energy electronic segments, disconnected dc voltage sources and charge adjusting control techniques which can increment the general working and upkeep costs.

These days, with a specific end goal to reduce the previously mentioned restrictions, numerous structures have been displayed in the writing. They have tended to the rise of the output voltage levels through the minimization of the general expenses by with respect to the essential idea of MLVSIs. Subsequently, a few new essential units were recommended which can fill in as a level maker sub-unit. These proposed essential units are associated with a full H-bridge unit for changing the voltage extremity of the output waveform and after that these modules are fell with each other in arrangement shape to produce various output voltage levels. Also, fell association of arrangement essential units offers the measured quality property which can strengthen the dependability and adaptability of system. Since cascaded modeled multilevel inverters (CMMLI) can normally produce any coveted number of higher output voltage levels, the estimation of the dc voltage sources which can be given from a few renewable energy source assets (REs) can be seen either symmetric or asymmetric. In the symmetric structures, the sizes of the dc voltage sources are same. In this way, the assortment of disengaged dc voltage sources is low which makes them more appropriate for cost compelling force electronic applications.

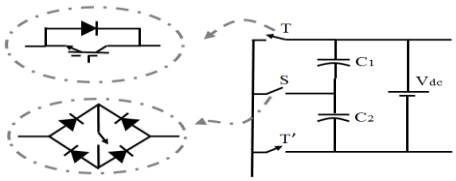

Fig.1. Proposed basic unit.

Then again, these dc voltage esteems can be chosen to be diverse in the uneven setups. For this situation, despite the fact that the assortment of disconnected dc voltage sources is high, the number of produced output voltage levels is significantly more than the symmetric structures which endeavors to accomplish a superior control quality through a lower estimation of the THD and a diminished number of energy electronic components. By and by, utilizing an extra full H-bridge unit in the new created MLVSIs as a rule prompts an expansion in the number of energy switches and in the most extreme number of current way parts which can upgrade the aggregate

conduction misfortune and debase the general proficiency consequently.

The point of this paper is to diminish the general segment check of CMMLIs through showing a novel topology which does not require a traditional full H-bridge cell for evolving the output voltage extremity and can enhance the adaptability of the framework by the commitment of the capacitive divider procedure connected on the dc-joins. Along these lines, whatever remains of this investigation is sorted out as takes after. At initial, another essential particular MLVSI topology is introduced which is involved six unidirectional and two bi-directional power switches, two disengaged dc voltage sources furthermore, four capacitors as the dc connect vitality sharing components in the power circuit. For this situation, the four used capacitors are charged and released every now and again amid the positive and negative half cycles of the output waveform by control supply self-voltage adjusting.

II. PROPOSED MLVSI TOPOLOGY

The principle segment of the proposed particular MLVSI topology named as the proposed essential unit is appeared in Fig. 1. As can be seen, the proposed fundamental unit comprises of one dc voltage source, two capacitors as dc connect vitality sharing components, and one bi-directional and two unidirectional power switches which ought to be activated by correlative activities to maintain a strategic distance from impede. For this situation, the bi-directional power switch can be substituted by one common power switch and four power diodes to attempt the conduction of the switch current in the two bearings. To exhibit the working methods of the proposed essential unit, the present stream way of four passible output voltage states are shown in Fig. 2(a)- (d). As indicated by Fig. 2(a) and (b), when either the switch of T or on the other hand $\grave{T}$ is tuned ON and S turns into off, the voltage of the dc source ($+V_{DC}\ or - V_{DC}$) is transferred to the output. At this organize, none of the dc interface capacitors go into the current way and subsequently both two are directly charged by control supply.

Likewise, as indicated by Fig. 2(c) and (d), when S moves toward becoming ON and switches T or $\grave{T}$ OFF, the across voltage of $C_1\ or\ C_2$ are pumped to the output. Here, when the across voltage of one gathered capacitor ($C_1\ or\ C_2$) is being pumped to the output, another capacitor is directly charged by the power supply.

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The proposed MLVSI topology appeared in Fig. 3(a) is made by the commitment of the presented essential unit. Here, to make an ideal structure of a MLVSI as far as having the least number of switching devices with most noteworthy number of created output voltage levels, two same fundamental units with inverse polarities are utilized as a part of the proposed general structure rather than utilizing a full H-bridge unit in the front of the proposed essential unit. Table I shows the seventeen extraordinary ON switching conditions of the proposed topology in which C and D remain for the charging and releasing methods of the capacitors, separately. Furthermore, V_{C1}, L , V_{C2}, L , V_{C1}, R *and* V_{C2}, R are the across voltages of the capacitors C_1, L , C_2, L , C_1, R *and* C_2, R respectively.

In the mean time, V_{dc}, L *and* V_{dc}, R signify the required dc voltage sources situated at the left and right half of the circuit, separately. For this situation, to keep away from impede, the matched switches (T $\acute{T}$) , (T_R , $\acute{T_R}$) and (T_L , $\acute{T_L}$) ought not be turned ON, all the while.

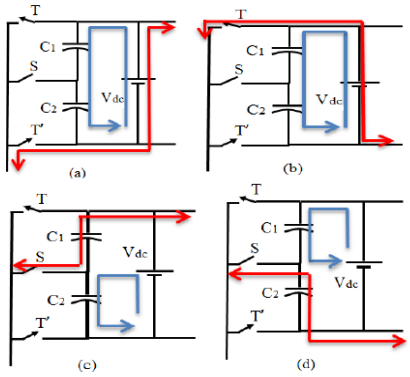

Fig.2. Different current flow path of operating modes for proposed basic unit when (a) -*Vd c* (b) $+V_{dc}$ (c) across voltage of C_1 (d) across voltage of C_2 is transferred to the output.

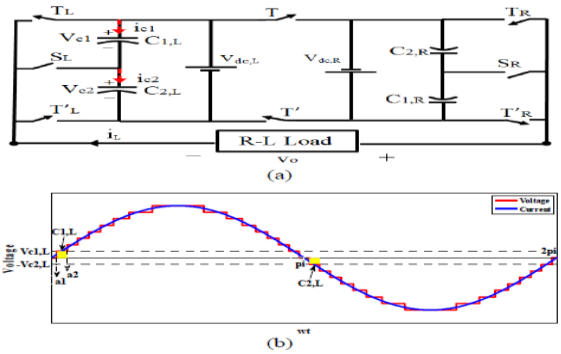

Fig.3. (a) Proposed MLVSI topology (b) Typical output voltage and current waveforms of proposed topology.

Fig. 3(b) indicates average output voltage and current waveforms of the proposed topology in light of a 50Hz exchanging recurrence. For this situation, two used dc voltage sources are thought to be non-measure up to and a resistive-inductive stack has been associated at the output of the proposed topology. At this stage, to show

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the precise self-charge adjusting activity of capacitors in the proposed topology, the capacitance for the greater part of the capacitors are thought to be the same and equivalent to C . In this way, by thinking about the time

TABLE I DIFFERENT SWITCHING AND CAPACITORS' STATES FOR ROPOSED MLVSI

States	ON-STATE SWITCHES	Cap States				v_o
		$C_{1,L}$	$C_{2,L}$	$C_{1,R}$	$C_{2,R}$	
1	(T_L,T,T_R) / (T_L',T',T_R')	C	C	C	C	0
2	(S_L,T,T_R)	D	C	C	C	$V_{C1,L}$
3	(T_L',T,T_R)	C	C	C	C	$V_{dc,L}$
4	(T_L,T,S_R)	C	C	C	D	$V_{C2,R}$
5	(S_L,T,S_R)	D	C	C	D	$V_{C1,L}+V_{C2,R}$
6	(T_L',T,S_R)	C	C	C	D	$V_{dc,L}+V_{C2,R}$
7	(T_L,T,T_R')	C	C	C	C	$V_{dc,R}$
8	(S_L,T,T_R')	D	C	C	C	$V_{C1,L}+V_{dc,R}$
9	(T_L',T,T_R')	C	C	C	C	$V_{dc,L}+V_{dc,R}$
10	(S_L,T',T_R')	C	D	C	C	$-V_{C2,L}$
11	(T_L,T',T_R')	C	C	C	C	$-V_{dc,L}$
12	(T_L',T',S_R)	C	C	D	C	$-V_{C1,R}$
13	(S_L,T',S_R)	C	D	D	C	$-V_{C2,L}-V_{C1,R}$
14	(T_L,T',S_R)	C	C	C	D	$-V_{dc,L}-V_{C1,R}$
15	(T_L',T',T_R)	C	C	C	C	$-V_{dc,R}$
16	(S_L,T',T_R)	C	D	C	C	$-V_{C2,L}-V_{dc,R}$
17	(T_L,T',T_R)	C	C	C	C	$-V_{dc,L}-V_{dc,R}$

interim of (α_1 , α_2) in Fig. 3(b) and concerning Table I, the voltage varieties of the capacitor C_1, L for the first positive advance of the output voltage can be communicated as:

$$\Delta V_{\substack{C1,L \\ <\alpha_1,\alpha_2>}} = \frac{1}{C}\int_{\alpha_1}^{\alpha_2} i_{C,1L}(t)\,dt = -\frac{1}{C}\int_{\alpha_1}^{\alpha_2} i_L(t)\,dt \qquad (1)$$

Where, ,$i_{C1}, L(t)$ is the passing current of C_1, L and $i_L(t)$ is expected to be a sinusoidal load current which can be communicated as:

$$i_L(t) = I_m \sin(\omega t - \varphi) \qquad (2)$$

Where I_m , ω *and* φ the sufficiency of load current, the rakish recurrence of the output voltage and the stage contrast between the heap voltage and the current waveforms, individually. Then again, by applying the Kirchhoff voltage law (KVL) in the left circle of the converter, clearly:

$$V_{C1,L} + V_{C2,L} = V_{dc,L} \qquad (3)$$

In this manner, the voltage variety of the capacitor C_2, L is continuously equivalent to the contrary estimation of the voltage variety of the capacitor C_1, L or as it were:

$$\Delta V_{C1,L} = -\Delta V_{C2,L} \qquad (4)$$

What's more, by utilizing (4) and as per Fig. 3(b), the voltage varieties of the capacitors for the time interim of ($\alpha_1 + \pi$, $\alpha_2 + \pi$) in the primary negative advance of the output voltage can be taken by:

$$\Delta V_{\substack{C1,L \\ <\alpha_1+\pi,\alpha_2+\pi>}} = -\Delta V_{C2,L} = -\frac{1}{C}\int_{\alpha_1+\pi}^{\alpha_2+\pi} i_{C,2L}(t)\,dt = -\frac{1}{C}\int_{\alpha_1+\pi}^{\alpha_2+\pi} i_L(t)\,dt \qquad (5)$$

where, ,2 ( ) C L I t is the passing current of 2,L C . From the sinusoidal presumption of the heap current as indicated by (2) and

having considered (1) and (5), the voltage varieties of 1,L C amid the age of the principal output voltage level in both the positive and negative half cycles is equivalent to zero, as indicated by (6):

$$\Delta V_{\substack{C1,L \\ <\alpha_1,\alpha_2>}} + \Delta V_{\substack{C1,L \\ <\alpha_1+\pi,\alpha_2+\pi>}} = 0 \qquad (6)$$

In the mean time in the main output voltage level in both half cycles, two different capacitors from the correct side of the circuit are being charged independently by another dc control supply. Regarding this examination, the crosswise over voltage of each capacitor is adjusted at the underlying voltage esteem in the zero output voltage level which is equivalent to $\frac{V_{dc}}{2}$.

A comparable examination can be refined for each of the output voltage levels and for every one of the capacitors. The aftereffect of this conduct is that the proposed circuit can settle the voltage of the capacitors at the half estimation of the dc voltage sources since the capacitive divider system and this task don't rely upon the esteem or kind of burdens. Presently, keeping in mind the end goal to expand the quantity of output voltage levels what's more, to characterize the general secluded structure, the proposed CMMLI is made by Fig. 4. In such manner, if n is thought to be the quantity of the proposed MLVSI units associated with each other by arrangement association, the output voltage of the proposed CMMLI can be acquired by:

$$V_O(t) = v_{o,1}(t) + v_{o,2}(t) + \ldots + v_{o,n}(t) \qquad (7)$$

Likewise, the quantity of required power switches or required entryway drivers and the quantity of required dc voltage sources, dc-connect capacitors and the greatest number of switches in the present way for proposed CMMLI are computed by the accompanying conditions, separately:

$$N_{Switch} = N_{Driver} = 8n \qquad (8)$$

$$N_{Source} = 2n \qquad (9)$$

$$N_{Cap} = 4n \qquad (10)$$

$$N_{C,\max} = 3n \qquad (11)$$

III. PROPOSED ALGORITHMS TO DETERMINE THE Management OF DC VOLTAGE SOURCES

In this area, to decide a reasonable size for the dc voltage wellsprings of the proposed CMMLI topology, four diverse passible calculations are exhibited. Also, the number of created output voltage levels, the most extreme estimation of the output voltage, the assortment of the confined dc voltage sources and the aggregate estimation of the

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blocked voltage are figured for every one of them.

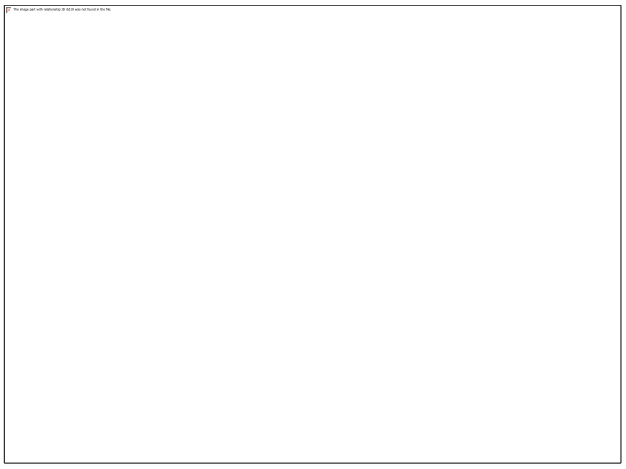

Fig.4. Proposed CMMLI topology.

A. Initially Proposed Algorithm

In the principal calculation, the extent for the greater part of the dc voltage sources is thought to be the same (symmetric calculation) and equivalent to:

$$V_{dc,Li} = V_{dc,Ri} = 2V_{dc} \quad for(i = 1,2,...,n) \qquad (12)$$

Obviously the assortment of confined dc voltage sources based on the proposed symmetric calculation is one. In this manner, the number of output voltage levels and the most extreme estimation of the output voltage are communicated as (13) and (14), separately.

$$N_{level} = 8n + 1 \qquad (13)$$

$$V_{o,\max} = 4nV_{dc} \qquad (14)$$

Another basic parameter which generally impacts the general cost capacity of an inverter is the aggregate estimation of the greatest blocked voltage over the switches in their OFF state condition. Along these lines, this esteem is figured by the following conditions for the greater part of the included switches in the proposed CMMLI in light of the main proposed strategy.

$$V_{Block,T_i'} = V_{Block,T_i} = 4V_{dc} \qquad (15)$$

$$V_{Block,T_{Li}'} = V_{Block,T_{Li}} = V_{Block,T_{Ri}'} = V_{Block,T_{Ri}} = 2V_{dc} \qquad (16)$$

$$V_{Block,S_{Li}} = V_{Block,S_{Ri}} = \pm V_{dc} \qquad (17)$$

$$V_{Block} = 2\sum_{i=1}^{n}(V_{Block,T_i} + V_{Block,T_{Li}} + V_{Block,S_{Li}}) = 18nV_{dc} \qquad (18)$$

B. Second Proposed Algorithm

The second proposed calculation is devoted to the parallel design for the size of the dc voltage sources in each arrangement unit, which can be composed by (19):

$$V_{dc,Ri} = 2V_{dc,Li} = 2 \times 13^{n-1}V_{dc} \quad for(i = 1,2,...,n) \qquad (19)$$

Consequently, the quantity of output voltage levels, the greatest estimation of the output voltage, the most extreme estimation of the blocked voltage and the assortment of the detached dc voltage sources are computed by the accompanying conditions:

$$N_{level} = 13^n \qquad (20)$$

$$V_{o,\max} = \frac{(13^n - 1)}{2}V_{dc} \qquad (21)$$

$$V_{Block} = 9 \times (\frac{13^n - 1}{4})\,V_{dc} \qquad (22)$$

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$$N_{Variaty} = 2n \quad (23)$$

C. Third Proposed Algorithm

The extent of the dc voltage sources in every arrangement unit of the proposed CMMLI can be balanced as a trinary design in third proposed calculation, as indicated by (24):

$$V_{dc,Ri} = 3V_{dc,Li} = 2\times 17^{n-1}V_{dc} \quad for(i = 1,2,...,n) \quad (24)$$

$$N_{level} = 17^n \quad (25)$$

$$V_{o,\max} = \frac{(17^n - 1)}{2}V_{dc} \quad (26)$$

$$V_{Block} = 9\times(\frac{17^n - 1}{4})\,V_{dc} \quad (27)$$

$$N_{Variaty} = 2n \quad (28)$$

D. Fourth Proposed Algorithm

In the fourth proposed calculation, the extent of the dc voltage sources utilized as a part of every unit is balanced in the symmetric shape. These qualities are distinctive in contrast with the other units in the proposed CMMLI and can be set in view of (29):

$$V_{dc,Ri} = V_{dc,Li} = 2\times 9^{n-1}V_{dc} \quad for(i = 1,2,...,n) \quad (29)$$

For this situation, the related conditions, similar to those of the other proposed calculations, are ascertained and can be communicated as:

TABLE II

SYMMETRIC COMPARISON BETWEEN PROPOSED CMMLI AND OTHER TOPOLOGIES FOR 25 *level N*

Paramaters					
No. Refs	N_{Switch} & N_{Driver}	N_{Source}	$N_{C,\max}$	V_{Block}	CF
[12]	30	12	12	$54V_{dc}$	1620
[14]	36	6	24	$60V_{dc}$	1080
[20]	26	12	13	$48V_{dc}$	1248
[21]&[25]	36	12	12	$60V_{dc}$	2160
[22]	36	12	24	$48V_{dc}$	1728
First top [26]	28	6	14	$72V_{dc}$	1008
Second top [26]	48	6	24	$72V_{dc}$	1728
Proposed CMMLI	24	6	9	$54V_{dc}$	648

$$N_{level} = 9^n \quad (30)$$

$$V_{o,\max} = \frac{(9^n - 1)}{2}V_{dc} \quad (31)$$

$$V_{Block} = 9\times(\frac{9^n - 1}{4})\,V_{dc} \quad (32)$$

$$N_{Variaty} = n \quad (33)$$

At this stage, with a specific end goal to assess the three assumed asymmetric algorithms calculations for the proposed CMMLI topology, varieties of the quantity of required power switches, the number of required dc voltage sources and the assortment of separated dc voltage sources versus distinctive quantities of output voltage levels have been appeared based on Fig. 5(a)- (c).

Moreover, the resulting previously mentioned parameters which can gauge the general working expense of the framework are functionalized as indicated by (34). This condition is inferred from the characterized cost work (CF) displayed in [14]. At that

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point its separate varieties are appeared by Fig. 5(d). Here, the per unit estimation of the aggregate blocked voltage (pu Piece V) can be signified by (35).

$$CF = (\mathrm{N}_{Switch}) \times (\mathrm{N}_{Source}) \times (\mathrm{N}_{Variaty}) \times (V_{Block}{}^{pu}) \quad (34)$$

$$V_{Block}{}^{pu} = \frac{V_{Block}}{V_{o,\max}} \quad (35)$$

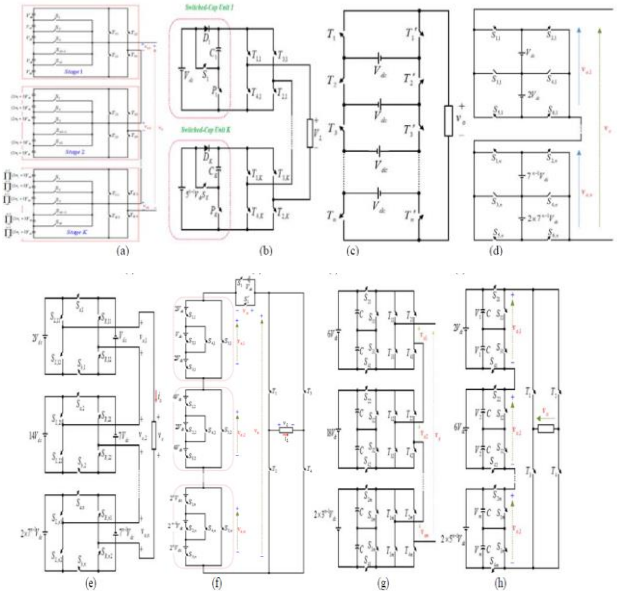

Fig.6. Suggested CMMLI topologies.

It ought to be noticed that, the estimations of the blocked voltages for each of the proposed calculations, as far as number of output voltage levels, are constantly equivalent to each other and can be composed as:

$$V_{Block} = \frac{9 \times (N_{level} - 1)}{4} \quad (36)$$

By considering these figures, obviously the third proposed calculation offers the better condition in difference to others and since it can limit the cost, this calculation would be chosen as the fundamental proposed awry structure for the correlation done in the following area.

CONCLUSION

In this paper, to create a higher number of output voltage levels with decreases in the parts include and the other essential power electronic parameters of the fell particular multilevel inverters (CMMLIs), another topology was exhibited in which does not require any H-bridge cells in every arrangement unit to turn the output voltage extremity. Henceforth, every arrangement unit of the proposed CMMLI is made out of two disconnected dc voltage sources, four capacitors and eight entryway drivers. For this situation, the majority of the dc connect capacitors are specifically charged by control supplies without using any confounded control procedures. What's more, so as to accomplish an alternate number of output voltage levels, four distinct calculations for deciding the extent of the dc voltage sources were proposed. A far reaching examination from various perspectives affirms the upsides of the proposed structure in correlation with a few as of late exhibited CMMLIs. Finally, the viability and right execution of proposed 17-

level and 81-level determined topologies have been checked by reenactment and trial comes about.

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