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High-Speed and Energy-Efficient Gray Mapping Polar Codes

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ABSTRACT: A significant attention has received for polar codes due to their capacity-achieving performance and low encoding and decoding complexity. Successive cancellation decoding (SCD) and belief propagation decoding (BPD) are the two popular approaches for decoding polar codes. SCD is having less computational complexity when compared with BPD, but suffers from long latency due to the serial nature of the SC algorithm. BPD is parallel in nature and is more attractive for low-latency applications. However, due to the iterative nature of BPD, the required latency and energy dissipation increase linearly with the number of iterations. In this paper presents an efficient multi-strategy ECC scheme called pre-check scheme which consists of hard, quantized-soft, and pure-soft decoders geared to MLC NAND flash memory based on polar code. The hard decoder is designed to correct the majority of erroneous codewords in the initial phase of the flash memory, while the soft decoders aim to correct codewords which contain larger amount of errors. In addition, we clarify that the mapping scheme using Gray code can achieve best performance compared to other alternatives.

INDEX TERMS: Belief propagation decoding (BPD), energy efficiency, factor graph, iterative decoders, polar codes, successive cancellation decoding (SCD).

I.INTRODUCTION

Different capacity-approaching codes, such as Turbo codes and low-density parity-check (LDPC) codes have been designed and used for some time in applications, such as wireless communication and data storage, to achieve very high data rates. Recently, the first provable capacity-achieving codes, called polar codes, were invented by Arikan. Being the first family of codes known to achieve the channel capacity with explicit construction, polar codes have attracted a lot of attention since their invention. Polar codes have been proved to achieve the capacity for binary-input symmetric memory less channels as well as discrete and continuous memory less channels.

Additionally, an explicit construction method for polar codes has been given and it is shown that they can be efficiently encoded and decoded with complexity O (n log n), where n represents the code length. Several decoding methods for polar codes have been proposed and among these, successive cancellation decoding (SCD) and belief propagation decoding (BPD) are the two most popular methods. Due to the serial nature of the algorithm, SCD suffers from long latency, although it requires less computation as compared with BPD. Several methods have been proposed for reducing the latency of SC decoders to achieve a high throughput. In addition, list decoding and stack decoding, which are depends on SCD has been proposed for improving the error-correcting performance for polar codes with short code lengths.

Polar BP decoders have the intrinsic benefit of parallel processing. Therefore, polar BP decoders are more attractive when compared with their counterparts of SC, for low-

latency applications. Hence, due to their iterative nature, the required latency and energy dissipation of BP decoders maximizes linearly with the number of iterations. The requirement of a large number of iterations results in high computation complexity, and hence makes BPD less attractive than its SC counterpart. To reduce the cost of area, a memory efficient BP decoder was proposed by Sha *et al.* based on the idea of combining two adjacent stages of a BPD factor graph. To reduce the complexity of computation, another decoding method, called soft cancellation (SCAN) decoding, was existed.

In the decoding process, by restricting the soft information propagation schedule the computational complexity of SCAN is much lower than that of BPD. However, different from BPD, the SCAN operation is serial in nature which leads to a much longer decoding latency. Based on the SCAN decoder, another decoding algorithm known as reduced complexity soft cancelation (RCSC) was proposed to reduce the BPD complexity. RCSC requires significantly less memory for storing log-likelihood ratios (LLRs) as compared with the SCAN decoder, and by eliminating the unnecessary additions, it also requires fewer computations. However, similar to the SCAN decoder, RCSC suffers from latency of long decoding. In this paper, we present design of a low-latency polar codes decoder, and hence, we concentrate on the implementation of parallel BPD.

II.EXISTED SYSTEM

Polar Codes and Belief Propagation Decoding: Polar codes are a linear block code which depends on the phenomenon of channel polarization, in which individual channels are recursively combined and split, such that their mutual information tends toward either 1 or 0. In other words, some of these channels become completely noise-free, while the others become completely noisy. Furthermore, the fraction of noiseless channels tends toward the capacity of the underlying binary symmetric channels.

Connected Sub factor Graph Freezing (CSFG) Concept: The existed BP decoding scheme is based upon a CSFG freezing concept to achieve lower complexity. At a particular iteration t, if a CSFG at stage j can correctly decode its corresponding constituent code, it is frozen and no message passing or updating within the CSFG will be needed in the subsequent iterations. The details of how to check whether a CSFG can be frozen will be presented later. When the decoding reaches a certain stage, its CSFGs are checked for freezing. If the CSFG cannot correctly decode its constituent code, then it cannot be frozen and the message passing and updating are executed by the PEs at that stage. After that, we move to the next stage and check the convergence of the corresponding CSFGs. When we move to the next stage, the number of CSFGs is doubled. This procedure of freezing checking is continues from stage to stage till the end of the BPD factor graph is reached.

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Checking Order for CSFGs: The order of checking the freezing of CSFGs at a stage is significant to the operation of the existed scheme. Here, we borrow an idea from SCD, where the results of the previously decoded bits are used for the decoding of the current bit. Similar to the SCD operation, the decoded result of a constituent code associated with a frozen CSFG will be useful in decoding the constituent codes of the subsequent CSFGs in the next few iterations. Hence, the freezing order of the CSFG has to follow the order of decoded bit and the top CSFGs at each stage will be frozen first. A CSFG can only be checked for freezing if all the previous CSFGs (in the order of the decoded bits) at that stage have already been frozen.

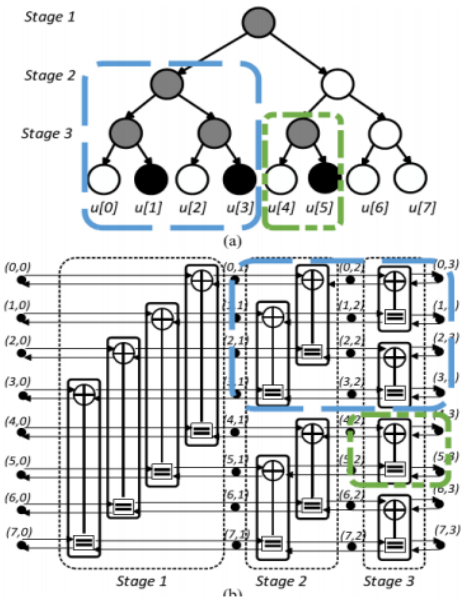

FIGURE 1: CORRESPONDENCE BETWEEN SCD SCHEDULING TREE AND BPD FACTOR GRAPH. (A) SUB TREES IN SCD SCHEDULING TREE (TOP). (B) CSFG'S IN BPD FACTOR GRAPH (BOTTOM)

Fig. 1 shows the SCD scheduling tree and the factor graph of polar code. We can seen that the top CSFGs at the various stages which corresponds to the first few sub trees that resulted from the depth-first traversal of the SCD scheduling tree.

III.PROPOSED SYSTEM

The functional diagram of information storage in SSD is shown in Fig. 2. The external data sent by users are processed in operating system at first to transform into binary bits and then encoded by polar encoder. After encoding, these bits are sequentially mapped into voltages pairwise per cell to be stored. When information is read out, the threshold voltages will be sensed by detector and translated into corresponding digital information according to the adopted decoder.

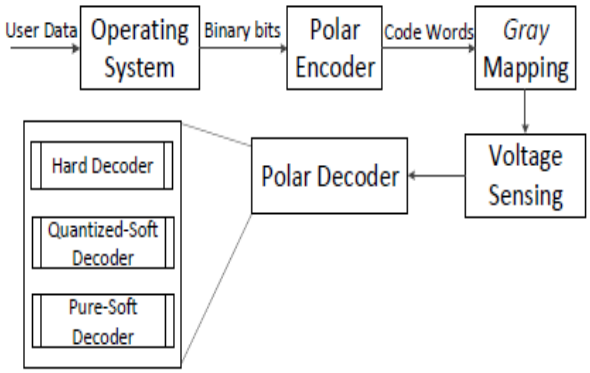

FIG 2. BLOCK DIAGRAM OF PROPOSED SYSTEM

Before sensing voltages, the detector will first check the cell state to ensure the worsening (distortion) of the voltage condition presumed as a Gaussian

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distribution which is called pre-check scheme. The pre-check scheme can choose an optimum decoder according to the degree of cell distortion to satisfy performance requirements of the system. After this procedure, sensed voltages will be processed into different kinds of input information and sent to corresponding decoders.

On the basis of pre-check scheme, we can select an optimum decoder according to the worsening condition of each cell. When overlapped regions are small or even non-existent, the hard or quantized-soft decoder is chosen since their decoding latency is short. When cell distortion is getting worse, soft information which contains larger amount of information than previous hard and quantized-soft information will be fed to pure-soft decoder for better performance with longer decoding latency. With reasonable arrangement based on system requirement, most codewords will be decoded in first 2 decoders to improve reading speed.

IV.RESULTS

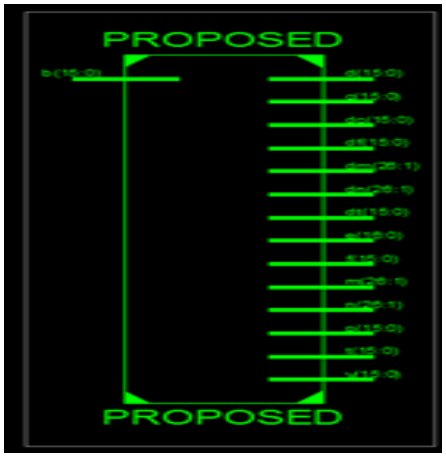

FIG 3. RTL SCHEMATIC

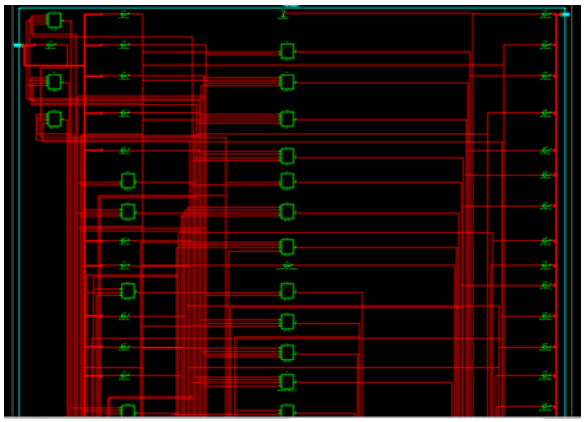

FIG 4. TECHNOLOGY SCHEMATIC

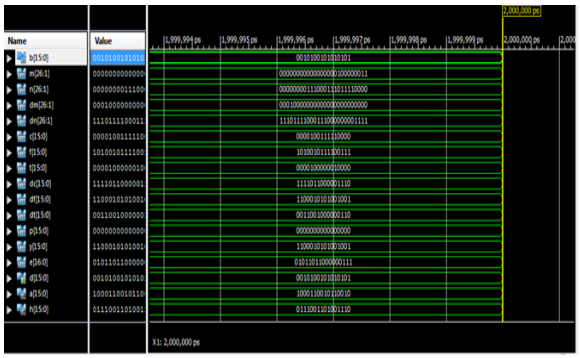

FIG 5. OUTPUT WAVEFORM

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	69	960	7%
Number of 4 input LUTs	128	1920	6%
Number of bonded IOBs	281	66	425%

FIG 6. SUMMARY REPORT

V.CONCLUSION

In this paper, a multi-strategy ECC scheme is proposed using pre-check mechanism based on polar code which can prolong the life endurance of SSD with reasonable hardware cost. The proposed hard decoder plays a significant role by improving the decoding efficiency with simple bitwise operations which sufficiently eliminate corresponding hardware cost. Meanwhile,

the proposed pure-soft decoder provides powerful protections to guarantee the dependability of SSD, making it possible to facilitate large-scale application of enterprise-level products. In addition we briefly prove that Gray code is the best mapping scheme in flash memory.

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