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Reduction of Static Power in CMOS Circuits by Using Biasing and Body Biasing Techniques

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Abstract: — The VLSI design of an efficient integrated circuit in terms of power, area, and speed simultaneously, has become a very challenging problem. Power dissipation is recognized as a major problem in modern VLSI design. The market of portable, battery operated computing devices has grown rapidly in recent years and so the need for energy efficient design. The mobile computing devices are inactive for a long time and active only for a brief amount of time. So during the inactive state, the devices keep consuming certain power which is dominated by the leakage power consumption of all the components. Various methods have been existed to reduce the leakage power like Power Gating Architecture and Multimode Power Gating Architecture. Power Gating Architecture was presented to support Multiple Power-off modes and reduce the leakage power during short periods of inactivity. However, this scheme suffers from high wakeup time. Recently, a Multimode Power Gating method is used where the wake up time is reduced than the Power Gating Architecture method but the leakage power increases. To reduce static power reduction use low supply voltage and low threshold voltage without losing speed performance. The drawback in Multimode Power Gating method is increase in delay. I proposed a the Body Biasing method that can be combined with Multimode Power Gating method to offer further Static Power Reduction benefits in Standby mode. The Body Biasing requires less design effort and offers greater leakage power reduction than the Multimode Power Gating method. Analysis and extensive simulation results demonstrate the effectiveness of the Body Biasing design.

***Index Terms*—Leakage power, Multi-mode VTCMOS switches, power Consumption reduction, process variation, Reconfigurable power-gating structure.**

(1) INTRODUCTION

Power dissipation is recognized as a major problem in modern VLSI design field. The development of competitive market sectors such as wireless applications, laptops, and portable devices, depends on the power dissipation as the most important parameter because the growth rate of the battery technologies is not so promising. In most cases, the low power dissipation is equally important with the remaining two design parameters, namely area and speed. Consequently, the design of an efficient integrated circuit in terms of power, area, and speed simultaneously, has become a very challenging problem; two components determine the power dissipation in a CMOS circuit:

I.Static Power Dissipation
II. Dynamic Power Dissipation

(I) STATIC POWER DISSIPATION

Static power is power consumed while there is no circuit activity. The static power dissipation mainly includes sub threshold current and reverse biased diode leakage current. Below the threshold voltage, in weak inversion, the transistors are not completely off. The sub threshold current has a strong dependence on the threshold voltage.

Sub threshold Current: The sub threshold current that arises from the inversion charges that exists at the gate voltages below the threshold voltage.

Tunneling Current: There is a finite probability for carrier being passed through the gate oxide which results in tunneling current thorough the gate oxide.

Reverse-biased Diode Leakage: Reverse bias current in the parasitic diodes.

(a) Leakage Power scaling down features requires lowering the threshold voltage, which also increases leakage power; almost doubles with each shrinking [1]. Multiple threshold devices are used to reduce leakage power. There are different types of power leakages shown below in Figure 1. due to loss of current. As devices keep shrinking, the channel length shortens and the gate oxide thickness reduces, increasing the gate-induced drain leakage, the gate oxide tunneling current, and the junction leakage [11].

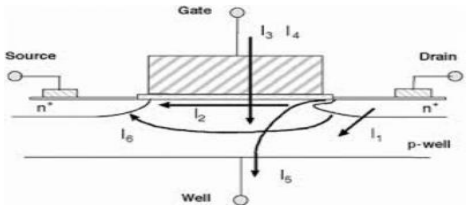

Figure 1: Leakage Power Component

Where I_1: reverse bias PN junction (both ON & OFF), I_2: sub threshold leakage (OFF), I_3: Gate Leakage current (both ON & OFF), I_4: gate current due to hot carrier injection (both ON & OFF), I_5: gate induced drain leakage (OFF) and I_6: channel punch through current (OFF).

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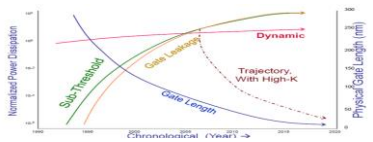

Figure 2: Increased Sub threshold Leakage

(b) Sub threshold current Sub threshold current is given by the equation:

$$I_{sub} = \mu_0 C_{OX} \left(W/L\right) V_t e^{(V_{GS}-V_{th})/nV_t} \quad \ldots(1)$$

Where μ_0: carrier surface mobility, Cox: gate oxide capacitance per unit area, L: channel length, W: gate width, V_t = kT /q where q: thermal voltage, n: technology parameter [1]. The reduction of threshold voltage affects the subthreshold current, which increases exponentially. Borkar predicts that leakage power increases by 5 times every generation, as shown in Figure 1.2. While active power remains roughly constant.

(c) Junction Leakage

There is a small amount of static power dissipation due to reverse-bias leakage between diffused regions and the substrate. This leakage inside a device can be explained with the parasitic diodes of a CMOS inverter. The source drain diffusion and N-well diffusion form parasitic diodes as shown in Figure 3. The parasitic diodes are shown between the N-well and substrate. Because parasitic diodes are reverse biased; only their leakage currents contribute to static power dissipation. The PN junctions between diffusion, substrate and well are all junction diodes. These are revered biased as substrate is connected to GROUND and well connected to V_{DD}. However reversed biased diode also conduct small amount of current.

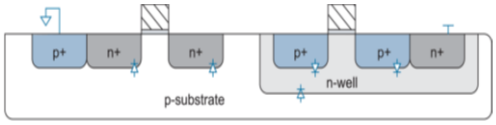

Figure 3: Junction Leakage due to Reverse Biasing

The leakage current ($I_{Leakage}$) of the diode is described by the following equation:

$$I_{Leakage} = I_S \left(e^{qV/kT} - 1\right) \quad (2)$$

Where: I_S = reverse saturation current, V = diode voltage, k = Boltzmann's constant (1.38 × 10–23 J/K), q = electronic charge (1.602 × 10–19 C),T = temperature in Kelvin (300ºK).Static Power Dissipation takes place due to the leakage current and the leakage current occur due to the off transistor because some minute current flows in off transistor whether it is PMOS or NMOS [17]. Expression for Leakage Power:

$$P_L = V_{DD} * I_{Leakage} \quad (3)$$

Where: P_L = Leakage power, $I_{Leakage}$ = Leakage current, V_{DD} = Supply voltage. Even though the architecture proposed is efficient for reducing leakage power during short periods of inactivity, it has several drawbacks that limit its applicability. First, it cannot be easily extended to support more than two intermediate power-off modes and thus it cannot fully exploit the power reduction potential of the power-gating structure, especially for high-performance circuits. Second, the architecture consumes a significant amount of power, and this reduces the benefits offered by the power switches.

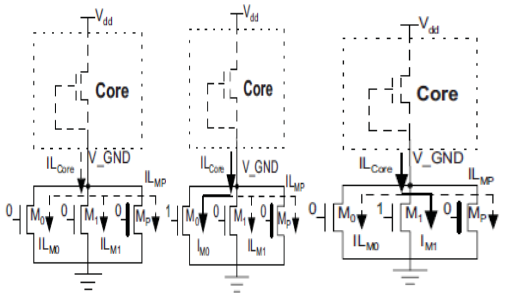

Figure: 4 Multi-Mode power gating Architectures:
a) Snore mode b) Dream mode c) Sleep mode

Third, this structure is very sensitive to process variations, which can adversely affect its manufacturability and predictability. Finally, it is not easily testable, as it consists of analog components. In this paper we present an effective body biasing architecture that has none of the above drawbacks of the architecture proposed. The proposed structure requires minimal design effort since it is very simple, and with no analog components. It is considerably smaller than the architecture proposed and offers greater power savings for similar wake-uptimes. The proposed architecture is also more tolerant to process variations; thus its operation is more predictable. Finally, a reconfigurable version of the proposed architecture is also proposed, which can tolerate even greater process variations, enabling thus the utilization of the proposed architecture for newer technologies. The organization of the rest of this paper is as follows Section II presents background material to place the proposed work in an appropriate context. Section III introduces the proposed body biasing architecture, the design method, and the reconfigurable architecture. Section IV presents an evaluation of the proposed architecture, including comparisons with previous work. Finally, Section V concludes this paper.

(2) PROPOSED METHOD

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Fig. 4 presents Multi-mode power gating Architectures. It consists of the main power switch transistor M_P and two small transistors M_0 and M_1, each corresponding to an intermediate power-off mode (M_0 corresponds to the dream mode and M_1 corresponds to the sleep mode). Transistor *MP* is a high-*Vt* transistor and it remains on only during the active mode. Transistors M_0 and M_1 are small low-*Vt* transistors that are turned on only during the corresponding power-off mode. (i.e., *M*0 is turned on during the dream mode and M_1 is turned on during the sleep mode).In proposed system, VTCMOS technique threshold voltage of low threshold devices is varied by applying variable substrate bias voltage from a control circuit

- Increase in the lower threshold voltage, devices leads increased sub threshold leakage and hence more standby power consumption.
- To reduce static power reduction is to use low supply voltage and low threshold voltage without losing speed performance.
- It provides power in reduction only 10%. Try. It has major advantages.

(3) BODY BIASING TECHNIQUE

A. Main Architecture:

Fig.5 presents the proposed design. It consists of the main power switch transistor M_P and two small transistors M_0 and M_1, each corresponding to an intermediate power-off mode (M_0 corresponds to the dream mode and M_1 corresponds to the sleep mode). Transistor M_P is a high-V_t transistor and it remains on only during the active mode. Transistors M_0 and M_1 are small low-V_t transistors that are turned on only during the corresponding power-off mode. (i.e., M_0 is turned on during the dream mode and M_1 is turned on during the sleep mode). The various modes of operation are as follows.

1) Active Mode: Transistors M_P, M_0, M_1 are on.

2) Snore Mode: Transistors M_P, M_0, and M_1 are off as shown in Fig. (a).In this case, the leakage current of the core, $I\,L_{core}$, is equal to the aggregate leakage current flowing through transistors M_0, M_1, M_P ($I\,L_{core} = I\,L_{M0} + I\,L_{M1} + I\,L_{MP}$), which is very small (note that M_0, M_1 are small transistors and M_P is a high- V_t transistor). Thus the voltage level at $V_{\_GND}$ is close to *V*dd and the circuit consumes a negligible amount of energy, but the wake-up time is high.)

3) Dream Mode: Transistor M_0 is on and transistors M_P and M_1 are off as shown in Fig. 2(b). In this case *the* current flowing through transistor M_0 (and thus the aggregate current flowing through M_0, M_1 and M_p) increases because M_0 is on ($I_{MO} > I\,L_{M0}$). The exact value of I_{M0} depends on the size of transistor M_0 , and it sets the virtual ground node at a voltage level which is lower than V_{dd} (i.e., $VV_{_GND} < V$dd). Thus the Static power consumed by the core is higher compared to the snore mode, but the wake-up time is less.

***4)* Sleep Mode:** Transistor *M*1 is on, and *MP*, *M*0 are off as shown in Fig. 2(c). Provided that transistor *M*1 has larger aspect ratio than M_0 ($W_{M1}/L_{M1} > W_{M0}/L_{M0}$), the agree *MP* increases even more when *M*1 is on (note that$I_{M1} > I_{M0}$). Consequently, the voltage level at the virtual ground node is further Reduced compared to the dream mode and thus the wake-up time decreases at the expense of increased power consumption ate current flowing through *M*0, *M*1.

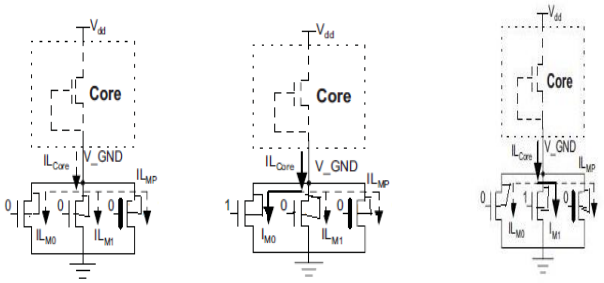

Figure: 5 Proposed architecture: (a) Snore mode (b) Dream mode (c) Sleep mode

B. Design Method:

Body biasing has been demonstrated to be effective in addressing process variability in a variety of simple chip designs. However, for modern microprocessor ICs with multiple cores and dynamic voltage/frequency scaling (DVFS), the use of body biasing has significant implications. For a 16- core chip-multiprocessor implemented in a high-performance 22 nm technology, the body biases required to meet the frequency target at the lowest and highest voltage/frequency levels differ by an average of 0.7 V, implying that per-level biases are required to fully leverage body biasing. The need to make abrupt changes in the body biases when the voltage/frequency level changes affects the cost/benefit analysis of body biasing schemes. It is demonstrated that computing unique body biases for each voltage/frequency level at chip power-on offers the best tradeoff among a variety of methods in terms of area, performance and power.

While continuously adjusting the body biases during operation offers improvements in energy/efficiency, these benefits were outweighed by the implementation costs. The implementation costs of continuously adjusting the body biases are dominated by the settling time of the controller.

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Existing controllers designed for simple general-purpose microprocessors do not optimize for settling time, and require D/A converters with high time constants. We propose a fully-analog controller that is able to achieve significantly lower settling time for a fixed area and power than previous controllers. With the proposed controller, continuously computing the body biases offers a better tradeoff in terms of area, performance, and power than computing unique body biases for each voltage/frequency level at chip power-on. Further improvements in energy/efficiency can be achieved with an integrated approach to body biasing and DVFS. Because V_{DD} is scaling and body biasing has different effects on static versus dynamic power, the operating point yielding the lowest overall power is dependent on the percentage of total power due to leakage. Leakage power, in turn, is strongly influenced by process variations.

C. Body Biasing:

Body biasing is another method of improving energy/efficiency, by reclaiming performance lost to margins due to variations. After fabrication, the threshold voltage (V_{TH}) of transistors can be modulated by changing the body-to-source voltage. In bulk MOSFETs, the V_{TH} is given by:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|}\right)$$

Where V_{TH0} is the device threshold voltage with no body bias applied, $2\Phi F$ is the surface potential at strong inversion, and γ is the body effect coefficient. For simplicity, we examine this equation for the case of an NFET with the source tied to ground. If a negative voltage is applied to the body then the depletion width increases, which means that a higher gate voltage is required to form an inversion layer and thus the V_{TH} increases; this is known as a reverse body bias (RBB).

Similarly, if a positive voltage is applied to the body while the source is grounded, then the depletion width decreases, and thus the V_{TH} decreases; this is known as a forward body bias (FBB). Throughout this work, V_{BSn} and V_{BSp} will represent the body to source voltage of NFETs and PFETs, respectively. Negative values of these parameters will indicate RBB and a positive one FBB, regardless of which direction the body-to-source voltage must actually be shifted. There are several technology issues with body biasing in bulk MOS RBB increases short channel effects, which increases variability within devices sharing a bias. This is especially problematic in circuits that are sensitive to device matching, such as SRAMs. FBB improves short channel effects, but also increases junction leakage, potentially to the point where the source-to bulk junction is forward biased.

Additionally, an analog signal, the body bias, must be distributed a significant distance – in the extreme, across the entire die. This becomes increasingly problematic with scaling because cross-talk between wires worsens. Finally, the sensitivity of V_{TH} to the body bias decreases with scaling, because the channel doping increases. Body biasing is limited in the magnitude of the V_{TH} shift that can be induced. The maximum forward-bias is limited by current flows across the P-N junction formed between the n-well and p-well. A thyristor-like device is formed in the substrate by the two bipolar transistors, as shown in Figure 3 found that there was no latch-up effect FETs.

Body biasing is limited in the magnitude of the V_{TH} shift that can be induced. The maximum forward-bias is limited by current flows across the P-N junction formed between the n-well and p-well. A thyristor-like device is formed in the substrate by the two bipolar transistors, as shown in Figure 6 Oowaki *et al.* found that there was no latch-up effect with up to 0.5 V forward bias [(assumed by Miyazaki *et al.* , Tachibana *et al.* , and Narendra *et al.* . The maximum reverse-bias is limited by high leakage and possible break-down across the reverse biased drain body junction, particularly during burning. The sensitivity of threshold voltage to the body bias for NFETs and PFETs is shown in Figure for the 90 nm, 45 nm, and 22 nm predictive technologies. While the sensitivity of V_{TH} to the body biases does decrease as technology scales, the decrease from 90 nm to 22 nm. (4 technology generations) is only 12% for the NFET and 10% for the PFET.

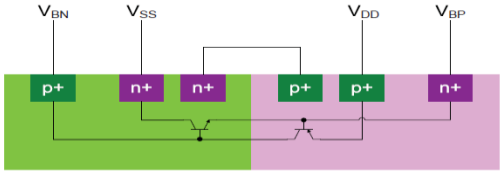

Figure 6: Leakage path in forward body biasing

(4) EVALUATION AND COMPARISONS

In this section, we present simulation results and comparisons against other techniques presented in the literature.

Results and Comparisons Using a Large Logic Core:

The target of the first subsection is to evaluate the proposed method when it is applied to large logic cores that are comparable in size to real designs from industry. To this end, we present simulation results on a large logic core consisting

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of 9 million transistors. This core consists of multiple inverters of various sizes which are driven by various input vectors. Even though it is not a real circuit, it is representative of a realistic industrial circuit in terms of static power consumption during dc operation in power-off mode. We used the 45-nm predictive technology with 1.1-V power supply. The leakage power consumption of the core in idle mode with no power gating is equal to 10 mW. All simulations were done using the Synopsis HSpice simulation engine. We note that, because of the use of a different core with respect as well as different experimental parameters (such as the technology, the voltage setting, and the input vector), we cannot directly compare the experimental results of our method with the results presented. Therefore, we implemented both the architecture [see Fig. 4(c)] and the proposed architecture (see Fig. 5) for the aforementioned logic core. As suggested, the width of the main power switches. (Transistor denoted as *MP*).

TABLE I: COMPARISON BETWEEN EXISTING AND PROPOSING METHODS

Mode of operation	Power dissipation values for Existing Method (µw)	Wake up time (ns)	Power dissipation values for Proposed Method using Body Biasing (µw)	Wake up time (ns)
Snore Mode	25µw	31.15 ns	**10.07 µw**	39.10 ns
Dream Mode	35.3111µw	28.56 ns	**26.74 µw**	32.5 ns
Sleep Mode	35.3110µw	29.22 ns	**20.15 µw**	33.2 ns

Was set equal to 12% of the total width of the n MOS transistors in the logic core. For the logic core that we used, the width/length ratio of transistor *MP* is calculated as equal to 43.2 × 106 nm/45 nm and it is implemented as the parallel connection of a number of smaller transistors. In order to provide fair comparison, the transistor sizes in both architectures were selected in such a way as (a) to be of minimum size required and (b) to provide similar wake-up times, in both architectures. In dream and sleep mode the power dissipation is same, as only one transistor is in on mode in the network apart from core logic. Moreover, in the proposed scheme, the sizes of transistors M_0 and M_1 have been selected in such a way as to provide the same voltage level at the virtual ground node with the scheme proposed at each power-off mode and for the same input vector. Thus, the logic core consumes the same amount of static power in both architectures at each power-off mode. For example, considering an input vector that drives the two-thirds of the transistors to logic "1" and the rest of the transistors to logic 0," the voltage level at the $V_{\_GND}$ node is equal to 217.1, 415.8, 541.8, and 668.5 mV at four intermediate power-off mode. For both architectures, we assume that the voltage at the $V_{\_GND}$ node settles to the expected value before the waking up process begins. In addition, the core is considered as fully operational after the virtual ground node is discharged to the value of 1% of V_{dd}. First, we compare both architectures in terms of area overhead measured as transistor sizes. The width of transistors *M*0, *M*1 in the proposed structure is equal to 250 and 480 nm, therefore, for comparison purposes; we excluded the overhead of these transistors from the overhead of both architectures. We also exclude the decoder, as it is optional in both architectures and can be omitted (we implemented both schemes without the use of decoders). The rest of the circuitry in the proposed architecture occupies Almost one-fifth (1/4.8) of the area of the architecture and it is less than 0.0002% of the area of the core. Even though this is an estimate based on transistor sizes, it is apparent from Figs. 4(c) and 5 that the proposed architecture is much simpler.

Note that the schemes proposed support only one intermediate power-off mode, which is denoted as Dream for comparison purposes. Entries in Table II corresponding to the second intermediate power-off mode (i.e., the Sleep mode) which is not applicable for the schemes proposed, are denoted as "N/A" (not applicable). The last three rows show the number of cycles that are needed for waking up the core from each power-off mode that is supported by each method. The first two columns present the results for both a high-*Vt* and low-*Vt* parker transistor proposed. The next two columns present the results for the high-*Vt* and low-*Vt* parker transistor proposed. We assumed four different bias voltages, 0, −0.2, −0.4, and −0.6 V for both the high-*Vt* and low-*Vt* parker transistor proposed but the results were nearly the same (except for the sleep mode where the static power slightly varied between 0.94 and 0.96 mW as reported in Table II). The next two columns present the results for configurations Conf. 1 and Conf. 2 that are used.

The last column presents the results for the proposed method. It is obvious that the methods proposed fail to deliver a tradeoff between wake-up time and power consumption regardless of the kind of parker transistor (high-*Vt* or low-*Vt)* or the bias voltage. Even though multiple types of these transistors and/or bias voltages are used at the same core, with an obvious impact on area overhead, they still fail to deliver a sufficient range of wake-up times. The method proposed in offers low static power consumption at the expense of very large wake-up times and increased area overhead. More importantly, similar to the method proposed, the method proposed supports only a single intermediate power-off mode.

In contrast to the proposed method offers more than one intermediate power-off mode with a wide range of wakeup times and, as will be presented later, the proposed method can easily provide even more than two intermediate power off modes—a target that is obviously unachievable for the other

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methods. Finally, the proposed method has the smallest used area overhead. Therefore, the proposed method better exploits the tradeoff between static power dissipation and wake-up time with much less area overhead than the rest of the methods.

(5) EXPERIMENTAL RESULTS ANALYSIS

In figures a given below a Snore Mode, Dream Mode, Sleep Mode, Input/output waveforms. When input is high, output is low. The wave forms can represented in x-axis time and in y-axis voltage.

(A) Multimode Power Gating of a CMOS Inverter in Snore Mode

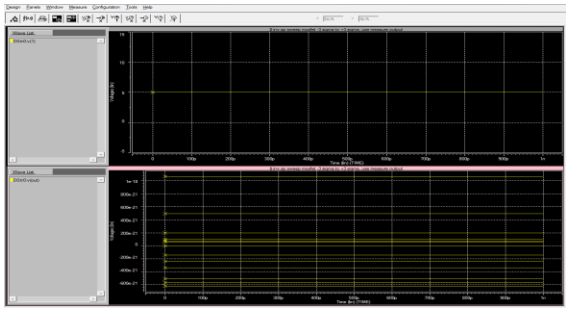

Figure 7: Multimode Power Gating of a CMOS Inverter in Snore Mode

The power dissipation value for the Multimode Power Gating of a CMOS Inverter in Snore Mode is 2.50E-05.

(B)Multimode Power Gating of a CMOS Inverter in Dream Mode

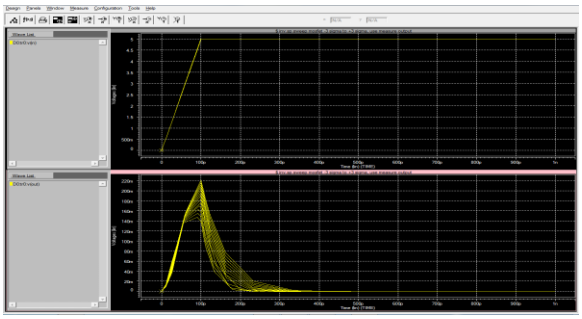

Figure 7: Multimode Power Gating of a CMOS Inverter in Dream Mode

The power dissipation value for the Multimode Power Gating of a CMOS Inverter in Dream Mode is 3.53E-05.

C) Multimode Power Gating of a CMOS Inverter in Sleep Mode

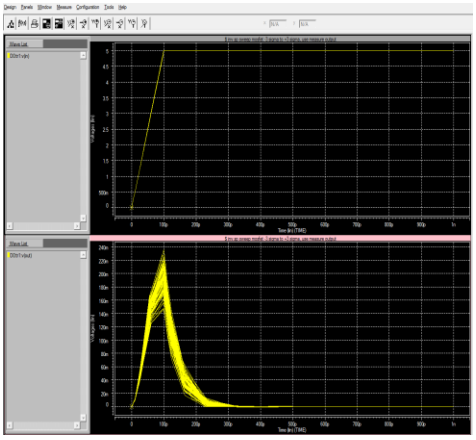

Figure 8: Multimode Power Gating of a CMOS Inverter in Sleep Mode

The power dissipation value for the Multimode Power Gating of a CMOS Inverter in Sleep Mode is 3.53E-05.

D) Snore Mode with Body Bias of a CMOS Inverter

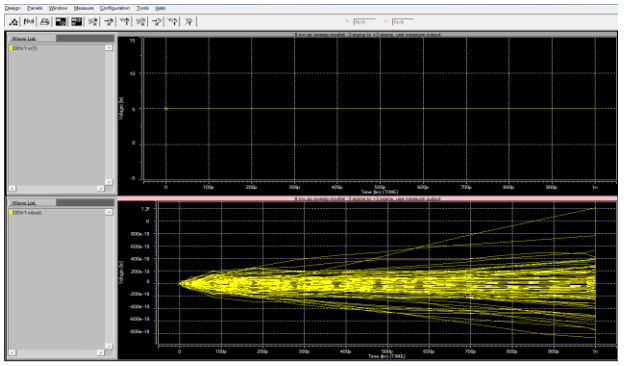

Figure 9: Snore Mode with Body Bias of a CMOS Inverter

The power dissipation value for the Snore Mode with Body Bias of a CMOS Inverter is 1.02E-05.

E) Dream Mode with Body Bias of a CMOS Inverter

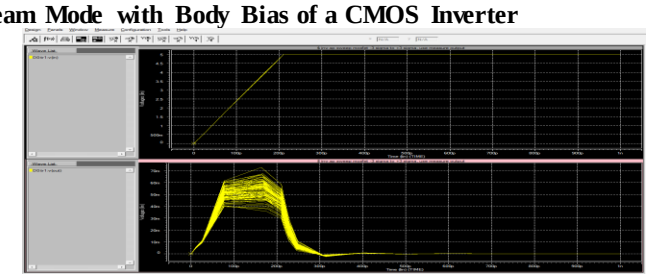

Figure 10: Dream Mode with Body Bias of a CMOS Inverter

The power dissipation value for the Dream Mode with Body Bias of a CMOS Inverter is 2.67E-05.

F) Sleep Mode with Body Bias of a CMOS Inverter

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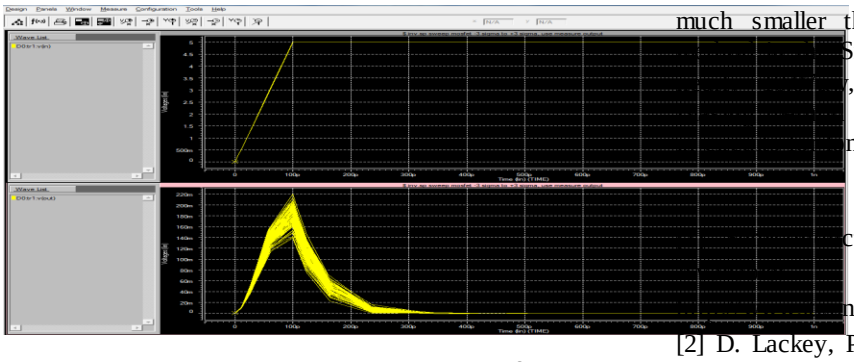

Figure 6.10: Sleep Mode with Body Bias of a CMOS Inverter

The power dissipation value for the Sleep Mode with Body Bias of a CMOS Inverter is 2.83E-05.

(6) CONCLUSION

In this project the existing method is Multimode Power Gating method, the power dissipation values obtained in Snore Mode, Dream Mode, and Sleep Mode are 25µw, 35.31µw, 35.31µw.The power dissipation values obtained in Standby mode are higher. So a Body Biasing method is proposed. The proposed method, Body biasing method offered the advantage of simplicity. It is very simple and all digital, and it is minimally sized since it consists of only a single small transistor for each power off mode. . A reconfigurable version of this method can be used to increase the manufacturability It requires significantly less area and consumes much less power than the previous Multimode Power Gating method. The Power Dissipation values for the Body Biasing method are much smaller than that of the Multimode Power Gating Snore Mode, Dream Mode and Sleep mode of , 20.15µw, and 26.75µw. Hence the Body is preferred to achieve low Power Dissipation nger battery life.

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