

Design and Analysis of Multilevel Inverter Topology using less number of Switches

G. Krishnaiah

M.Tech (Digital Systems and Computer Electronic)

Abstract: *The emergence of the multilevel inverters has been in increase since the last decade. The main choice of the multilevel inverters in the area of high power medium voltage energy control. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. The multilevel cascaded inverter was introduced in Static VAR compensation and drive system. In this paper presents a new technique for getting a multilevel output and also uses PWM control techniques. In this technique, the number of switches used for the dc to ac conversion is reduced so this dc to ac conversion significantly reduces the initially cost. This technique exhibits some attractive features which suits in industrial applications.*

Keyword: Matlab Simulink, PWM, multilevel inverter.

I. INTRODUCTION

Recently multilevel power conversion technology has been a very rapidly growing area of power electronics with good potential for further developments. The most attractive applications of this technology are in the medium to high-voltage range and it makes the semiconductor devices in a multilevel converter have a much lower dv/dt , the outputs of the converter are very much distortion less, allows having almost perfect currents with very good voltage waveforms most of the undesirable harmonics will be eliminated generating low switching losses. The dc voltage sources are available from batteries, capacitors, or fuel cells

[1-5].

Multilevel voltage source inverter is recognized as an important alternative to the normal two level voltage source inverter especially in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter.

II. MULTILEVEL INVERTER

A. Basic concept of Multilevel Inverter:

Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. The semiconductor devices are not connected in series to form one single high-voltage switch. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Fig.1 shows the block diagram of the general multilevel inverter.

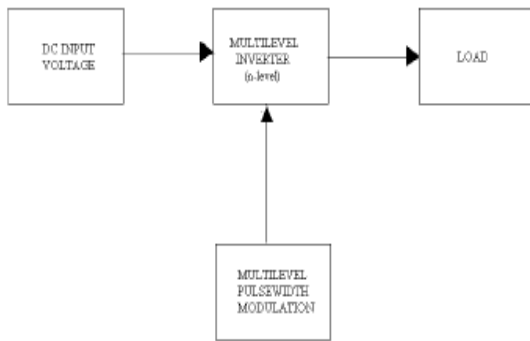


Fig. 1 Multilevel Inverter System

Generally, the output waveform of the multilevel inverter is generated from different voltage sources obtained from the capacitor voltage sources. In the past two decades, several multilevel voltage source converters have been introduced. In that some of the topologies are popular and some are not popular. Consider a three phase inverter system as shown in the fig.2 with DC voltage V_{dc} . Series connected capacitors constitute the energy tank for the inverter, providing some nodes to which the multilevel inverter can be connected. Each capacitor has the same voltage E_m , which is given by

$$E_m = V_{dc} / (m-1)$$

Where m denotes the number of the level is referred to as the number of nodes to which the inverter can be accessible. An m level inverter needs $(m-1)$ capacitors. Output phase voltages can be defined as voltage across output terminals of the inverter and the ground point denoted by 0 as shown in figure 2.2

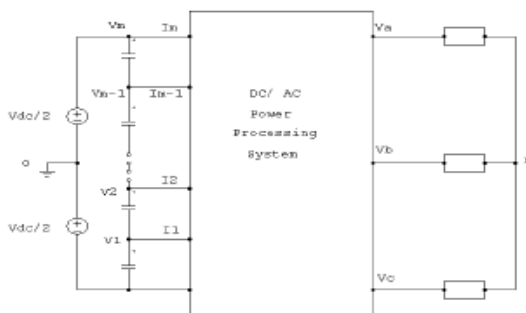


Fig. 2 Three Phase Multilevel Power Processing System

B. Types of Multilevel Inverter

The general purpose of the multilevel inverter is to synthesize a nearly sinusoidal voltage from several levels of dc voltages, typically obtained from capacitor voltage sources. As the number of level increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also as more steps added to the waveform, the harmonic distortion of the output waveform decreases, approaching zero as the level increases. As the number of level increases, the voltage that can be summing multiple voltage levels also increases. Three converter topologies have been considered to have commercial potential. They are

- A) Diode-clamped multilevel inverter
- B) Flying-capacitor multilevel inverter
- C) Cascaded inverter with separate DC sources

Among the three familiar topologies, cascaded multilevel inverter is an effective one. So by skipping the other topologies, the cascaded multilevel inverter is explained below. Cascaded multilevel inverter is having a unique and attractive topology such as simplicity in structure, usage of less number of components, etc.

C. Cascaded Multilevel Inverter with Separate DC Source:

The multilevel inverter using the cascaded converters with separate DC sources is discussed here. The cascaded multilevel inverter synthesizes a desired voltage from several independent sources of DC voltages which may be obtained from batteries, fuel cells or solar cells. This configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications. This converter can avoid extra clamping diodes or voltage-balancing capacitors. A single phase, m -level configuration of the cascaded multilevel inverter shown in the fig.3 Each single DC sources is associated with a single H-bridge converter. The AC terminal voltages of different level converters are connected in series. Through different combinations of the four switches, $S1-S4$, each converter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero.

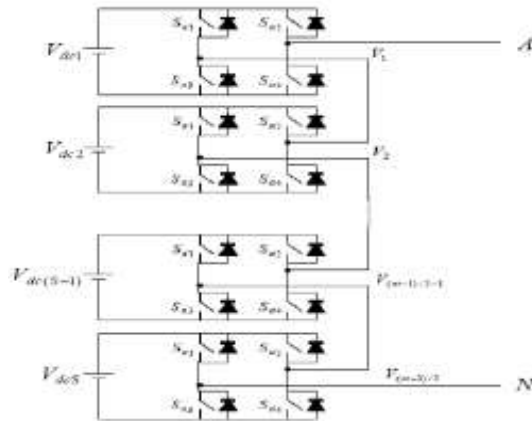


Fig.3 Single Phase Structure of Cascaded Multilevel Inverter

The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output waveform is the sum of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters. In this topology, the number of output-phase voltage levels is defined by $m=2N+1$, where N is the number of DC sources. A five level cascaded converter, for example, consists of two DC sources and two full bridge converters. Minimum harmonic distortion can be obtained by controlling the conduction angles at different converter levels.

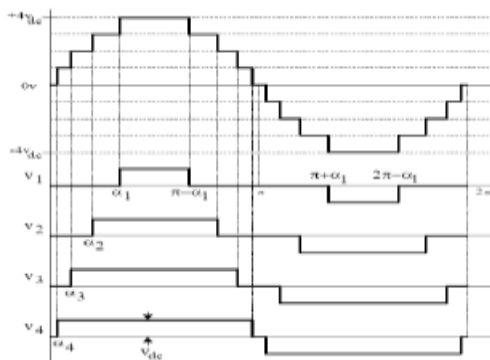


Fig.4 Waveform of a Nine-Level Output Phase Voltage and each H-Bridge Output Voltage.

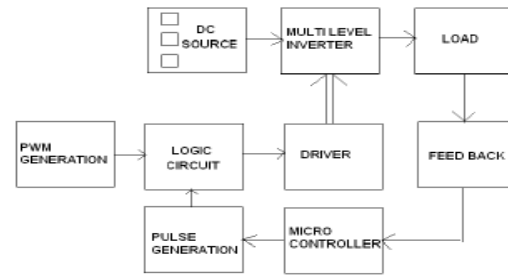


Fig.5 Block Diagram of the Proposed Multilevel Inverter

Advantages

1. The series structure allows a scalable, modularized circuit layout and packaging since each bridge has the same structure.
2. Switching redundancy for inner voltage level is possible because the phase voltage output sum of each bridges output.
3. Potential of electrical shock is reduced due to separate DC sources.
4. Requires less number of components when compared to other two types.

Disadvantages

1. Limited to certain applications where separate DC sources are available.
2. Usage of the power semiconductor switches increases exponentially whenever the level is to be increased

III. PROPOSED MULTILEVEL INVERTER

The proposed converter consists of less number of switches when compared to the other familiar topologies. The initial cost reduces because of the switch reduction. So, it looks attractive and an apt one for industrial applications. The block diagram of the proposed multilevel inverter is shown in the general circuit diagram of the proposed multilevel inverter is shown in the fig.6. The switches are arranged in the manner as shown in the figure. For the proposed topology, we just need to add only one switch for every increase in levels. So initial cost get reduced. Let us see operation in the next subdivision in detail for the seven-level inverter.

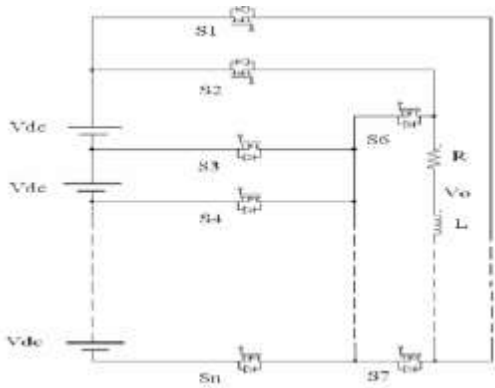


Fig.6 General Circuit Diagram of the Proposed Multilevel Inverter Topology

A. Proposed Multilevel Inverter for Seven Levels

The proposed multilevel inverter for seven levels is shown fig.7.

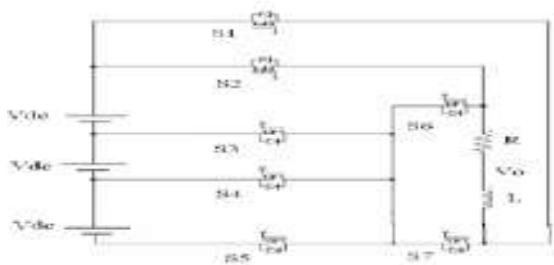


Fig.7 Circuit Diagram of the Seven Levels Proposed Multilevel Inverter

The inverter consists of seven MOSFET switches and three separate DC sources with a load. By switching the MOSFETS at the appropriate firing angles, we can obtain the seven level output voltage. MOSFET is preferred because of its fast switching nature.

Table.1 Switching Conditions

SINO	Conducting Switches	Amplitude Of the Output Voltage
1	S ₂ , S ₇ , S ₃	+Vdc
2	S ₂ , S ₇ , S ₄	+2Vdc
3	S ₂ , S ₇ , S ₅	+3Vdc
4	Nil	0
5	S ₁ , S ₆ , S ₃	-Vdc
6	S ₁ , S ₆ , S ₄	-2Vdc
7	S ₁ , S ₆ , S ₅	-3Vdc

The fig.8 shows the expected waveform of the proposed converter. Consider the input supply as 100volts DC supply. Three various supplies are given individually. By switching the MOSFETS, according the Table.1 given above, the various levels of output is obtained.

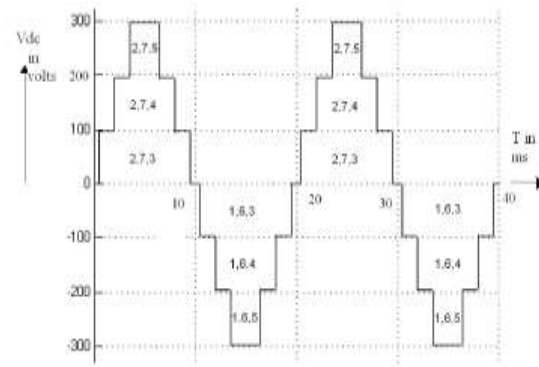


Fig.8 Output Waveform of the Proposed Multilevel Inverter

Advantages

1. Because of the reduction in the number of switches the initial cost reduces.
2. Controlling becomes easier.
3. Losses become less due to the elimination of the harmonics.
4. Apt structure for industrial applications.
5. Overall weight reduces because of the usage of less number of components.

Comparison between the Proposed Multilevel Inverter and the Cascaded Multilevel Inverter

TheTable.2 shows the comparison between the proposed inverter with the cascaded multilevel

inverter. The proposed converter exhibits a significant outcome such as reduction in the number of switches and an easy control is possible.

Parameters	Cascaded				Proposed			
	3	4	5	6	3	4	5	6
Levels								
Switches required	12	16	20	24	7	8	9	10

IV. SIMULATION RESULTS

Simulation results of the proposed converter for seven levels using MATLAB/Simulink. The PWM technique is used for pulse generation. The MOSFET switches are used because of its fast switching capability. The input supply for each DC source is 100V. The load used is a R-L load. The output waveform is phase voltage and it comprises seven levels. The PWM technique is used to produce the control signal.

A. Simulation of the Proposed Multilevel Inverter for Seven Levels

The MATLAB simulation circuit for the proposed inverter which comprises only seven MOSFET switches for producing seven levels is shown in the fig.9. The MATLAB circuit used for generating gate pulse without using PWM technique is shown in the fig.10. The MATLAB circuit used for generating gate pulse using PWM technique is shown in the fig.11. The pulse generated by the circuit shown in the fig.12. The output waveform of the proposed inverter for seven levels without PWM technique is shown in the fig.13. The output waveform of the proposed inverter for seven levels with PWM technique is shown in the fig.14. The pulse is generated using comparison between constant DC voltage and power supply. The comparison is done using operational amplifiers. For the first pulse we give a DC voltage of lesser amplitude and moderate amplitude for the second pulse. Likewise we have to increase the amplitude to reduce the pulse width. The PWM

technique is used to obtain a good harmonic spectrum. The gating pulse is generated from the above mentioned process and given separately to the respective MOSFETs. The supply is given through three separate DC sources. The R-L load is used for the simulation purpose. The simulation results show that the circuit is operating properly. The output waveform has three levels in the positive side and three levels in the negative side and a zero level. Totally there are seven levels. Thus the proposed multilevel inverter for seven levels is successfully simulated. And the results are shown below in sequential manner.

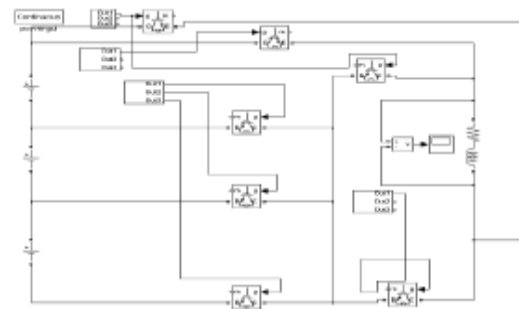


Fig. 9 Proposed Multilevel Inverter for Seven Levels

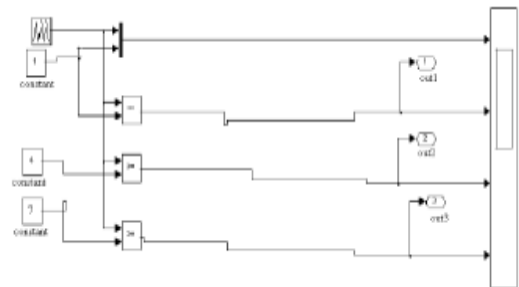


Fig. 10 Gate Pulse Generation Circuit without PWM Technique

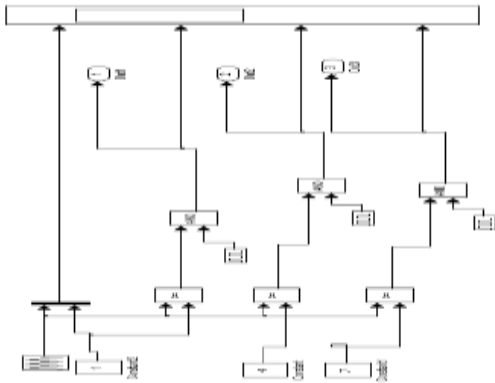


Fig.11 Gate Pulse Generation Circuit with PWM Technique

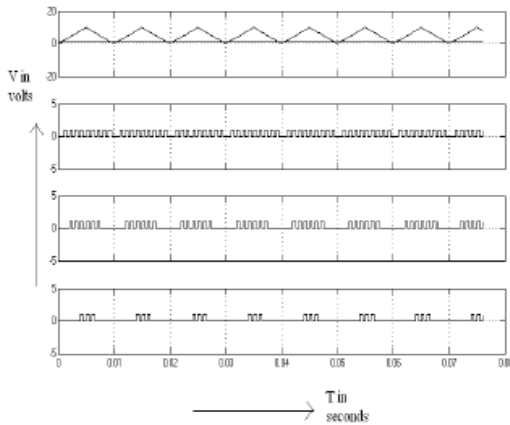


Fig.12 Pulses Generated Using PWM Technique

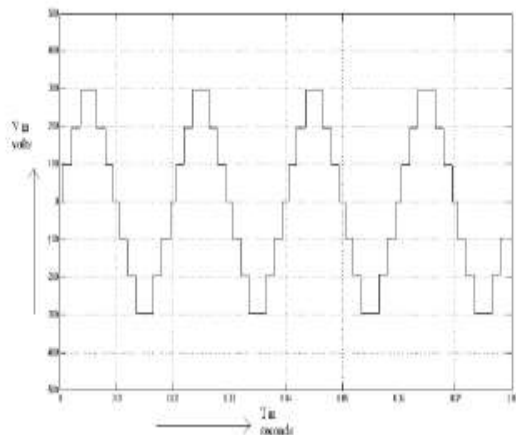


Fig.13 Output Voltage Waveform without Using PWM Technique

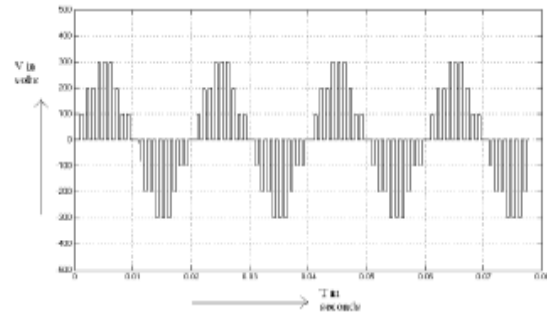


Fig.14 Output Voltage Waveform Using PWM Technique

V. CONCLUSION

The simulation of the seven-level multilevel inverter is successfully done using pulse width modulation technique. From the simulation, it is noted that the new multilevel inverter topology works well and shows hope to reduce the initial cost and complexity. When we increase the levels, the number of switches used is very less compared to the other topology.

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Biodata



G.Krishnaiah completed M.Tech (Digital Systems and Computer Electronic).