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# CMOS Realization of a Novel VCO for Low Voltage and Low Power Applications

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**Abstract**: *This paper presents a low power consumption LC tank voltage controlled-oscillator (VCO). It is suitable for communication system of Integrated circuit. In this circuit, the operating frequency is generated by LC-tank. The circuit add a forward-bias circuit at the body to decrease the threshold voltage. Therefore, it can reduce the operation voltage and minimize the dc power consumption. This design was simulated by using TSMC 0.18-µm CMOS process.*

## I INTRODUCTION

In recent years, single-chip integration using CMOS technology has become a major research area. Advanced CMOS processes have enabled the implementation of high data rate wireless communication systems which are frequently used for local clock generation in the communication transceivers for the frequency synthesis applications. It needs to provide a clean and stable carrier to the mixer what the transmitted long distance is done. voltage-controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input.

The low power consumption LC-tank voltage controlled oscillator (VCO) is suitable for communication system of integrated circuit. The operating frequency is generated by LC-tank circuit.

The VCO's are the heart of every wired and wireless communication systems including phase locked loop, clock data recovery, digital millimeter radar etc.. LC-tank voltage-controlled oscillators (VCOs) are widely used in RF communication systems, the circuit-based oscillators depends on the quality of inductors and capacitors. The inductors are not ease to adjust because of the fixed by the coil in circuit, so we could only tuning capacitors by the tuning voltage (Vtune) that also change VCO oscillator's frequency. The phase noise of VCO is one of the most important parameters for the reliability and high quality of data transmission, so the phase noise is a quite important factor to determine the specification of wireless communication systems.

## II LITERATURE SURVEY

**A 40-GHz Quadrature LC VCO in 90-nm CMOS Technology**

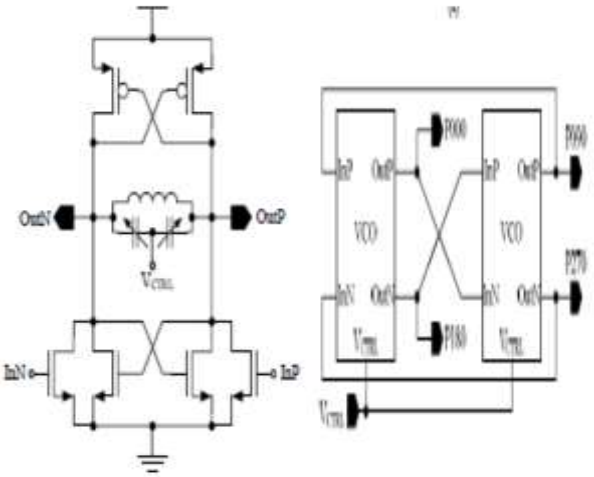

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Fig.1.LC VCO differential core and quadrature configuration

Quadrature phase oscillators are required to modulate/demodulate the orthogonal signals, which are important for modern digital communication techniques. Several alternatives have been proposed to generate the quadrature phases such as poly-phase filtering, injection locking, coupling differential oscillators.

Drawback of this Quadrature LC VCO is coupled VCOs are appropriate for low phase error, but there exists a trade-off between the quadrature accuracy and phase noise of the VCO. It also occupies larger area.

## III PROPOSED SYSTEM

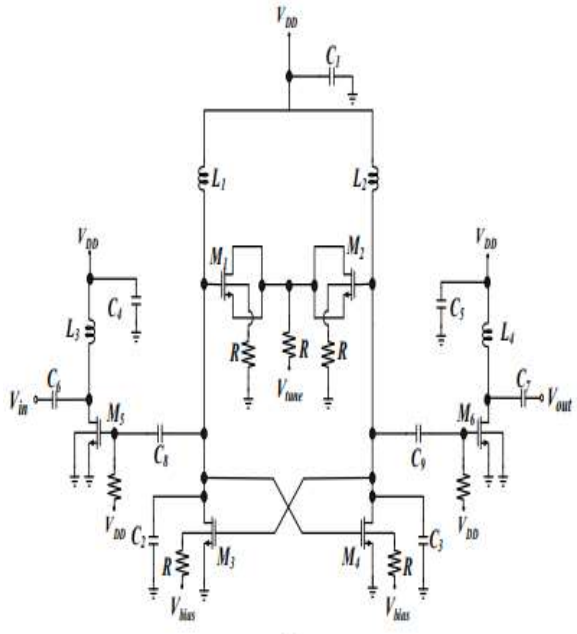


Fig. 2. (a) Schematic of the VCO

The cross-connection of NMOS differential pair(M3-M4) provides positive feedback. Capacitances of the tank consists of effective parasitic capacitors(C2 and C3) and varactor, which are made up of NMOS (M1 and M2).

In this NMOS varactor, the body is connected to ground to increase tuning range. The operation frequency is

$$f = \frac{1}{2\pi\sqrt{L(C+\Delta C)}} \quad (1)$$

generated by the LC-tank oscillator's capacitor varactor (M1and M2) add constant capacitance (C2,C3) and inductor (L1,L2) the oscillation frequency is To reduce power consumption, the circuit add the bias voltage (Vbias) in the NMOS (M3 and M4) differential pair's body. To avoid oscillator signal is too weak, we use a pair of buffer amplifier.

So this CMOS VCO provides better tuning range and phase noise performance compared to all other VCO's present till date. To compare the performance to VCO with others, our designed lower power consumption and better phase noise than others. With the formula:

$$FOM = L(f_{offset}) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mw}\right) \quad (2)$$

## IV RESULTS

### SCHEMATIC OF EXISTING

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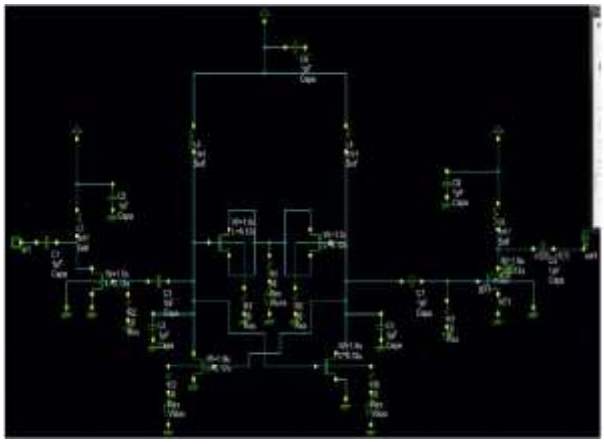
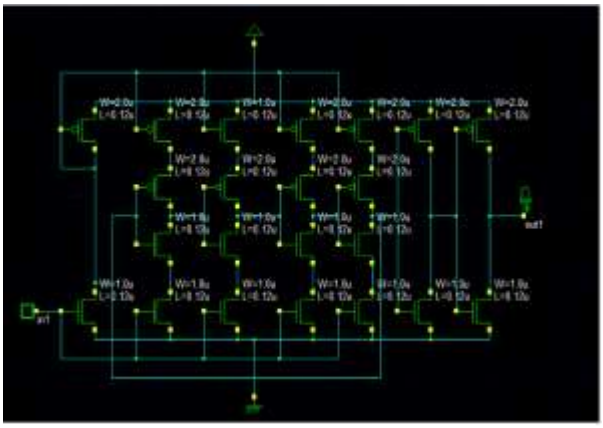
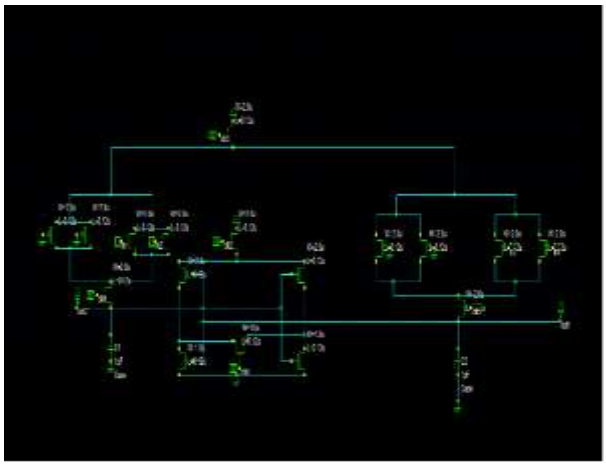
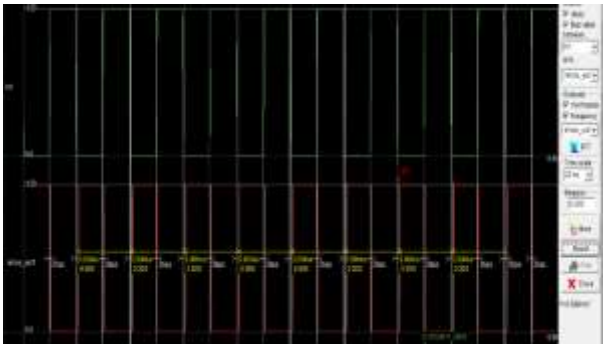


**Modified Circuit schematic**



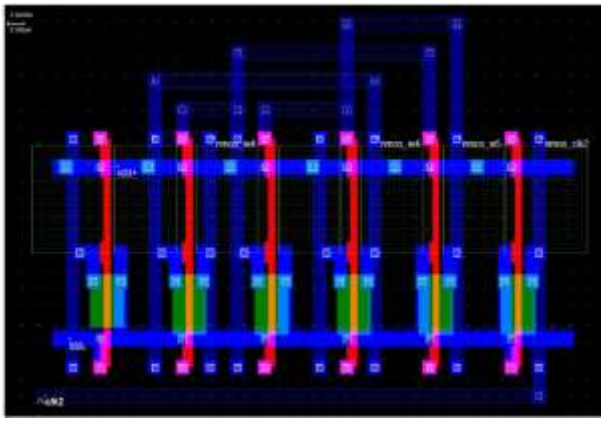
Simulated waveforms



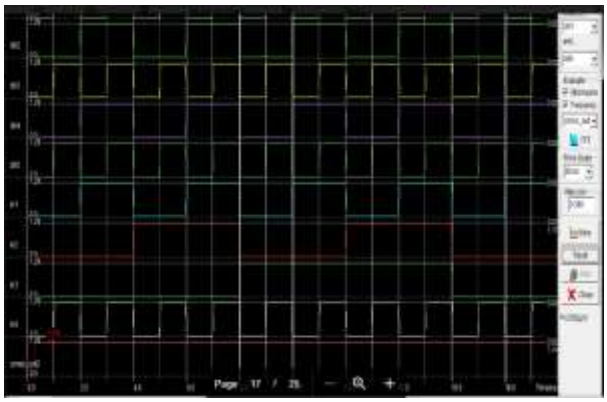


**LAYOUT DESIGN**

**SIMULATED WAVE FORMS**



Comparison table



**SCHEMATIC Of proposed**

| REF | TECH(µm) | Fosc(GHz) | Power(mv) | Lowest PN dBc/Hz | FOM |
|---|---|---|---|---|---|
| [4] | 0.13 | 40 | 11.25 | -90.3 | -170.8 |
| [3] | 0.18 | 40 | 27 | -99 | -176.7 |
| BASE PAPER | 0.18 | 40 | 4.5 | -101 | -186.5 |
| THIS WORK | 0.18 | 40 | 0.599 | -103.5 | -192.4 |

## V CONCLUSION

Power consumption has become one of the most important factor for high speed circuits so by reducing the power we improve the performance compared to previous designs.

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