International Journal of Research
Available at https://edupediapublications.org/journals

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 15
May 2018

Biquad filter design using VDCC (Earth resistor help in designing of biquad filter using VDCC)

Er. Shatanjay Mishra & *Er. Pavan Kumar*

[1]Dept. of ECE (VLSI & embedded system) Maharishi University of information technology Lucknow, UP (INDIA)
shatanjay272@gmail.com

[2]Head of Dept. of ECE Maharishi University of information technology Lucknow, UP (INDIA)
pavandohare25@gmail.com

Abstract— *(Analog VLSI can deal with nearly all real world issues and has extended its range of circuits (amplifier, filters, communication circuits, current comparators etc) for new information processing applications in numerous fields like integrated sensors, image processing, speech recognition, hand writing recognition etc.This lead to an increased interest in the evolution process of active elements which are used for analog signal processing.*
Current conveyors an excellent linear active element with high bandwidth, greater dynamic range and better high frequency response has evolved as a building block for higher efficiency blocks. Evolved in 1968 as the first generation current conveyor, the block gained huge reputation with the second generation in 1970 and the third generation in 1995.
Voltage Differencing Current Conveyor (VDCC) is emerging as quite flexible and versatile building block for analog circuit design. Here an attempt has been made to highlight the realization of the VDCC active block using MOSFETs and VDCC based biquad filter. The workability of the circuit is supported by PSPICE simulations using TSMC 0.18µm parameters.
Keywords- *VDCC, MOCCI, OTA, FILTERS (First order, second order, Biquad) etc.*

1. Introduction

It is widely accepted that all filters can be fabricated with the help of standard operational amplifiers. It is mainly used for audio application. For the creation of higher frequency ranges modern active functional blocks have been used. Recently, various kind of functional building blocks have been implemented, out of them only versatile and functional building blocks are useful for voltage differencing current conveyor (VDCC). VDCC based continuous time active RC filters have gained more attention in recent time. This branch of electronics having some useful advantages of the current conveyor filters and OTA filters, which is named as low supply voltages and power. Standard amplifiers are able to provide well developed IC topology and specific frequency ranges for signal processing. Since their inception, the VDCC have guided multiple of applications in signal processing circuits, for the development of many oscillators and filters. Sedra and Smith in 1968, first time introduced the principal of the current conveyor of first generation. After that multiple applications of current conveyors have been published by other people. After putting so much of efforts on research, current conveyors are still not available in the form of IC and, because of this reason this active block not being used in many analog circuit and system design applications by many developers. Some op-amps based applications on current conveyors are available, which can provide high speed and wide band, in the form of integrated circuits such as AD844, OPA660, and AD844. In 1968 when current conveyor was firstly introduced, the advantages of its applications were not very much clear over the conventional OP-amp. Moreover, it was just a beginning for the electronics industry to focus its efforts on the creation of applications s of the first generation of monolithic op-amps. At the end, the op-amp concept was able to create a good image in the minds of many analog circuit designers since its inception in the late 1940's. According to many IC manufactures an op-amp market was already there to be tapped and expanded. But it is now clear that analog designers are researching that the current conveyor offers several advantages over the conventional op-amp. A current conveyor circuit will able to provide a higher voltage gain over a larger signal frequencies under small or large signal conditions than a conventional op-amp circuit, results a higher gain frequencies product. However, current conveyors have added extra advantages in the development of an instrumentation amplifier, which does not depends on the external components, instead it is only depends on the absolute value of a single component.

2.PROPOSED WORK AND METHODOLOGY USED

VDCC transfers voltage and current in its correspondent terminals and provides trans-conductance gain which is electronically tunable. Different devices like filters, multipliers, simulators etc. can be designed efficiently using the VDCC. CMOS circuits for low pass, high pass and band pass filters are designed and simulated in PSpice tool using 180nm library. All the circuits and waveforms are included in this chapter. **PSpice** stands for ***Personal Simulation Program with Integrated Circuit Emphasis***. It is a circuit simulator for the simulation and verification of analog as well as mixed signal circuits. PSpice was first introduced by MicroSim in 1984. A file with code or schematic diagram also called net list is analyzed and simulated in PSpice. It also includes waveform viewer and program analyzer. There are three analyzes which can be done in PSpice. These analyzes are as follows:

Transient Analysis: This analysis is done when the circuits have time variant sources like sinusoidal sources or switched DC sources. In this analysis voltage at each node and current in each branch over a specific time interval are calculated and output is the instantaneous value.

DC Analysis: This analysis is done when the circuits have time invariant sources like steady state DC sources. In this analysis voltage at each node and current in each branch over a specific range of values are calculated. Linear Sweep and Logarithmic Sweep are some examples of this analysis.

AC Analysis: This analysis is done when the circuits have components with varying frequency for small signal. In this analysis magnitude and phase angle of voltage at each node and current in each branch over a specific range of frequencies are calculated.

Voltage differencing current conveyor

2.1 Introduction

It is well known that precisely tailored frequency filters can be produced with standard operational amplifiers but for audio application only. In higher frequency range it is better to use some of modern active functional blocks. Recently, various active building blocks have been introduced in [1], in which versatile and powerful building blocks are the voltage differencing current conveyor (VDCC). Continuous-time active RC filters based on the VDCC have recently found attractive considerable attention. This stems from inherent advantages of the current conveyor circuits and OTA circuits, namely low supply voltages and power, current operational mode possibility, well-developed IC topology and particularly a frequency range of the signal processing which can be higher than with circuits with the standard operational amplifiers.

VDCC provides electronically tunable transconductance gain in addition to transferring both current and voltage in its relevant terminals; it is very suitable for the design of various active filters or inductor simulators.

The circuit symbol of the proposed active element,VDCC, is shown in Fig. 4.2, where P and N are input terminals and Z, X, W_P and W_N are output terminals. Ideally, the VDCC is an active block which is the combination of OTA and MO-CCII as shown in Fig. 4.1.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 15
May 2018

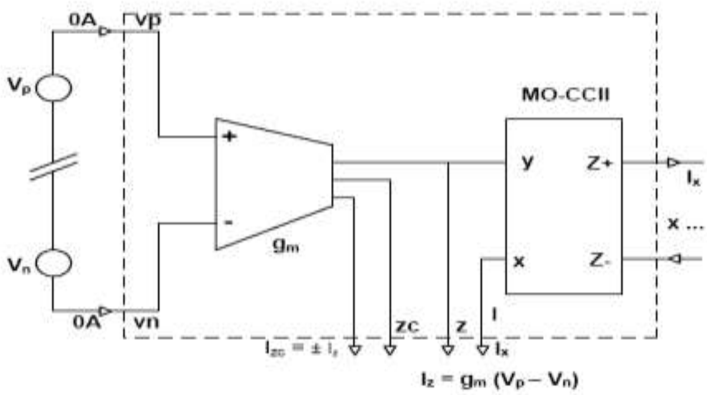

Figure 2.1: Internal structure of VDCC [17]

All of the terminals exhibit high impedance, except the X terminal.Using standard notation the port of an ideal VDCC.

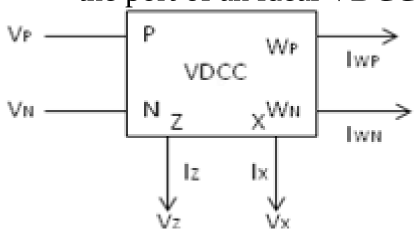

Figure 2.2: Voltage differencing current conveyor [17]

Using standard notation, the port relations of an ideal VDCC can be characterized by

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

According to the above matrix equation, the first stage can be realized by a balanced transconductance amplifier to convert the difference of the input voltages ($V_p - V_n$) into the output current (I_z) with transconductance gain of g_m and the second stage is a current conveyor used for transferring x-terminal current to W_p and W_n terminals. For a balanced CMOS transconductance amplifier, the parameter g_m can be given as

$$g_m = \sqrt{I_B}$$

where μ_n is the mobility of the carrier for NMOS transistors, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length and I_{B1} is bias current. In the VDCC block [2] in the input stage we have a trans-conductance amplifier and in the output stage we have a second generation current conveyor.

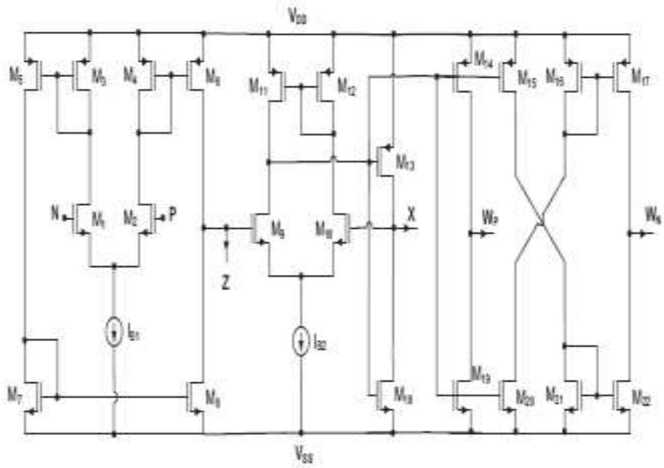

Figure 2.3: CMOS Realization of VDCC [18]

Table1: Transistors aspect ratios for the VDCC of Fig.1.3.

Transistors	W/L (m)
M1–M4	3.6/1.8
M5–M6	7.2/1.8
M7–M8	2.4/1.8
M9–M10	2.4/1.8
M11–M12	9/0.72
M13–M17	14.4/0.72

The CMOS schematic of VDCC shown in fig.4.3 was simulated in PSpice

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 15
May 2018

using TSMC CMOS 0.18µm model parameters [2]. The aspect ratios of the transistors used are given in Table 1. The supply voltages are chosen as V_{DD}=-V_{SS}= 0.9V, I_{B1} = 50µA and I_{B2} = -100µA. The following analysis has been carried out:

(i) DC sweep (to obtain the linear voltage for various current and voltage transfers),

(ii) AC sweep (to obtain the bandwidth of the device).

The following terminating impedances were used in characterization of the VDCC as Rz= 9kΩ, Rx= 100Ω, Rwp= 100Ω, Rwn= 100Ω. The input signal for AC sweep was taken as 3 mV with frequency 10MHz.

Different parameters obtained by PSpice Simulations of VDCC are listed as:
Transconductance g_m= 277µA/V
Power consumption = 0.90mW

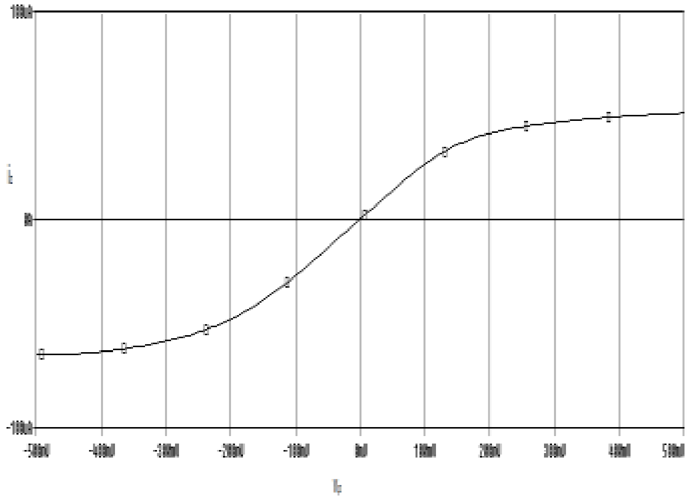

Figure 2.4: Input DC characteristic of VDCC

Although many circuits for the simulation of grounded and floating inductance using different active building blocks such as operational amplifiers, current conveyors, current feedback amplifiers, current differencing buffered amplifiers current differencing transconductance amplifiers , operational transconductance amplifiers , have been reported. In many active building blocks have been presented, and VDCC is one of them.

3. CALCULATION AND CASE STUDY

Here single voltage differencing current conveyor (VDCC) based second order filter is proposed. The proposed circuit employs one voltage differencing current conveyor (VDCC) as active elements together with capacitors an resistors as passive elements.

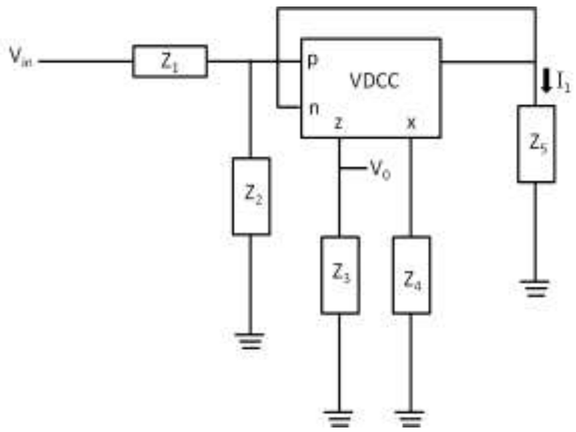

Figure 3.1: Circuit based on VDCC

Transfer Functions of Filter

Consider a circuit based on VDCC [6] which is used to generate the different equations for the different types of filters as shown in figure

In this circuit p, n are input terminals, z, x are output terminals,Z_1,Z_2 ,Z_3, Z_4 ,Z_5 are impedances and V_{in} is the input voltage.

$$V_p = \frac{Z_2}{Z_1 + Z_2} V_{in}$$

$$I_Z = g_m (V_p - V_n)$$

Since $V_n = I_1 Z_5$ & $I_1 = I_Z Z_3/Z_4$

Therefore $I_Z = g_m(V_P - I_Z Z_3 Z_5/Z_4)$

$$I_z = g_m V_p - I_z \frac{Z_3 Z_5}{Z_4} g_m$$

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 15
May 2018

$$I_z\left(1+g_m\frac{Z_3Z_5}{Z_4}\right)=g_mV_p$$

$$I_z\left(\frac{Z_4+g_mZ_3Z_5}{Z_4}\right)=g_mV_p$$

$$I_z=\frac{g_mV_pZ_4}{Z_4+g_mZ_3Z_5}$$

$$I_z=\frac{g_mZ_4}{(Z_4+g_mZ_3Z_5)}\frac{Z_2}{(Z_1+Z_2)}V_{in}$$

Since $I_O=I_Z Z_3$

Therefore

$$V_0=\frac{g_mZ_4Z_3}{(Z_4+g_mZ_3Z_5)}Z_1/(Z_1+Z_2)V_{in}$$

1 Low Pass Filter- A low pass filter is an electronic filter that passes signals with a frequency lower than a certain cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency. The general form of transfer function for low pass filter is given as follow –

$$T_{lp}(s)=\frac{V_{out}}{V_{in}}=\frac{K\omega_0^2}{s^2+s\frac{\omega_0}{Q}+\omega_0^2}$$

For Low Pass filter, let Z_2, Z_3 are capacitors and Z_1, Z_4, Z_5 are resistors so

put $Z_1 = Z_5 = Z_4 = R$ & $Z_2 = Z_3 = 1/sC$ in equation (1) where R is the resistors and C is capacitance, So

$$T_{lp}(s)=\frac{\frac{g_m}{RC^2}}{s^2+\frac{s}{CR}(g_mR+1)+\frac{g_m}{RC^2}}$$

2 High Pass Filter A high pass filter is an electronic filter that passes signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency. The general form of transfer function for high pass filter is given as follow

$$T_{hp}(s)=\frac{V_{out}}{V_{in}}=\frac{Ks^2}{s^2+s\frac{\omega_0}{Q}+\omega_0^2}$$

For High Pass filter, let Z_1, Z_5 are capacitors and Z_2, Z_3, Z_4 are resistors so

put $Z_2 = Z_3 = Z_4 = R$ & $Z_1 = Z_5 = 1/ sC$ in equation (1), So

$$T_{hp}(s)=\frac{s^2g_mR}{s^2+\frac{s}{CR}(g_mR+1)+\frac{g_m}{RC^2}}$$

3 Band Pass Filter A band pass filter is an electronic circuit that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range. The general form of transfer function for band pass filter is given as follows –

$$T_{bp}(s)=\frac{V_{out}}{V_{in}}=\frac{K\omega_0 s}{s^2+s\frac{\omega_0}{Q}+\omega_0^2}$$

For Band Pass filter, let Z_2, Z_5 are capacitors and Z_1, Z_3, Z_4 are resistors so

put $Z_1 = Z_3 = Z_4 = R$ & $Z_2 = Z_5 = 1/sC$ in equation (1), So

$$T_{bp}(s)=\frac{\frac{sg_m}{C}}{s^2+\frac{s}{CR}(g_mR+1)+\frac{g_m}{RC^2}}$$

4. RESULTS AND DISCUSSION ON SIMULATION

Simulation was performed using a CMOS realization of VDCC given in fig 2.3. To prove the theoretical validity of single VDCC biquad filter of for pole frequency (f_0) = 5MHz. The simulated center frequency of BPF was measured as 5.30 MHz. 3dB (cut-off) frequency of LPF and HPF were measured as 5MHz and 4.56MHz respectively.

To study the time-domain behavior of the proposed filter, an input sinusoidal signal of amplitude 10mV is applied. The transient response for low-pass, band-pass and high-pass are shown. To show the effectiveness of the proposed structure, sinusoidal signal of frequencies of 100 KHz, 100

MHz having amplitude of 10mV each is applied at the input of the low pass filter and high pass filter and sinusoidal signal of frequencies of 100 KHz, 5 MHz having amplitude of 10mV each is applied at the input of the band pass filter. The frequency spectrum of input and output are also given. It is clear that the 100 KHz signals is passed without attenuation and 100 MHz signal is significantly attenuated for low-pass response. There is appreciable reduction in amplitude of 100 KHz signal for both band-pass and high-pass responses. The sinusoidal signal of 5 MHz is passed through both band-pass and 100MHz through high-pass.

To study the impact of variation in resistance the Monte Carlo simulation (with 100 samples) has been carried out. The center frequency of band-pass response is taken as performance parameter. Figure 4.26 shows Monte Carlo simulations at 27◦C with 1% variations in resistance R_1. It may be noted that the variations affect the center frequency of the band-pass filter. It is found that there is 0.51% deviation in the mean value of the center frequency of band-pass response of proposed filter. Further, it is noted that the center frequency varies by a factor of 1.004 and 1.005 between the minimum and maximum values.

5.CONCLUSION AND FUTURE SCOPE

In this thesis, I have designed low pass, high pass and band pass filter circuits using voltage differencing current conveyor (VDCC). Each circuit structure has been simulated in PSpice simulator. All the circuits are made from CMOS transistors and analyzed using 180nm TSMC CMOS technology. These circuits work efficiently and consume less average power compared to other designs published in previous literatures.

In future more designs can be constructed and analyzed using different types of current conveyor with less number of CMOS transistors. We know that technology is getting advanced and delay time, average power consumption & chip area are the main concerns which we have to solve in less time. Therefore not only filters but other important devices can also be designed for particular application. Cost is also an important factor so circuits should be carefully designed.

6. References

1) *[1] P. V. Ananda Mohan, "Current-Mode VLSI Analog Filters: Design and Applications", Birkhäuser, Springer, 2003.*

2) *[2] K. C. Smith and A.S. Sedra, "The current conveyor - a new circuit building block", IEEE Proceedings, vol. 56 (8), pp. 1368-1369, August 1968.*

3) *[3] R. Senani, D. R. Bhaskar and A. K. Singh, "Current Conveyors: Variants, Applications and Hardware Implementations", Springer, 2014.*

4) *[4] A. S. Sedra and K. C. Smith, "A second generation current conveyor and its application", IEEE Trans Circuit Theory, pp. 132-134, 1970.*

5) *[5] A. P. Naik, N. Devashrayee, "Cmos Second Generation Current Conveyors", Lap Lambert Academic Publishing GmbH KG, 2012.*

[6] J. W. Horng, Z. R. Wang, C.C. Liu, "Voltage-Mode Low pass, Band pass and Notch Filters Using Three Plus-Type CCIIs", IEEE Journal on Circuits and Systems, pp. 34-37, 2011.

[7] H. A. Kuntman, "New Advances and Possibilities in Active Circuit Design", International Conference on Development and Application Systems, Romania, 2010.

[8] A. Fabre, "Third Generation Current Conveyor: A New Helpful Active Element", IEEE Electronics Letters, vol. 31(5), pp. 338-339, March 1995.

[9] M. Yildiz, S. Minaei, S. Tiirkoz, H. Kuntman, "High Performance CMOS Realization of the Third Generation Current Conveyor (CCIII)", IEEE Circuits and Systems 45th Midwest Symposium, vol. 1, pp. 307-310, August 2002.

[10] A. M. Soliman, El-Adway, H. O. Elwan, "A Novel Fully Differential Current Conveyor and Its Application for Analog VLSI", IEEE Transactions on Circuits and Systems, vol. 47 (4), pp. 306-313, April 2000.

[11] S. Zhixing, W. Chunhua, L. Haiguang, "New CMOS Current-Controlled Second Generation Current Conveyors", IEEE Circuits and Systems for Communications 4th International Conference, pp. 333-337, may 2008.

[12] Z. Qiujing, W. Chunhua, "Current Controlled Fully Balanced Current Conveyor", IEEE Conference on Circuits and Systems, pp. 1062-1065, November 2008.

[13] H. Elwan, M. Ismail, H. A. Alzaher, "A CMOS Fully Balanced Second-Generation Current Conveyor", IEEE Transactions on Circuits and Systems-II, vol. 50 (6), pp. 278-287, June 2003.

[14] S. Minaei, E. Yuce, "ICCII-Based Universal Current- Mode Analog Filter Employing Only Grounded Passive Components", Springer Analog Integrated Circuits and Signal Processing, vol. 58 (2) , pp. 161-169 , 2009.

[15] Mohd. S. Ansari, S. Maheshwari, "Catalog of Realizations for DXCCII using Commercially Available ICs and Applications", Radio engineering, vol. 21, pp. 281-289, April 2012.

[16] E. Yüce ,S. Minaei , I. Myderrizi , "DXCCII-Based Grounded Inductance Simulators and Filter Applications", Micro-electron Journal, 2011.

[17] D. Biolek, R. Senani, V. Biolková, Z. Kolka, "Active Elements for Analog Signal Processing: Classification, Review, and New Proposals", Radio Engineering, vol. 17 (4), pp. 15- 32, December, 2008.