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New Multilevel Inverter with Resonance Switched Capacitor Converter

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Abstract— *In this paper proposes a novel multilevel DC-AC inverter. A seven level AC output voltage is generated using the proposed multilevel with the befitting gate signals design. The low-pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals' design. The switching losses and the voltage stress of power devices can be reduced in the proposed multilevel inverter. The operating principles of the proposed inverter and the voltage balancing method of input capacitors are discussed. The multilevel inverter is controlled with sinusoidal pulse-width modulation (SPWM). By using the simulation results we can analyze the that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.*

Index Terms—DC–AC inverter, digital signal processor (DSP), maximum power point tracking (MPPT), multilevel.

I. INTRODUCTION

Nowadays Multi Level Inverter (MLI) plays a vital role in the field of power electronics and being widely used in many industrial and commercial applications. Moreover the advantages like high quality power output, low switching losses, low Electro-Magnetic Interference (EMI) and high output voltage made multilevel inverter as a powerful solution in converter topology. As a result of high-technology development, the demand and the quality of electric power are higher than before. Because of the advancement of semiconductor, the specification of power device and power conversion technique is promoted. One of the power converters which can transform dc–ac is called inverter. Generally multilevel inverter configuration is classified into (1) Diode Clamped Multilevel Converter refer shown below[3],[4]-[5] (2) Flying Capacitor Multilevel Converter (FCMC) refer shown below[3].(3)Cascaded Multilevel Converter (CMC) refer shown below[7]-[6],[8].The operation of all these three configurations were compared and analyzed in terms of reliability, feasibility and efficiency. Inverter is the inter medium which transmits power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid composed of renewable energy shown in Fig. 1.

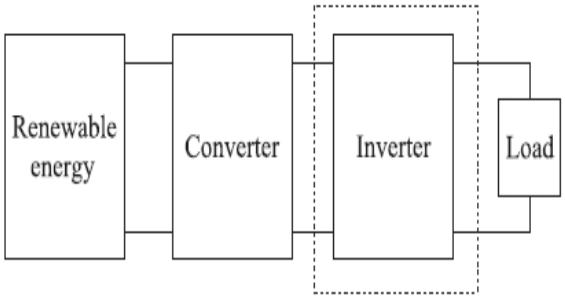

Fig. 1. Block diagram of renewable system.

To satisfy different demands and characteristic of loads, the output frequency and voltage have to change with different loads [1]–[3]. In recent years, the amount of power equipment is increasing. Therefore, the harmonic pollution of power system becomes more serious.

The purpose of the multilevel topology is to reduce the voltage rating of the power switch. Therefore, it usually is used at high-power application. By combining output voltages in multilevel form, it has advantages of low dv/dt, low input current distortion, and lower switching frequency. As a result of advantages of multilevel topology, several topologies have emerged in recent years [7], [8]. A novel multilevel inverter is designed and implemented in this paper. The major feature of the proposed topology is the reduction of power components. The sinusoidal pulse-width modulation (SPWM) is used to control proposed circuit.

II. POWER STAGE

A. Circuit Configuration

Fig. 2 shows the proposed novel topology used in the seven level inverter.

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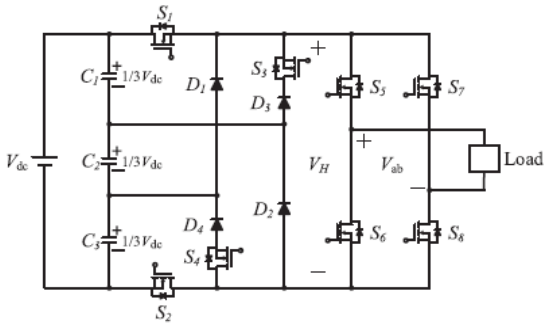

Fig. 2. Proposed seven-level inverter topology.

An input voltage divider is composed of three series capacitors C1, C2, and C3. The divided voltage is transmitted to H-bridge by four MOSFETs, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design.

B. Operating Principles

1) The required seven voltage output levels (±1/3Vdc, ±2/3Vdc,±Vdc, 0) are generated as follows. 1) To generate a voltage level Vo = 1/3Vdc, S1 is turned on at the positive half cycle. Energy is provided by the capacitor C1 and the voltage across H-bridge is 1/3Vdc. S5 and S8 are turned on, and the voltage applied to the load terminals is 1/3Vdc. Fig. 3 shows the current path at this mode.

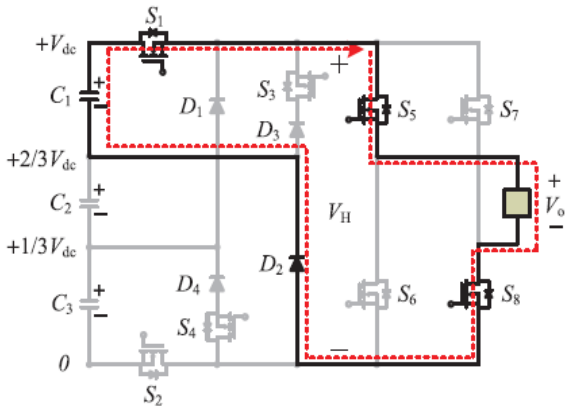

Fig. 3. Switching combination of output voltage level 1/3Vdc.

2) To generate a voltage level Vo = 2/3Vdc, S1 and S4 are turned on. Energy is provided by the capacitor C1 and C2. The voltage across H-bridge is 2/3Vdc. S5 and S8 are turned on, and the voltage applied to the load terminals is 2/3Vdc. Fig. 4 shows the current path at this mode.

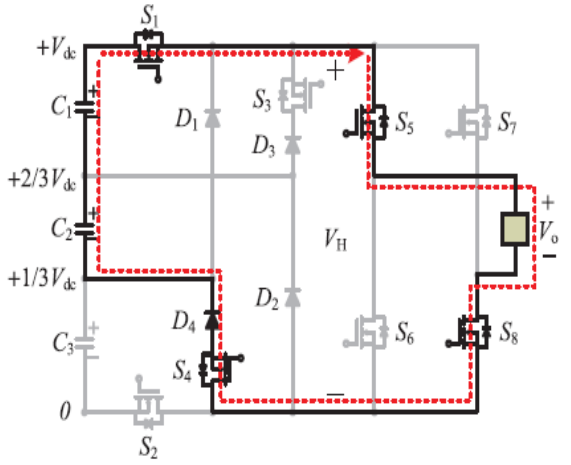

Fig. 4. Switching combination of output voltage level 2/3*V*dc.

3) To generate a voltage level Vo = Vdc, S1 and S2 are turned on. Energy is provided by the capacitor C1, C2, and C3.

The voltage across H-bridge is Vdc. S5 and S8 are turned on, and the voltage applied to the load terminals is Vdc. Fig. 5 shows the current path at this mode.

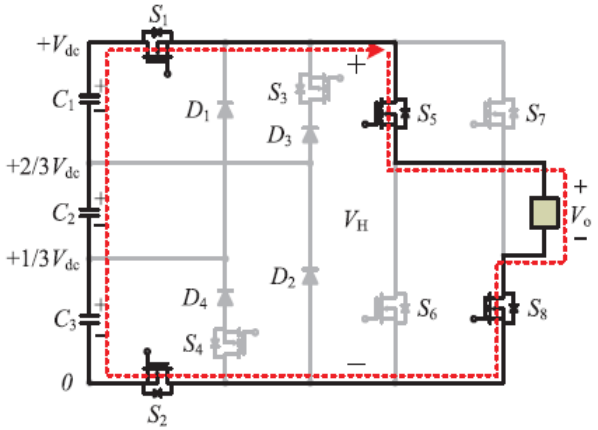

Fig. 5. Switching combination of output voltage level *V*dc.

4) To generate a voltage level Vo = −1/3Vdc, S2 is turned on at the negative half cycle. Energy is provided by the capacitor C3, and the voltage across H-bridge is 1/3Vdc. S6 and S7 are turned on, and the voltage applied to the load terminals is −1/3Vdc. Fig. 6 shows the current path at this mode.

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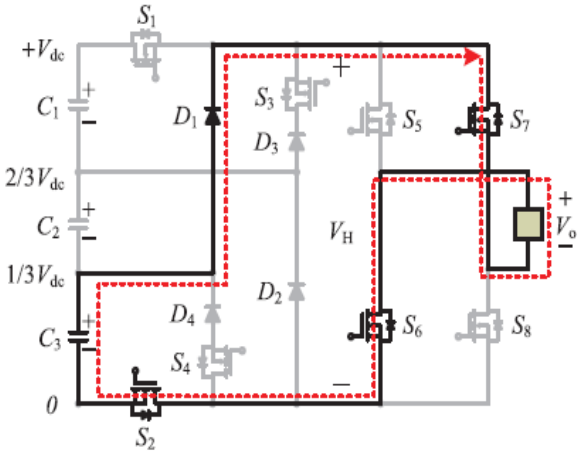

Fig. 6. Switching combination of output voltage level −1/3*V*dc.

5) To generate a voltage level Vo = −2/3Vdc, S2 and S3 are turned on. Energy is provided by the capacitor C2 and C3. The voltage across H-bridge is 2/3Vdc. S6 and S7 are turned on, and the voltage applied to the load terminals is −2/3Vdc. Fig. 7 shows the current path at this mode.

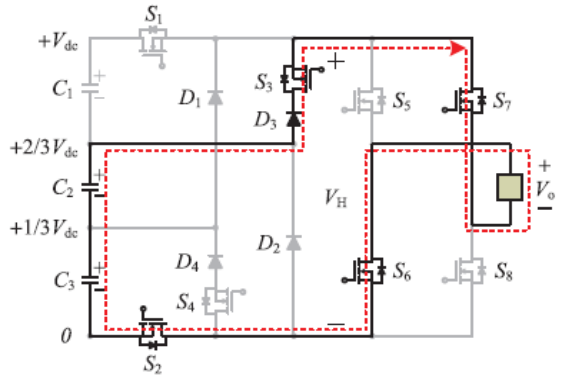

Fig. 7. Switching combination of output voltage level −2/3*V*dc.

6) To generate a voltage level Vo = −Vdc, S1 and S2 are turned on. Energy is provided by the capacitor C1, C2, and C3, the voltage across H-bridge is Vdc. S6 and S7 is turned on, the voltage applied to the load terminals is −Vdc. Fig. 8 shows the current path at this mode.

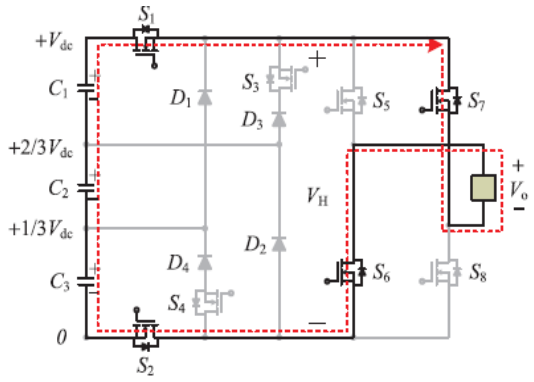

Fig. 8. Switching combination of output voltage level −*V*dc.

7) To generate a voltage level Vo = 0, S5 and S7 are turned on. The voltage applied to the load terminals is zero. Fig. 9 shows the current path at this mode.

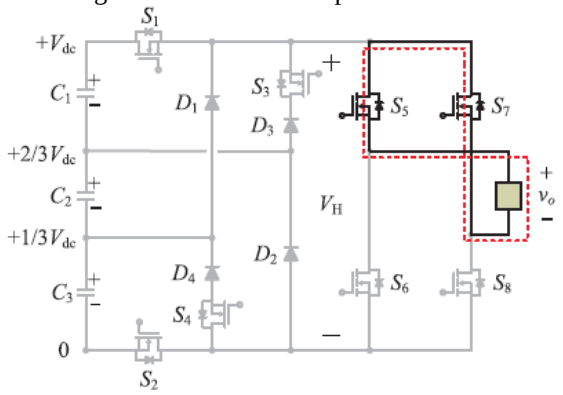

Fig. 9. Switching combination of output voltage level 0.

Table I lists the switching combinations at different output levels.

TABLE I SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

C. Topology Comparison

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Table II presents the number of components required to implement a seven-level inverter using the proposed topology

TABLE II
COMPONENTS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

and three previously ones [9], [10] that can be considered as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multicell inverter. Table II shows that the new topology achieves the reduction in the number of power devices. Table III shows the voltage stress comparison between different type inverters**.**

TABLE III VOLTAGE STRESS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

III. VOLTAGE BALANCING CIRCUIT BASED ON RSCC

Since the voltage deviation causes larger harmonics distortion in the output voltage, voltage-balancing circuits are indispensable for the capacitors in the multilevel inverters [11]–[15]. By using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Fig. 10 shows the circuit configuration of a unit of the resonant switched-capacitor converter (RSCC).

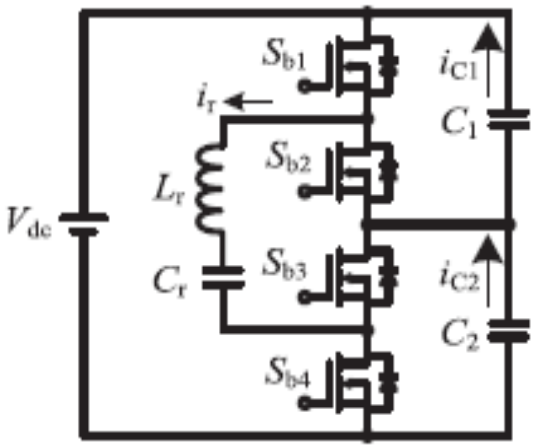

Fig. 10. Circuit configuration of RSCC

The duty cycle of every switch is equal to 50%. The voltage of C1 is higher than the voltage of C2. Since the average current of C1 is higher than that of C2 at one switching cycle, most of the charges flow from C1 to C2. After few switching cycles, the voltages of C1 and C2 are equal. Fig. 11 shows the waveforms of the RSCC.

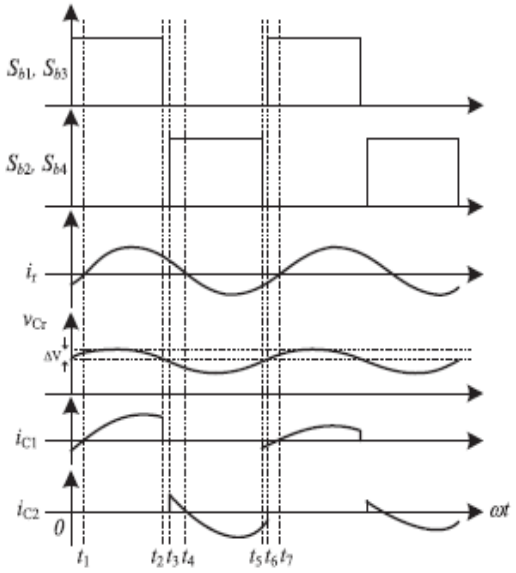

Fig. 11. Waveforms of RSCC.

Fig. 12 shows the configuration of proposed seven-level inverter with RSCC.

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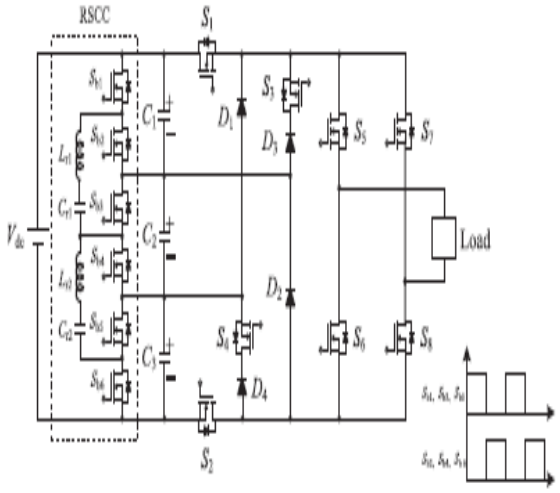

Fig. 12. Proposed multilevel inverter with RSCC.

To apply RSCC at seven-level configuration, two switches Sb5 and Sb6, resonant inductor Lr, and resonant capacitor Cr are added. In this application, switches Sb1, Sb3, and Sb5 are turned on at the same time; Sb2, Sb4, and Sb6 are turned on at the same time. The duty of each switch is equal to 50%.

IV. APPLICATION OF SPWM

In this paper, several triangular carriers are distributed by phase disposition technique. The advantage of phase disposition technique is uncomplicated to realize and less total harmonic distortion [16], [17]. These carriers are compared with a reference sine waveform vsin to get signal of switches. The peak-to-peak value of triangular carrier is ˆ Vtri. The frequency of carrier is switching frequency of inverter. The peak value of reference sine wave is ˆ Vsin, and the modulation index mA is defined as

$$\boldsymbol{m_A} = \frac{\hat{V}_{sin}}{3.\hat{V}_{tri}} \qquad (1)$$

According to (1), the relationship between the peak value of output sine wave and mA can be expressed as

$$\boldsymbol{V_o} = \boldsymbol{m_A}.\boldsymbol{V_{dc}} \qquad (2)$$

Fig. 13 shows the reference sine wave, carriers, and control signals of switches. The method that determines switch signals in Fig. 12 is as follows.

1) vsin < 0 and vsin > vtri2 → S2 are turned on

2) vsin > vtri4 → S4 is turned on.

3) vsin < vtri8 → S7 is turned on.

4) vsin > vtri8 → S8 is turned on

5) vsin > 0 and vsin < vtri1 → S1 are turned on.

6) vsin < vtri3 → S3 is turned on.

7) vsin > vtri6 → S5 is turned on.

8) vsin < vtri6 → S6 is turned on.

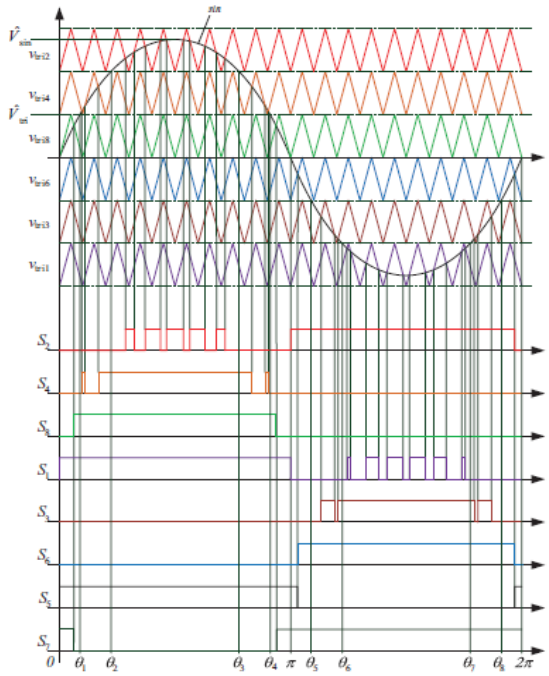

Fig. 13. Reference sine wave, carriers, and control signals of switches.

V. PI CONTROL USED IN MODIFIED SPWM

Modified SPWM based on PI control is used in this paper [18], [19]. Fig. 14 shows the block diagram of PI control. The block diagram can be expressed in S domain as

$$u(s) = \left[K_p + \frac{K_i}{s}\right] e(s) \qquad (3)$$

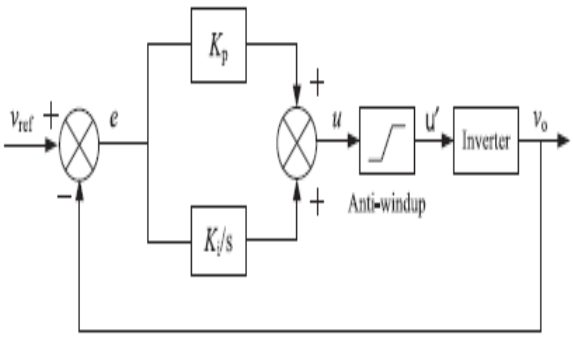

Fig. 14. Block diagram of PI control.

From (3), the equation can be transformed in the Z domain as

$$u(z) = \left[K_p + \frac{K_i}{1-z^{-1}}\right] e(z) \qquad (4)$$

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Then, transform (4) becomes a difference equation is expressed as

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1] \quad (5)$$

Fig. 15 shows system configuration and control block.

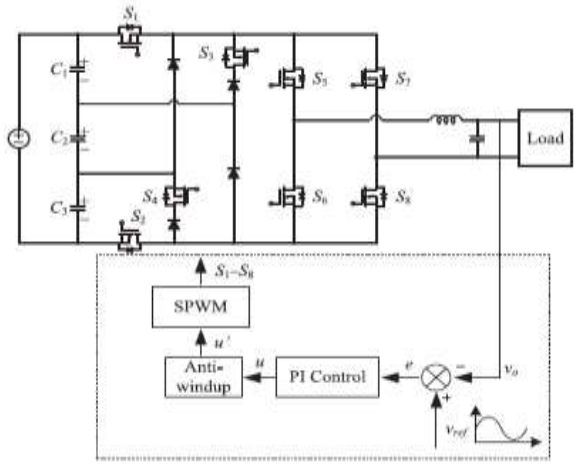

Fig. 15. Seven-level inverter with control algorithm.

System detects output voltage first and compares this signal with a built-in reference. Then, the system feedbacks an error to PI controller. Finally, the PI controller exports a control signal to gate driver. The main idea of modified SPWM is to record the previous error of output voltage and generate a suitable correction at the latest cycle. Because the frequency of carrier is 18 kHz and the frequency of output sine wave is 60 Hz, the number of times of switching is 300 times. Fig. 16 shows the schematic of modified SPWM. vref[n] is defined as the reference output voltage, vo[n] is the feedback of output voltage, and e[n] is error between reference output and feedback output which is expressed as

$$e[n] = v_{ref}[n] - v_o[n] \quad (6)$$

LetK1 = Kp + Ki,K2 = Kp, then e[n] is multiplied byK1 and e[n − 300] multiplied by K2.

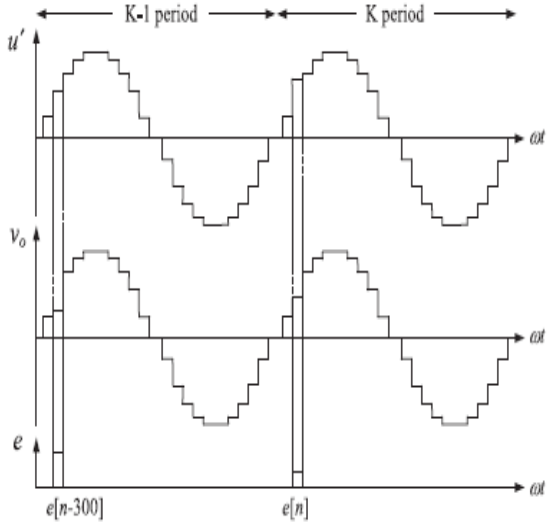

Fig. 16. Schematic of modified SPWM

Then, add the previous output signal u[n − 300]. Finally, it can obtain the output of PI controller after the process by the anti-windup.

$$u'[n] = K_1 e[n] - K_1 e[n-300] + u'[n-300] \quad (7)$$

TABLE IV
SPECIFICATIONS OF THE PROPOSED INVERTER

Input voltage V_{dc}	400 V
Output voltage V_o	220 V_{rms}
Rated output power P_o	2 kW
Switching frequency f_s	18 kHz

Simulation scope

The MLI topologies are compared with each other and with a conventional two-level PWM inverter to investigate the differences between multilevel technology and ordinary two-level technology. For the comparison quality issues such as harmonic components and THD are used together will calculated switching and conduction losses. The capacitor voltage balance problem have been investigated for both MLI topologies.

SIMULINK DIAGRAM FOR CONVENTIONAL MULTILEVEL INVERTER

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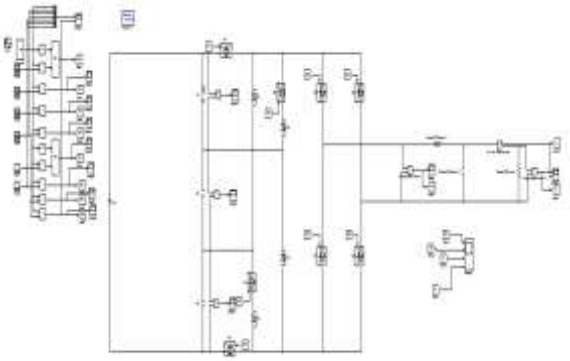

Fig 17..simlink model of conventional multilevel inverter

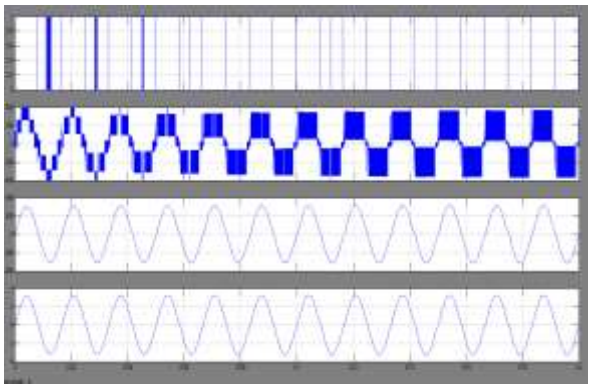

Fig.18 Waveforms of vgs1, vab, vo, and io.

Fig 18 shows the output voltage waveform vab showing the desired seven voltage levels and output waveform vo. The seven voltage levels in the figure are ±133, ±267, ±400, and 0 V. So the given voltage input was 400V we will get output volage vo=220V, output current io=3A at power 660 watts. Fig 19 shows THD across output voltage.

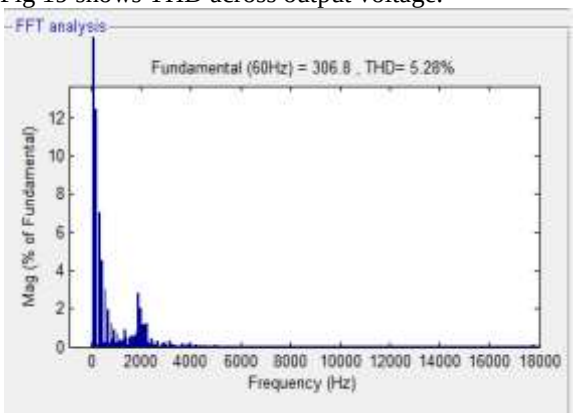

Fig 19. Output voltage harmonic spectrum calculated by FFT.

SIMLINK DIAGRAM FOR PROPOSED MULTILEVEL INVERTER

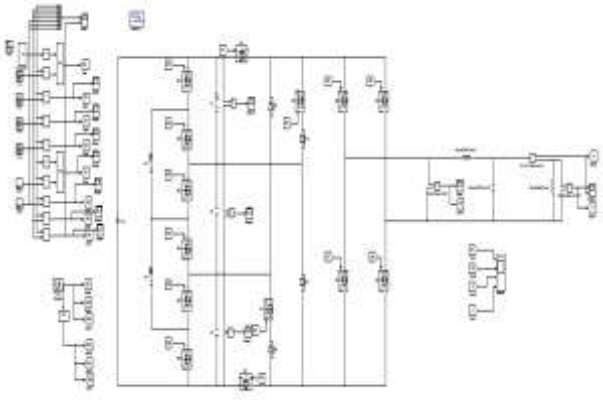

Fig 20.simlink model of proposed multilevel inverter

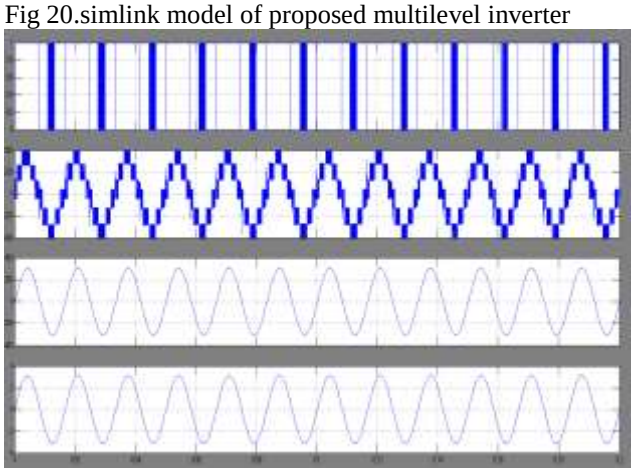

Fig 21. Waveforms of vgs1, vab, vo, and io.

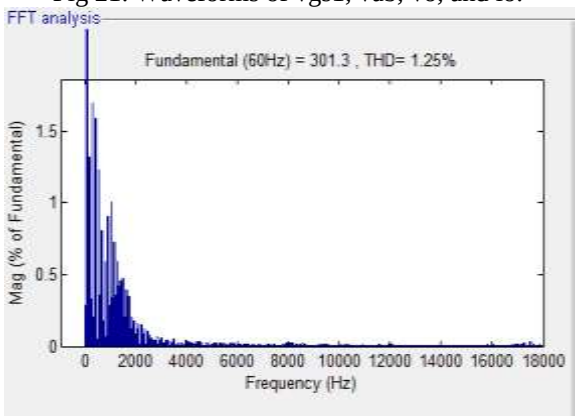

Fig 22. Output voltage harmonic spectrum calculated by FFT.

Fig 21 shows the output voltage waveform vab showing the desired seven voltage levels and output waveform vo. The seven voltage levels in the figure are ±133, ±267, ±400, and 0 V. So the given voltage input was 400V we will get output voltage vo=220V, output current io=3A at power 660 watts.

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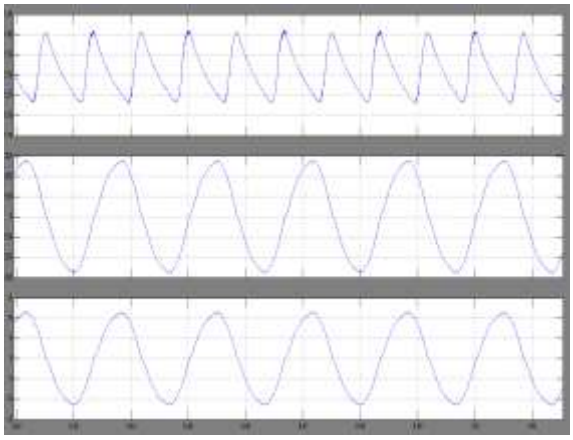

Fig 23. waveforms for Vc2,Vo,Io at 1000W.

Fig.23 shows capacitor voltage VC2, output voltage vo, and output current io at 1000W. In this figure, the capacitor voltage is 133 V. Thus, the function of voltage balancing is achieved. Multilevel structure is usually used in inductive loads such a motor. Thus, this paper applies the proposed topology in inductive load.

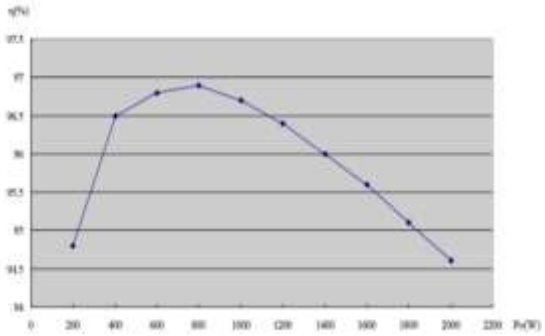

Fig 24. efficiency of the proposed inverter.

VII. CONCLUSION

A novel multilevel DC–AC inverter is proposed multilevel generates seven-level ac output voltage with the appropriate gate signals design. The main idea of the proposed configuration is to reduce the number of power device. The reduction of power device is proved by comparing with traditional structures. By using simulation results we can analyze a seven-level inverter with 400-V input voltage and output 220 Vrms/2kW is implemented. Simulation results show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%. The proposed circuit produces required seven level output voltage having low harmonics with reduced number of components when compared to conventional methods.

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