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10T SRAM-VDD PRE-CHARGE USING READ PORT FOR LOW SWITCHING POWER AND LOW RBL LEAKAGE

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ABSTRACT: In order to achieve a longer battery life suppression of energy consumption is vital. A demand for design methods for less energy consumption is increasing. The subthreshold scaling can reduce energy per cycle significantly by the scaling of supply voltage (VDD) below threshold voltage (Vth). Threshold voltage of CMOS technology represents the value of the gate-source voltage when the current in a MOS transistor starts to increase significantly since the conduction layer just begins to appear. MOS transistor can also function with a supply voltage below its threshold voltage (Vth), which is referred to as sub-threshold operation or weak-inversion of a transistor. The circuits that work under a supply voltage in the sub-threshold range are named as sub-threshold circuits. In ultra low power design, the operation of circuit in subthreshold regime is most important and the SRAM circuit has the limitation of read disturb. In order to eliminate this limitation The Single-ended design is used. In this paper we propose the 10T SRAM cell. In this paper focus is mainly on the stability of the cell which is affected by the process parameter variations.

KEYWORDS: SRAM, Subthreshold, CMOS, Power Dissipation.

I. INTRODUCTION

In order to reduce power dissipation, techniques like design of circuits with power supply voltage scaling, power gating and drowsy method are used. Lowering the supply voltage decrease the dynamic power in a quadratic fashion and the leakage power in exponential manner, along with reduction in noise margin. Most of SRAM arrays are based on minimizing the active capacitance and reducing the swing voltage. In submicron technologies gate leakage and sub threshold leakage are the primary sources of leakage currents. Techniques like forward body biasing methods and dual Vt are employed for subthreshold leakage, high dielectric constant gate technology is used in order to reduce the gate leakage current. In sub threshold SRAMs power supply voltage (VDD) is lower than the transistor threshold voltage (Vt) and the sub threshold leakage current is the operating current.

During writing operation the energy loss is higher than during reading in conventional SRAM, since there is full swing of voltage in bit lines whereas the bit line voltage swing is very less during reading. The main source of energy loss is during write operation, the transition from 1 to 0. The power consumption by bit lines during writing is proportional to the bit line capacitance, square of the bit line voltage and the frequency of writing. There is a powerful approach in which the energy stored in the bit line capacitance that is normally lost to ground is collected and pumped back into the source. This is known as energy recovery approach. Energy stored in the bit lines is recycled by the help of switches to adjacent bit lines in order to save energy in bit line charge- recycle method.

This method reduces the swing voltages to a low swing voltage. Based on whether energy recycling is done only during writing cycle or during both writing and reading cycles, there are variants. The circuit operation in the subthreshold regime has paved path towards ultralow power embedded memories, mainly static RAMs (SRAMs). However, in subthreshold regime, the data stability of SRAM cell is a severe problem and worsens with the scaling of MOSFET to subnanometer technology. Due to these limitations it becomes difficult for operating the conventional 6-transistor (6T) cell at ultralow voltage (ULV) power supply. In addition, 6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation.

II. EXISTED SYSTEM

SRAM cell must robustly operate under hold, read, and write mode. An SRAM cell utilizes the positive feedback of cross-coupled inverters (INVs) to store a single bit of information in a complementary fashion. Access transistors provide the mechanism for the read and write operation. Before every access, column Bit Line (BL) pair (BL and BLB) is precharged to the supply voltage. For the write operation, one of the precharged BLs is discharged through the write driver.

Fig. 1 shows a single column of M 6T SRAM cells, where one cell is accessed in read mode with data = 0 (Qa = 0), while other M − 1 cells are in the hold mode. Leakage components are labeled, and for the worst case leakage, all M − 1 cells store data = 1 (Qu = 1). Iread flows from BL to the VSS through AL and NL of the accessed cell, and the BL voltage is reduced.

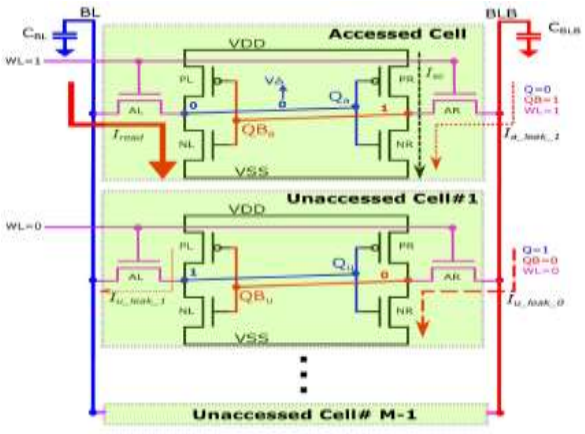

Fig. 1. Conventional 6T SRAM read.

The unaccessed cell on the BL exhibits BL leakage. IuLeak0 is the main component of BL leakage while IuLeak1 is negligible, as VDS of AR of the unaccessed cell is large, while VDS of its AL is very small. These leakage components reduce the differential BL voltage

development. As there are a large number of cells in a single column, the worst case BL leakage can decrease BLB voltage enough to make an erroneous read.

Thus, Iread must be greater than (M − 1) × IuLeak0, where M is the number of cells in a single column. During read operation, the internal node of the 6T cell storing a zero (Qa) lies in the read current path and its voltage increases during the read operation. This increase in voltage is dependent upon transistor sizing. For a successful read operation, β ratio must be larger than 1 (typically 2 to 3). The vulnerability of the internal nodes of an SRAM cell is captured through metrics Hold Static Noise Margin (HSNM), Read Static Noise Margin (RSNM), and Write Noise Margin (WNM) / write trip point (WTP) during hold, read, and write mode, respectively.

The increase in node Qa voltage not only decreases the cell stability, but also increases the short-circuit current from VDD to VSS and lets pass (now) the higher amount of leakage current from BLB (IaLeak1). This decreases the differential BL voltage and requires the increases in WL pulse duration. A wider read pulse can cause dynamic instability and increases the power dissipation. In addition, for a successful write operation, access transistors of the 6T must be strong enough to take over the pull-up pMOS transistors. Thus, γ ratio, must be smaller than 1. However, a stronger pMOS is beneficial for read operation and a weaker pull-down nMOS is beneficial for write operation to let access transistors have more strength for injecting current. Thus, proper sizing is required for specific conditions and application.

The conventional 6T SRAM has two BL s (BL and BLB), and for each read operation one of the BLs is decreased. We can model 6T SRAM by a single BL with an activity factor of 1. Leakage power dissipation is highly data dependent. In Fig. 1 AR of the unaccessed cell is OFF (having VGS = 0 V), while it's VDS = VDD, which exhibits large leakage. In essence, 6T SRAM has conflicting read and write requirements and transistor sizing cannot be done independently. Also, 6T has inherit RSNM problem as the read current passes through the cell internal node and it further degrades with VDD scaling. Also, being considered as baseline design, 6T has overall a higher power dissipation, and higher BL leakages, as the low power techniques employ a certain mechanism to lower the dynamic power dissipation, e.g., charge sharing and hierarchical BL and the leakages (by employing virtual rails).

III. PROPOSED SYSTEM

The 10T SRAM cell was designed to provide ultralow leakage for subthreshold operation. Read Bit Line (RBL) leakage is substantially reduced at the cost of area and performance. The proposed 10T SRAM cell with Single Ended (SE) RBL is shown in Fig. 2. We have added a 4T read port to the 6T cell to decouple the internal nodes during the read operation. Read port contains an INV P1-N1 driven by node QB, and a transmission gate (TG) P2-N2. The output (Z) of the INV is connected to RBL during the read operation through TG, which is controlled by (read) control signals. Furthermore, read port is powered by virtual power

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rails, VDD and VSS, which are dynamically controlled. These virtual power rails (control signals) run horizontally, and have the true rail values only during the read operation. For the RBL leakage reduction, both the virtual rails have the same level as the precharge level of RBL.

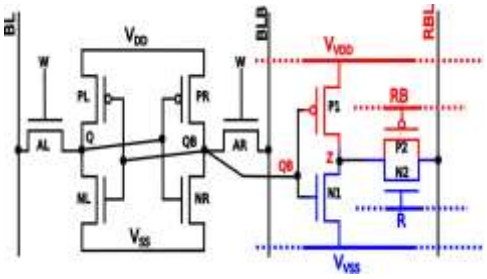

Fig. 2. Proposed 10T SRAM cell with row-wise read port dynamic power lines.

The proposed 10T SRAM is precharged by VP supply, which has a value half that of the supply voltage i.e., VP = vdd/2. For the read operation, R goes high and RB goes low and thus the transmission gate (TG) is activated to connect RBL to the node Z. If complementary data node (QB) is 0, then N1 is OFF and P1 connects node Z to the VDD, which is high for the read operation. Thus, the read current flows from VDD (having value of vdd) to RBL (which has value of vdd/2) through P1-TG. Hence, the RBL voltage increases toward the vdd level. Now, for a read-0 operation (i.e., QB = 1), P1 is turned OFF and N1 connects node Z to the VSS, which is low (0 V) during the read operation.

Thus, the read current flows from RBL having value vdd/2 to the GND through TG-N1, and hence RBL voltage decreases toward 0V. For the efficient read operation, we have utilized the boosted read (R and RB) signals which are nominal signal levels. This allows higher current to flow in both the directions. Boosted signals have been used to improve the performance degradation due to the half-vdd swing available for each read operation, as is the proposed precharging scheme. The levels of control signals and the change in RBL voltage during read, precharge, and hold mode.

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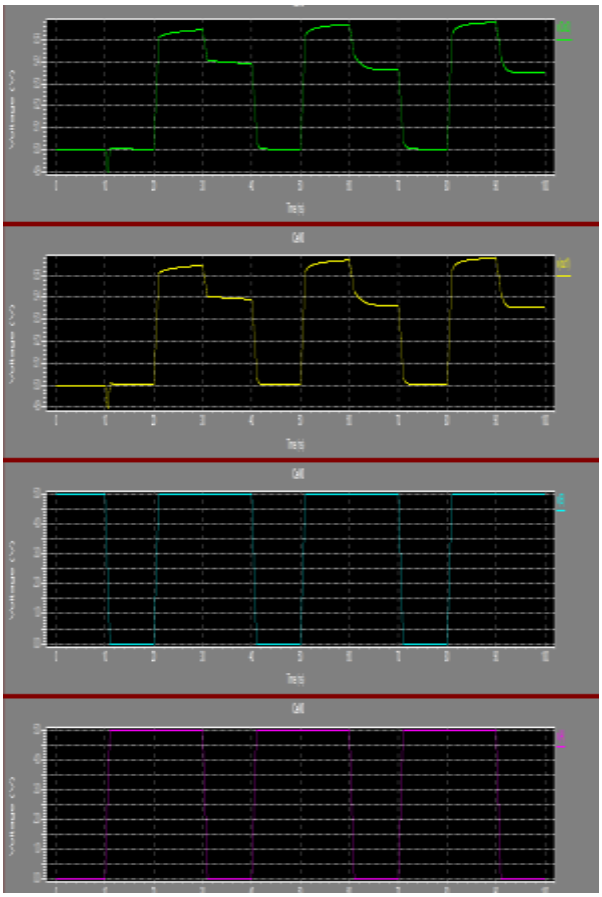
IV. RESULTS



V.CONCLUSION

In this paper, we have presented our 10T SRAM cell that uses a 4T read port and SE RBL. RBL is precharged at half the supply voltage and, during the read operation, is charged or discharged according to the bit stored. For a read-0 operation, RBL discharges through TG and nMOS transistor, and for the next precharge, RBL is supplied current by VP. For a read-1 operation, RBL is charged from vdd/2 to vdd by virtual read port. For the next precharge, RBL level is decreased and current flows from RBL to VP. By precharging through VP (which is half vdd) and charge recycling mechanism, 10T SRAM cell only dissipates half the average read dynamic power compared with 6T.

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