International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 15
May 2018

High-Speed Truncated Roba Multiplier for Energy-Efficient Digital Signal Processing

[1]PANIGRAHI VENKATA ARUNAKUMAR, [2]S. SRI VIDYA
[1] M.tech-student, Chaitanya institute of science and technology, Madhavapatnam, East Godavari, Kakinada, A.P, 533005.
[2] Associate Professor & HOD, Dept. Of ECE, Chaitanya institute of science and technology, Madhavapatnam, East Godavari, Kakinada, A.P, 533005.

ABSTRACT:In this paper, we propose an approximateMultiplier that is high speed yet energy efficient. The truncated multiplier, design is implemented by jointly considering the deletion, reduction, truncation, and final addition of PP bits. It is observed that the results of standard parallel multiplier and then compare this result with truncated multiplier which is approximately same. It is analysed that area required for implementation of truncated multiplier reduces to large extent as compare to standard parallel multiplier. The efficiency of the proposed multiplier is evaluated by comparing its performance with those of some approximate and accurate multipliers using different design parameters. Also there is reduction in power dissipation and propagation delay. In this system final truncated multiplier satisfies the precision requirement.

KEY WORDS: Accuracy, high speed, multiplier, truncated multiplier.

I.INTRODUCTION

The energy minimization is one of the main design requirements in almost any electronic systems, especially the portable ones such as smart phones, tablets, and different gadgets. It is highly desired to achieve this minimization with minimal performance (speed) penalty. Digital signal processing (DSP) blocks are key components of these portable devices for realizing various multimedia applications. The computational core of these blocks is the arithmetic logic unit where multiplications have the greatest share among allarithmetic operations performed in these DSP systems. Therefore, improving the speed and power/energy-efficiency characteristics of multipliers plays a key role in improving theEfficiency of processors.

Final outputs are either images or videos prepared for human consumptions. This fact enables us to use approximations for improving the speed/energy efficiency.
This originates from the limited perceptual abilities of human beings in observing an image or a video. In addition to the image and video processing applications, there are other areas where the exactness of the arithmetic operations is not critical to the functionality of the system. Being able to use the approximate computing provides the designer with the ability of making trade-offs between the accuracy and the speed as well as power/energy consumption.

Applying the approximation to the arithmetic units can be performed at different design abstraction levels including circuit, logic, and architecture levels, as well as algorithm and software layers. The approximation may be performed using different techniques such as allowing some timing violations (e.g., voltage overscaling or overclocking) and function approximation methods (e.g., modifying the Boolean function of a circuit) or a combination of them. In the category of function approximation methods, a number of approximating arithmetic building blocks, such as adders and multipliers, at different design levels have been suggested.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 15
May 2018

In this paper, we focus on proposing a high-speed low power/ energy yet approximate multiplier appropriate for error resilient DSP applications. The proposed approximate multiplier, which is also area efficient, is constructed by modifying the conventional multiplication approach at the algorithm level assuming rounded input values. We call this rounding-based approximate (RoBA) multiplier. The proposed multiplication approach is applicable to both signed and unsigned multiplications for which three optimized architectures are presented. The efficiencies of these structures are assessed by comparing the delays, power and energy consumptions, energy-delay products (EDPs), and areas with those of some approximate and accurate (exact) multipliers.

II. EXISTED SYSTEM

The main idea behind the proposed approximate multiplieris to make use of the ease of operation when the numberare two to the power n ($2n$). To elaborate on the operationof the approximate multiplier, first, let us denote the roundednumbers of the input of A and B by Ar and Br, respectively.The multiplication of A by B may be rewritten as

$$A\times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times A - Ar \times Br. \quad (1)$$

The key observation is that the multiplications of $Ar \times Br$,$Ar\times B$, and $Br\times A$ may be implemented just by the shift operation.The hardware implementation of $(Ar - A)\times(Br - B)$. However, is rather complex. The weight of this term inthe final result, which depends on differences of the exactnumbers from their rounded ones, is typically small. Hence,we propose to omit this part from (1), helping simplify themultiplication operation.

Thus, one can perform the multiplication operation using three shift and two addition/subtraction operations. In this approach, the nearest values for A and B in the form of $2n$ should be determined. When the value of A (or B) is equal to the $3 \times 2p-2$ (where p is an arbitrary positive integer larger than one), it has two nearest values in the form of $2n$ with equal absolute differences that are $2p$ and $2p-1$. While both values lead to the same effect on the accuracy of the proposed multiplier, selecting the larger one (except for the case of $p = 2$) leads to a smaller hardware implementation for determining the nearest rounded value, and hence, it is considered in this paper. It originates from the fact that thenumbers in the form of $3 \times 2p-2$ are considered as do notcare in both rounding up and down simplifying the process,and smaller logic expressions may be achieved if they are usedin the rounding up.

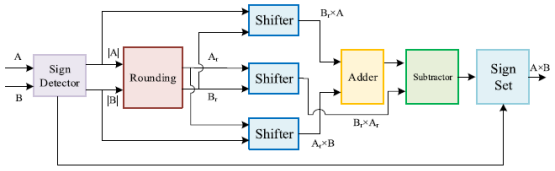

Fig. 1. Block diagram for the hardware implementation of the existed multiplier.

The only exception is for three, which in this case, two isconsidered as its nearest value in the proposed approximatemultiplier.It should be noted that contrary to the previous workwhere the approximate result is smaller than the exact result,the final result calculated by the RoBA multiplier may beeither larger or smaller than the exact result depending onthe magnitudes of Ar and Br compared with those of A and$B$, respectively.

Note that if one of the operands (say A) issmaller than its corresponding rounded value while the otheroperand (say B) is larger than its corresponding rounded value,then the approximate result will be larger than the exact result.This is due to the fact that, in this case, the multiplication resultof $(Ar - A) \times (Br - B)$ will be

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 15
May 2018

negative. Since the differencebetween (1) and (2) is precisely this product, the approximateresult becomes larger than the exact one. Similarly, if both *A*and *B* are larger or both are smaller than *Ar* and *Br*, then theapproximate result will be smaller than the exact result. From figure (1) we can observe the block diagram of existed system.

III. PROPOSED SYSTEM

Truncated Multiplier has the advantage of reducing powerconsumption in the DSP systems. It is most commonly used insystems where least significant part of partial product can beskipped or disabled which leads to low power consumption, area and timing. Here the partial product is split into twosections namely the Least Significant Part (LSP) and MostSignificant Part (MSP). The LSP is disabled or avoided to getthe truncated output. The product of a full-width Multiplier canbe described as Pfull = SMSP + SLSP, where SMSP represents thesum of the partial product bits belonging to the MSP and SLSPis the sum of the bits belonging to LSP. Generally, the outputof the fixed-width N x N truncated multiplier is represented asPfull-rounded = tN (SMSP + SLSP + LSB/2), where LSB represents theLeast Significant Bit and tN (x) represents the truncation of anoperand x by eliminating its lowest bits. Bits are discarded tomaintain bit-width of N-bits.

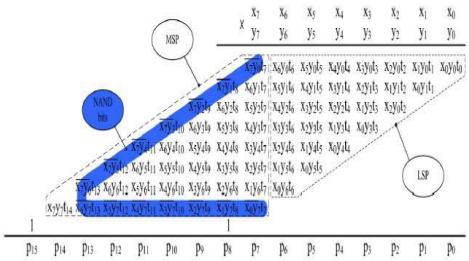

Fig. 2. 8 x 8 bit Variable Truncated Multiplier

Variable Truncated Multiplier effectively helps in adjusting the output width of the multiplier. This follows a column based strategy which flexibly truncates the partial product as per the requirement thus controlling the power and time constraints. Truncation may be different for different applications. This architecture is flexible and work differently for different applications. The applications may differ from each other as some may require a high precision output and some others may require low power, time or area. Thus Variable Truncated Multiplier can be employed as a general purpose multiplier.The concept of the Variable Truncated Multiplication for an 8x 8 bit multiplier is illustrated in Fig.2.

IV. RESULTS

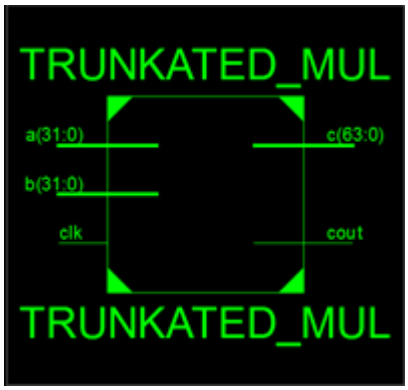

Fig. 3. RTL schematic

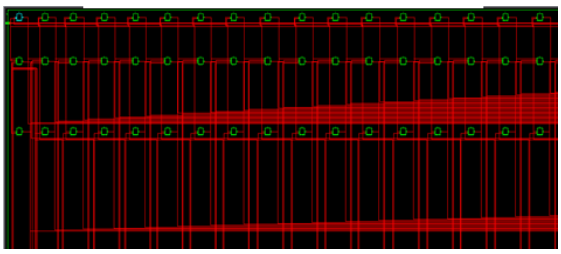

Fig. 4. Technology schematic

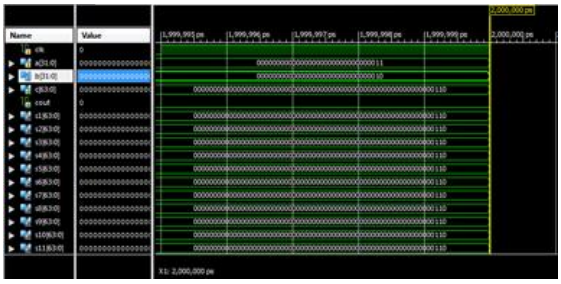

Fig. 5. Output

V. CONCLUSION

In this truncated multiplier, design is implemented by jointly considering the deletion, reduction, truncation, and final addition of PP bits. It is observed that the results of standard parallel multiplier and then compare this result with truncated multiplier which is approximately same. It is analysed that area required for implementation of truncated multiplier reduces to large extent as compare to standard parallel multiplier. Also there is reduction in power dissipation and propagation delay. In this system final truncated multiplier satisfies the precision requirement.

VI. REFERENCES

[1] Manuel de la Guia Solaz, Richard Conwayand WeiHan,"AFlexible Low Power DSP With a Programmable TruncatedMultiplier" IEEE transactions on circuits and systems—I :regular papers, vol. 59, no. 11, November 2012

[2] M. Schulte, J. Stine, and J. Jansen, "Reduced power dissipationthrough truncated multiplication," in Proc. IEEE AlessandroVolta Memorial Workshop Low-Power Design, 1999, pp. 61–69.

[3] W. J. Townsend, E. E. Swartzlander, Jr., and J. Abraham, "Acomparison of Dadda and Wallace multiplier delays," in Proc.SPIE Symp.Adv. Signal Process. Algorithms, Archit.,Implementations, San Diego, CA, 2003, vol. 5205.

[4] Ronak Bajaj, Saransh Chhabra, Sreehari Veeramachaneni andM B Srinivas,"A Novel, Low-Power Array MultiplierArchitecture", International Institute of InformationTechnology-Hyderabad and Birla Institute of Technology andSciences (BITS) Pilani, Hyderabad Campus

[5] P.C.Franklin, M.Ramya," Resource Efficient ReconfigurableProcessor for DSP Applications," International Journal ofInnovative Research in Science, Engineering andTechnology,Volume 3, Special Issue 3, March 2014.