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Design A High Speed Parallel Prefix Adder for Communication

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ABSTRACT: In this paper, a well-known regular and modular parallel prefix adder is analysed by using residue number system reverse converters. To achieve high speed reverse converters, VLSI is implemented. Because of this there is a reduction in delay and area, as well as high power consumption is obtained. To avoid the high power consumption obtained in the system, a hybrid parallel prefix adders is used. This produces better trade of between delay and power consumption. Anew approach is proposed to design an Efficient Ladner-Fischer Adder concentrates on gate levels to improve the speed and decreases the memory. It is like tree structure and cells in the Carry Generation Stage are decreased to speed up the binary addition. The Proposed Adder addition operation offers great advantage inreducing delay.This methodology helps the designer to adjust the performance of the reverse converter based on the target application and existingConstraints.

KEY WORDS: Digital arithmetic, parallel-prefix adder, residue number system (RNS), reverse converter.

I.INTRODUCTION

Addition operation is the main operation in digital signal processing and control systems. The fast and accuracy of a processor or system depends on the adder performance.In general purpose processors and DSP processors the addition operation addresses are taken from simple Ripple Carry Adder. It is used for the addition operation i.e., if N-Bits addition operation is performed by the N-Bit Full Adder. In Ripple Carry Adder each Bit Full Adder operation consists of sum and carry that carry will be given to next Bit Full Adder operation, that process is continuous till the N^{th} bit operation. The N-1^{th}Bit Full Adder operation carry will be given to the N^{th}Bit Full Adder operation present in the Ripple Carry Adder.

Adders are commonly found in the critical path of many building blocks of microprocessors and digital signal processing chips. Its purpose is to form the arithmetic sum of two binary numbers.The most important formeasuring the quality of adder designs in the past were propagation Delay, and area.Instead of waiting for the carry propagation of the first addition, the idea here is to overlap the carry propagation of the first addition with the computation in the second addition, and so forth, since repetitive additions will be performed by a multiplierand adder. In multiplication and division, multi operand addition is often encountered. More powerful adders are required which can add many numbers instead of two together. The design of a high-speed multioperand adder called Parallel Prefix Adders.

The Prefix outcome of the operation depends on the initial inputs. The Parallel involves the execution of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel. This operator is associative hence it can be implemented in a parallel fashion. Different topologies for the parallel generation of carries. Adders that use these topologies are called Parallel Prefix Adders.

Parallel algorithms for prefix sums can often be generalized to other scan operations on associative binary operations and they can also be computed efficiently on modern parallel hardware. Many parallel implementations

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follow a two pass procedure where partial prefix sums are calculated in the first pass on each processing unit; the prefix sum of these partial sums is then calculated and broadcast back to the processing units for a second pass using the now known prefix as the initial value. Asymptotically this method takes approximately two read operations and one write operation per item.

In this brief, for the first time, we present a comprehensive methodology to wisely employ parallel-prefix adders in carefully selected positions in order to design fast reverse converters. The collectedexperimental results based on area, delay, and power consumptionshow that, as expected, the usage of the parallel-prefix adders toimplement converters highly increases the speed at the expenseof additional area and remarkable increase of power consumption.The significant growing of power consumption makes the reverseconverter not competitive. Two power-efficient and low-area hybridparallel-prefix adders are presented in this brief to tackle with theseperformance limitations, leading to significant reduction of the

Parallel-prefix adders will have a different performance than VLSI implementations. In particular, most modern FPGAs employ a fast-carry chain which optimizes the carry path for the simple Ripple Carry Adder. The Ladner-Fischer is the Parallel Prefix Adders used to done the addition operation. It is look like tree structure to perform the high speed arithmetic operation. Ladner Fischer Adder is used for high performance addition operation.

II. EXISTED SYSTEM

The Chinese remainder theorem, or other related improved approaches and techniques underlie the RNS reverse conversion,whose formulation can be directly mapped to ripple-carry adders (RCA). However, this leads to significant speed degradation, due tothe linear increase of the delay in the RCA with the number of bits.Parallel-prefix adders can be used in the RNS reverse converters tobind the delay to logarithmic growth. However, in reverse converters, several parallel-prefix adders are usually required. Even when onlyone adder is used, the bit length of this adder is quite large.

A regular parallel-prefix adder with thedesirable prefix structure can be used to perform the first part of theaddition, for which the corresponding bits of the operands are fullyvariable, and a RCA with simplified logic to do the second part (fulladder becomes XNOR/OR gates because of the constant operand).

The main reason for the high power consumption and area overhead of these adders is the recursive effect of generating and propagating signals at each prefix level. An optimized approach is proposed which uses an extra prefix level to add theoutput carry. However, this method suffers from high fan-out, whichcan make it usable only for small width operands. However, wecould address this problem by eliminating the additional prefixlevel and using a modified excess-one unit instead. In contrastto the BEC, this modified unit is able to perform a conditionalincrement based on control signals as shown in Fig. 1.

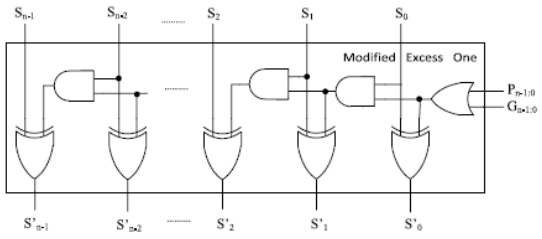

Fig. 1. Existed system

III. PROPOSED SYSTEM

The Proposed Ladner-Fischer Adder is flexible to speed up the binary

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addition and the structure looks like tree structure for the high performance of arithmetic operations. In Ripple Carry Adders each bit wait for the last bit operation. In Parallel Prefix Adders instead of waiting for the carry propagation of the first addition, the idea here is to overlap the carry propagation of the first addition with the computation in the second addition, and so forth, since repetitive additions will be performed by a multioperand adder.

Research on binary operation elements and motivation gives development of devices. Field programmable Gate arrays [FPGA's] are most popular in recent years because they improve the speed of microprocessor based applications like mobile DSP andtelecommunication. The construction of Efficient Ladner-Fischer Adder consists of three stages. They are Pre-Processing Stage, Carry Generation Stage, and Post-Processing Stage.

The first input bits goes under Pre-Processing Stage and it will produce propagate and generate. These propagates and generates undergoes Carry Generation Stage produces carry generates and carry propagates, these undergoes Post-Processing Stage and gives final sum. From below figure (2) we can observe the proposed system block diagram.

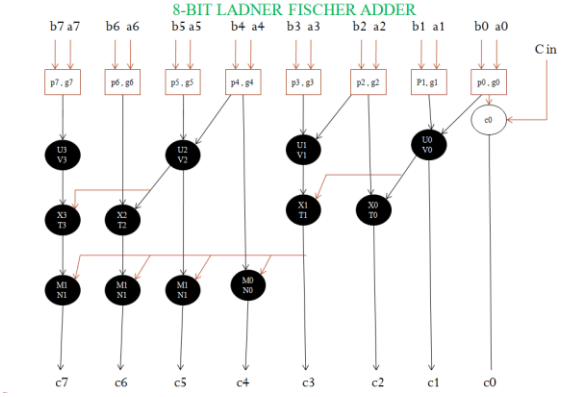

Fig. 2. Proposed system

The Efficient Ladner-Fischer Adder structure is looking like tree structure for the high performance of arithmetic operations and it is the fastest adder which focuses on gate level logic. It designs with less number of gates. So, it decreases the delay and memory used in this architecture.In Efficient Ladner-Fischer Adder, black cell operates three Gates and gray cell operates two Gates. The gray cell reduces the delay and memory because it operates only two Gates. The Proposed Adder is design with the both black and gray cells. By using gray cell operations at the last stage of Proposed Adder gives an enormous dropping delay and memory used.

IV. RESULTS

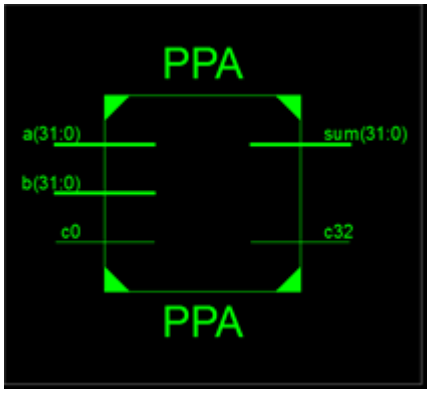

Fig. 3. RTL schematic

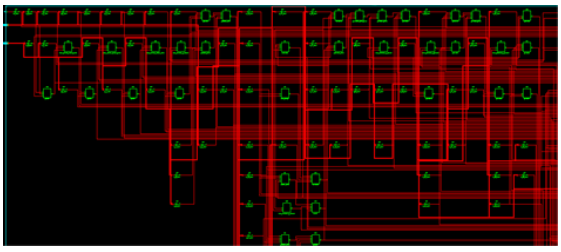

Fig. 4. Technology schematic

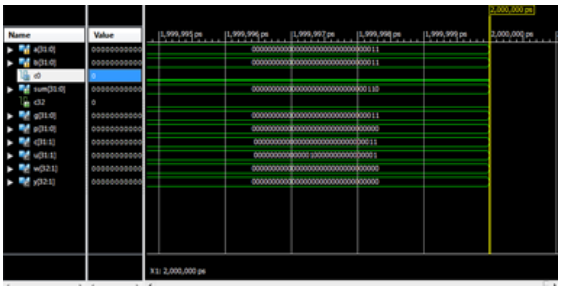

Fig. 5. Output

V. CONCLUSION

In this project, a new approach to design an Efficient Ladner-Fischer Adder concentrates on gate levels to improve the speed and decreases the memory. It is like tree structure and cells in the Carry Generation Stage are decreased to speed up the binary addition. The Proposed Adder addition operation offers great advantage in reducing delay. The future scope is to design 32 Bit Proposed Adder with less number of black cells to improve the area and delay performance of the adders.

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