

A Smooth Strategy For Design Of Low Power Sequential System Using Multi Bit Flip-Flop

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ABSTRACT:The major dynamic power consumers in computing and consumer electronics products is the system's clock signal, typically responsible for 30%–70% of the total dynamic power consumption. Clock gating is a predominant technique used for power saving. The Data driven clock gating is used for reduce power consumption in synchronous circuits. Common clock gating is used for power saving. However clock gating still leaves larger amount of redundant clock pulses. Multibit flip-flop is also used to reduce power consumption. Using of Multibit Flip-Flop method is to eliminate the total inverter number by sharing the inverters in the flip-flop. Combination of Multibit Flip-Flop with Data driven clock gating will increase the further power saving. Xilinx software tool and quattrus II for power analysis is used for implementing this proposed system.

KEYWORDS-Data Driven clock gating

I. INTRODUCTION

The data of digital systems are usually stored in flip-flops (FFs), each of which has its own internal clock driver. In an attempt to reduce the clock power, several FFs can be grouped into a module called a multibit FF (MBFF) that houses the clock drivers of all the underlying FFs. We denote the grouping of k FFs into an MBFF by a k -MBFF. Kapoor et al. [1] reported a 15% reduction of the total dynamic power in a 90-nm processor design. Electronic design automation tools, such as Cadence Liberate, support MBFF characterization.

The benefits of MBFFs do not come for free. By sharing common drivers, the clock slew rate is

degraded, thus causing a larger short-circuit current and a longer clock-to-Q propagation delay t_{pCQ} . To remedy this, the MBFF internal drivers can be strengthened at the cost of some extra power. It is therefore recommended to apply the MBFF at the RTL design level to avoid the timing closure hurdles caused by the introduction of the MBFF at the backend design stage. Due to the fact that the average data-to-clock toggling ratio of FFs is very small, which usually ranges from 0.01 to 0.1 [2], the clock power savings always outweigh the short-circuit power penalty of the data toggling.

An MBFF grouping should be driven by logical, structural, and FF activity considerations. While FFs grouping at the layout level have been studied thoroughly, the front-end implications of MBFF group size and how it affects clock gating (CG) has attracted little attention. This brief responds to two questions. The first is what the optimal bit multiplicity k of data-driven clock-gated (DDCG) MBFFs should be. The second is how to maximize the power savings based on data-to-clock toggling ratio (also termed activity and data toggling probability).

In existing system power reduction is achieved by using clock gating. With clock gating, the clock signals are multiply with an AND gate logic to explicitly predefined enabling signal. But this clock gating still leaves large number of redundant clock pulses. Although substantially increasing design productivity, such tools require the employment of a long chain of automatic synthesis algorithms, from register transfer level (RTL) down to gate level and net list. Unfortunately, such automation leads to a large number of unnecessary clock toggle, thus

increasing the number of wasted clock pulses at flipflops (FFs) as shown in this paper through several industrial examples. Consequently, development of automatic and effective methods to reduce this inefficiency is desirable. In the sequel, we will use the terms toggling, switching, and activity interchangeably

II. RELATED WORK

Several dynamic power control techniques are adopted in VLSI circuits out of which the most important one is clock gating. [5] uses multiple deliver voltages to reduce clock tree energy. The incoming, high voltage clock signal is down-scaled through a low-voltage buffer level. The low- V_{dd} signal is then propagated throughout the circuit, and regenerating factors (e.g., buffers) are inserted into the tree structure to make sure the appropriate pace and slew rate of the transitions. Finally, the original high-voltage is restored thru level shifters before the clock alerts feed the flip-flops.

In [3] Clock Distribution the use of Multiple Voltages reduces the rate of buffering and voltage converters this is crucial inside the electricity discount technique implemented the use of more than one supply voltages. The method supplied with the aid of Pangjung and Sapatnekar addresses this predicament with the aid of providing an extra sophisticated set of rules for introducing buffers into the clock tree and for putting the low-to-high voltage shifters, which are no longer necessarily positioned right in the front of the flip-flops. The set of rules considers the opportunity of buffer insertion after each step of backside-up subtree merging. In the diversion of keeping the skew very near zero, the set of rules guarantees that the range of regenerating factors is equalized along any root-to-sink paths of the tree. However, no matter the stable theoretical basis of this answer, experimental effects confirmed very small differences with the clock bushes generated through the approach the usage of multiple supply voltages. In [2] makes a specialty of Interconnect Power, i.e. Power dissipation due to the switching of interconnection capacitances, which can be a part of the full switched capacitance of every internet- C_j .

Applying wire capacitance discount techniques to a small percent of the wires can keep the majority of the interconnect energy.

Capacitance may be reduced by means of interconnect reduction and increasing interconnect spacing thereby decreasing capacitance and thereby reducing electricity dissipation.

In [4], a evaluate of some current strategies to be had for clock gating is provided. Also a brand new method that provides more immunity to the prevailing problems in available strategies is mentioned.

III. METHOD OF SOLUTION

Multi-bit Flip-Flop method is to eliminate the total inverter number by sharing the inverters in the flip-flops. Data driven clock gating reduce redundant clock pulses. Combination of Multi-bit Flip-Flop with Data driven clock gating will increase the further power saving. Xilinx software tool is used for implementing this proposed system. This paper studies data-driven clock gating, employed for FFs at the gate level, which is the most aggressive possible. The clock signal driving a FF is disabled (gated) when the FFs state is not subject to change in the next clock cycle [7]. Data-driven gating is causing area and power overheads that must be considered. In an attempt to reduce the overhead, it is proposed to group several FFs to be driven by the same clock signal, generated by bring the enabling signals of the individual FFs. This may however, lower the disabling effectiveness. It is therefore beneficial to group FFs whose switching activities are highly correlated and derive a joint enabling signal. In a recent paper, a model for data-driven gating is developed based on the toggling activity of the constituent FFs [9].

The optimal fan-out of a clock gate yielding maximal power savings is derived based on the average

toggle statistics of the individual FFs, process technology, and cell library in use. In general, the state transitions of FFs in digital systems depend on the data they process. Assessing the effectiveness of data-driven clock gating requires, therefore, extensive simulations and statistical analysis of the FFs' activity. Another grouping of FFs

for clock switching power reduction, called multi-bit FF (MBFF), has recently been proposed in [10] and [11]. MBFF attempts to physically merge FFs into a single cell such that the inverters driving the clock pulse into its master and slave latches are shared among all FFs in a group. MBFF grouping is mainly driven by the physical position proximity of individual FFs, while grouping for data-driven clock gating should combine toggling similarity with physical position considerations. While [9] answered

the question of what is the group size that maximizes power savings, this paper studies the questions of: 1) which FFs should be placed in a group to maximize the power reduction and 2) how to algorithmically derive those groups.

Data-Driven Clock Gating

Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling

signals at the gate level. In many cases, clock enabling signals are manually added for every FF as a

part of a design methodology. Still, when modules at a high and gate level are clocked, the state transitions

of their underlying FFs depend on the data being processed. It is important to note that the entire dynamic power consumed by a system stems from the periods where modules' clock signals are enabled. Therefore, regardless of how relatively small this period is, assessing the effectiveness of clock gating requires extensive simulations and statistical analysis of FFs toggling activity, as presented subsequently.

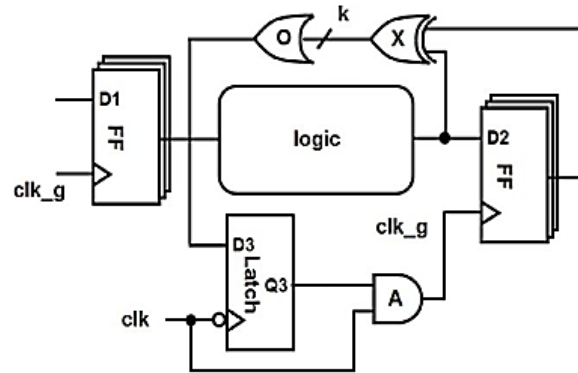


Fig. 1 Practical data-driven clock gating

Let the average toggling probability of a FF (also called activity factor) be denoted by p ($0 < p < 1$). Under the worst-case assumption of independent FF toggling, and assuming a uniform physical clock tree structure, it is shown in [9] that the number k of jointly gated FFs for which the power savings are maximized is the solution of

$$(1-p)k \ln(1-p) (c_{FF} + c_W) + c_{latch} / k^2 = 0 \dots \dots \dots (1)$$

Where c_{FF} is the FFs clock input capacitance, c_W is the unit-size wire capacitance, and c_{latch} is the latch capacitance including the wire capacitance of its clock input. Table I shows how the optimal k depends on p .

Such a gating scheme has considerable timing implications, which are discussed in [9]. We will return to those when discussing the implementation of data-driven gating as a part of a complete design flow.

Implementation and Integration In a Design Flow:

In the following, we describe the implementation of data-driven clock gating as a part of a standard backend design flow. It consists of the following steps.

- 1) Estimating the FFs toggling probabilities involves running an extensive test bench representing typical operation modes of the system to determine the size k of a gated FF group by solving (1).

2) Running the placement tool in hand to get preliminary preferred locations of FFs in the layout.

3) Employing a FFs grouping tool to implement the model and algorithms presented, using the toggling correlation data obtained in Step 1 and FF locations' data obtained in Step 2. The outcome of this step is k-size FF sets (with manual overrides if required), where the FFs in each set will be jointly clocked by a common gater.

4) Introducing the data-driven clock gating logic into the hardware description (we use VerilogHDL). This is done automatically by a software tool, adding appropriate Verilog code to implement the logic described in Fig. 2. The FFs are connected according to the grouping obtained in Step 3. A delicate practical question is whether to introduce the gating logic into RTL or gate-level description. This depends on design methodology in use and its discussion is beyond the scope of this paper. We have introduced the gating logic into the RTL description.

5) Re-running the test bench of Step 1 to verify the full identity of FFs' outputs before and after the introduction of gating logic. Although data driven gating, by its very definition, should not change the logic of signals, and hence FFs toggling should stay identical, a robust design flow must implement this step.

6) Ordinary backend flow completion. From this point, the backend design flow proceeds by applying ordinary place and route tools. This is followed by running clock-tree synthesis.

IV. SIMULATION RESULTS

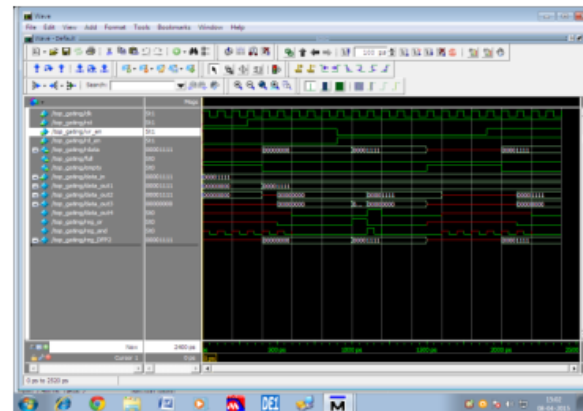


Fig. 2 Output Waveform of Clock Gated Synchronous FIFO

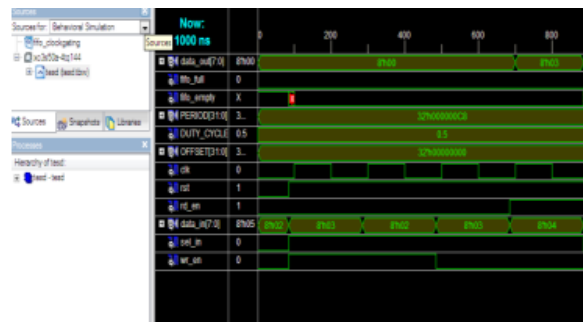


Fig. 3 Output Waveform of Synchronous FIFO Using Multibit Flipflop With Data Driven Clock Gating.

V. CONCLUSION

Common clock gating is used for power saving. But clock gating still leaves larger amount of redundant clock pulses. Multibit flip-flops are also used to decrease power consumption. Using of Multibit Flip-Flop method is to remove the total inverter number by sharing the inverters in the flipflops. Combination of Multibit Flip-Flop with Data driven clock gating will increase the additional power saving. Xilinx software tool is used for implementing this proposed system. The combination of data-driven gating with MBFF in an attempt to yield additional power savings.

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