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FPGA Implementation on Advance Traffic Light Control System

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ABSTRACT: The traffic in road crossings /junctions is controlled by switching ON/OFF Red, Green & Amber lights in a particular sequence. The Traffic Light Controller is designed to generate a sequence of digital data called switching sequences that can be used to control the traffic lights of a typical four roads junction in a fixed sequence. It is also proposed to implement the day mode and night mode operations. It plays more and more important role in modern management and control of urban traffic to reduce the accident and traffic jam in road. It is a sequential machine to be analyzed and programmed through a multistep process. The device that involves an analysis of existing sequential machines in traffic lights controllers, timing and synchronization and introduction of operation and flashing light synthesis sequence. The methods that are used in this project are design the circuit, write a coding, simulation, synthesis and implement in hardware. In this project, XILINX Software was chosen to design a schematic using schematic edit, writes a coding using Verilog HDL (Hardware Description Language) text editor and implements the circuit on Programmable Logic Device [PLD].

Keywords: FPGAs,CPLD,TLC

1.INTRODUCTION:

Traffic congestion is a severe problem in many modern cities around the world. Traffic congestion has been causing many critical problems and challenges in the major and most populated cities. To travel to different places within the city is becoming more difficult for the travelers in traffic. Due to these congestion problems, people lose time, miss opportunities, and get frustrated. Traffic congestion directly impacts the companies. Due to traffic congestions there is a loss in productivity from workers, trade opportunities are lost, delivery gets delayed, and thereby the costs goes on increasing. To solve these congestion problems, we have to build new facilities & infrastructure but at the same time make it smart. The only disadvantage of making new roads on facilities is that it makes the surroundings more congested. So for that reason we need to change the system rather than making new infrastructure twice.

Therefore many countries are working to manage their existing transportation systems to improve mobility, safety and traffic flows in order to reduce the demand of vehicle use. Therefore, many researches about traffic light system have been done in order to overcome some complicated traffic phenomenon but existent research had been limited about present traffic system in well-travelled traffic scenarios. The time of allocation is fixed from east to west or opposite way and from north to south way in crossroads. Field Programmable Gate Arrays (FPGAs) are extensively used in rapid prototyping and verification of a conceptual design and also used in electronic systems when the maskproduction of a custom IC becomes prohibitively

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expensive due to the small quantity. Many system designs that used to be built in custom silicon VLSI are now implemented in Field Programmable Gate Arrays. This is because of the high cost of building a mask production of a custom VLSI especially for small quantity.

2. LITERATURE SURVEY

In many cities Traffic Light Controller (TLC) is based on microcontroller and microprocessor. These TLC systems with microcontroller and microprocessor have limitations because it uses the pre-defined hardware, which is works as given program that does not have the flexibility of modification on real time basis. This program is fixed which is not reprogrammable or erasable by designer .Due to the fixed time intervals of green, orange and red signals the waiting time is more.

If waiting time of vehicles is more than fuel loss also occurred. So we have to implement some advanced system for traffic control due to this user can save their time. implementation of traffic Light Controller can be through Application Specific Integrated Circuit. ASIC design is more expensive than FPGA. Most of the TLCs implemented on FPGA are simple ones that have been implemented as examples of FSM. Traffic Light Control System can be implemented with Programmable Logic Device (PLD) and Complex Programmable Logic Device (CPLD). PLD like PALs and GALs are available only in small sizes, equivalent to a hundred of logic gates. So traffic light control system is not controlled by PLDs which is having more crowds of vehicles on road. Complex Programmable Logic Device (CPLD) is also used for TLC system. CPLD having large number of logic gates Now, CPLD can replace thousands, or even hundreds of thousands, of logic gates.

But CPLDs doesn"t have much memory. Due to lack of memory devices require lots of flip flops which complicate the design of system. When comparison of response time for various frequencies, for both is observed CPLD was performing twice as better than PLD. PLD based circuit shows a delayed response. The response with respect to clock, found that delay response of PLD is twice as much than the delay response of CPLD at a nano second level. Traffic system which requires fast response, CPLD may be the best choice. But further More to implement more complex circuits and tested the capability; the CPLD is not useful because not having very large number of gates capacity. CPLDs having thousand to ten thousand of logic gates available. FPGA is the perfect replacement for CPLD. CPLD and FPGA is having somewhat same features but FPGA is having more logic gates availability. FPGAs typically range from tens of thousands to several million which is more than CPLD.

FPGA which offers many advantages over microcontrollers such as fast speed, number of input/output ports, and performance which are all very important in TLC design. FPGAs are famous for their low-cost, high-volume applications and are very good as replacements for fixed-logic gate arrays. The FPGA is not only available for a very low cost, but it integrates many architectural features associated with high-end programmable logic. Due to these advantageous features like low cost and integrated features has made FPGA an ideal. By using Application Specific Integrated Circuits (ASIC) traffic light system become very expensive

3.PROPOSED METHOD

3.1 Design of Traffic Light Controller

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Traffic Light Controller can be designed by starting with some arbitrary assumptions. At first the North traffic will be allowed to move and then traffic in the East, South and West direction will be allowed to move in sequence. The advantage of writing Traffic Light Controller program is that in a program, modifications as per requirements can be done easily i.e., suppose the traffic on main road should be allowed for more time and for side roads the traffic should be allowed for less time: then the clock is divided in such a way that for main road the clock period will be more and for side roads the clock period will be less, this is because the main road traffic is heavy when compared to the side road traffic. In general TLC System will be having three lights (red, green and yellow) in each direction where red light stands for traffic to be stopped, green light stands for traffic to be allowed and yellow light stands for traffic is going to be stopped in few seconds.

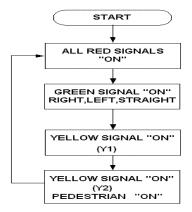


Fig 3.1 Flow Chart

3.2 Explanation of Traffic Light Controller

In this structure, there are four traffic signals, represented by R1, R2, R3 and R4 to be controlled. All the four signals have same priority as they all are main roads.

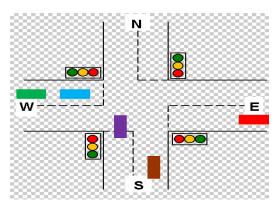


Fig 3.2 Traffic Signals at Junction

First of all the signal controller is in the reset mode where in the signal of road (R1) is green whereas all the other roads R2, R3 and R4 are red. This state we have assigned as S0.

Later the controller sends the control to state S1 where the R1 is yellow whereas all the other signals are still red only. In this state the controller checks whether the sensor at road R2 which is X2 is low or not. If the sensor gives a low signalling that there is no traffic on that road, then that signal on road R2 is skipped transferring control to the state S4 where signal on road R3 is turned whereas rest of the signals are showing red. On the hand if the traffic is present on the road R2 then the control is sent to state S2 which switches on the signal on road R2 to green and rest of the signals are red only when the control is with state S2 after showing the green signal the signal light changes from green to yellow for signal on the road R2 while all the other signals continue to be in red light mode only which is the operation of state S3.

Again when the controller is in state S3 it checks for the response of sensor X3 on road R3. If the output of sensor is low the control of the system will be transferred to state S6 skipping the working of the signal on road R3 otherwise the control is given to corresponding next state S4.



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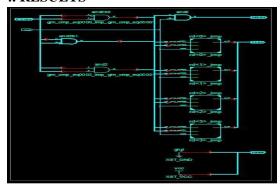
When in S4 the traffic signal of road R3 turns green on the other hand the signals of roads R1, R2 and R4 remain red itself. The control is then transferred to state S5.

When the control is with state S5 it checks for the output of the sensor X4 on the road R4. Depending on the output of X4 the further state change takes place accordingly. If low then the control is transferred to state S0 skipping the operation of the signal on road R4 otherwise the control is with the S6. When the controller is in state S5 there is change of signal on road R3 from green to yellow.

When the control is with state S6 the signal of road R4 turns green whereas all the signal turn or remain in red signal only. Thee control is then shifted to state S0.

In state S7 the signal of road R4 turns from green to yellow. Simultaneously the sensor on the first road R1 which is X1 is checked for its output. If the signal is low then the control is shifted directly to state S2 otherwise the control is shifted to default state S0. These states are not mandatory. The number of states, the order of the lights and the delay.

4. RESULTS



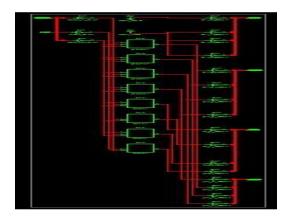


Fig 4.2 Technology Schematic

The below figure shows the Wave form of the Traffic Light Controller when the test bench is applied to the source code.

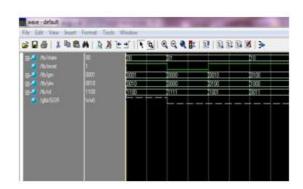


Fig 4.3 Wave Form

5. CONCLUSION

The modern ways of multi-way traffic management improves the traffic condition up to a large extent. Advanced signaling controllers contribute to the improvement of the urban traffic; which is proportional to the complexity of the controller. These more complex controllers can be well handled using states machines. Methods to reduce the states in the state machine also help in reducing the required hardware thus leading to low power and area efficient design. The future scope of this project

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is it can be directly applied in real time by employing more number of such circuits.

REFERENCES

- [1] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing:Principles, Algorithms and Applications*. Upper Saddle River, NJ, USA:Prentice-Hall, 1996.
- [2] T. Hentschel and G. Fettweis, "Software radio receivers," in *CDMA Techniques for Third Generation Mobile Systems*. Dordrecht, The Netherlands: Kluwer, 1999, pp. 257–283.
- [3] E. Mirchandani, R. L. Zinser, Jr., and J. B. Evans, "A new adaptive noise cancellation scheme in the presence of crosstalk [speech signals]," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 39, no. 10, pp. 681–694, Oct. 1995.
- [4] D. Xu and J. Chiu, "Design of a high-order FIR digital filtering and variable gain ranging seismic data acquisition system," in *Proc. IEEE Southeastcon*, Apr. 1993, p. 1–6.
- [5] J. Mitola, Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering. New York, NY, USA: Wiley, 2000.
- [6] A. P. Vinod and E. M. Lai, "Low power and high-speed implementation of FIR filters for software defined radio receivers," *IEEE Trans. Wireless Commun.*, vol. 7, no. 5, pp. 1669–1675, Jul. 2006.
- [7] J. Park, W. Jeong, H. Mahmoodi-Meimand, Y. Wang, H. Choo, and K. Roy, "Computation sharing programmable FIR filter for low-power and high-performance applications," *IEEE J. Solid State Circuits*, vol. 39, no. 2, pp. 348–357, Feb. 2004.

- [8] K.-H. Chen and T.-D. Chiueh, "A low-power digit-based reconfigurable FIR filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 617–621, Aug. 2006.
- [9] R. Mahesh and A. P. Vinod, "New reconfigurable architectures for implementing FIR filters with low complexity," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 2, pp. 275–288, Feb. 2010.
- [10] S. Y. Park and P. K. Meher, "Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter," *IEEE Trans. CircuitsSyst. II, Exp. Briefs*, vol. 61, no. 7, pp. 511–515, Jul. 2014.