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Design of Disorder and Fault Tolerant Non-volatile Spintronic Turn Flops

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ABSTRACT: With technology down scaling, static power has become one of the biggest challenges in a system on chip. Normally off computing using non-volatile (NV) sequential elements is a promising solution to address this challenge. Generally, various NV shadow flip-flop architectures have been introduced in which magnetic tunnel junction (MTJ) cells are employed as backup storing elements. Due to the emerging fabrication processes of magnetic layers, MTJs are more susceptible for manufacturing defects than their CMOS counterparts. Additionally, unlike memory arrays that can effectively be repaired with well-established memory repair and coding schemes, flip-flops scattered in the layout are more difficult to repair. Hence, without effective defect and fault tolerance for NV flip-flops, the manufacturing yield will be affected severely. In this paper, we propose a fault-tolerant NV latch (FTNV-L) design; in which various MTJ cells are arranged in such a way that it is resilient to various MTJ faults. The simulation results show that our proposed FTNV-L can effectively tolerate all single MTJ faults with a considerably lower overhead than traditional approaches.

Key Words: Fault tolerant, flip-flop, magnetic tunnel junction (MTJ) open defect, MTJ short defect, non-volatile (NV) memory faults, process variation, spin-transfer torque (STT), spintronics, stuck at AP, stuck at P, temperature, triple modular redundancy (3MR), tunnel magnetoresistance (TMR).

I. INTRODUCTION

With the advancements in technology scaling, the excessive leakage power of CMOS devices becomes a major design issue. Therefore, nonvolatile (NV) magnetic memories using spintronic

technologies such as spin-transfer torque (STT) and spin orbit torque are gaining popularity. This is due to their various advantageous features such as high endurance, scalability, high density, low access latency, soft error immunity and CMOS compatibility. In these technologies, magnetic tunnel junction (MTJ) cells are used as storing devices, which store the logic value as resistance states. These storing devices can also be employed for flip-flop designs in a low-power system on chip (SoC). Therefore, many NV shadow flip-flop architectures have recently been introduced that exploit the normally off and instant-on attributes of MTJs. However, a single MTJ failure in such designs can lead to a complete breakdown of the normally off capabilities.

The fabrication of the magnetic layers to implement MTJ cells is more complex than that of conventional CMOS, since it is a new process based on new materials. Therefore, it is expected that magnetic layers are more prone to manufacturing defects than CMOS layers. For instance, there is a possibility of a barrier short during the ion beam etching process. As a consequence, the affected MTJs have a very low resistance value. On the contrary, MTJ cells exhibit an extremely high resistance for an open defect. In addition,

the magnetic orientation of the MTJ cells can be fixed to a specific magnetization configuration, meaning that their magnetic orientation and thus their resistances cannot be changed. This may happen permanently because of manufacturing defects in the magnetic layers or due to loss of margin in the CMOS support circuitry, such as reduced switching current or duration. All these defects can severely hurt the manufacturing yield of these emerging technologies and prevent their widespread adoption.

In order to render manufacturing defects, memories are usually equipped with redundancies and error detection/correction mechanisms. However, these techniques are inapplicable to flip-flop designs, because flip-flops are scattered widely in the SoC layout as individual cells. Nevertheless, in flip-flop designs, these faults can be addressed using traditional triple modular redundancy (3MR),1 in which the shadow latch component is triplicated, and the final output is generated based on a voting mechanism. In fact, it incurs huge area, energy, and latency costs. Therefore, it is a decisive need to have a cost-effective solution to deal with MTJ faults for overall yield and energy efficiency.

In this paper, we propose a novel shadow flip-flop architecture, in which we design a generic fault-tolerant NV latch (FTNV-L) to address the aforementioned faults in MTJ cells. In our proposed FTNV-L design, several MTJ cells are structured in such a way that it can easily tolerate all single MTJ faults within a flip-flop.

A preliminary version of this work was published in which the basic implementation of FTNV-L was discussed. In this paper, we extend our work with a detailed process variation analysis for our proposed FTNV-L design. Moreover, we demonstrate implications on MTJ resistance differences (also known as TMR) and read latency for our proposed design for various operating temperatures. In addition, we also present an algorithm to determine the minimum required TMR and resistance values for the MTJ cells to guarantee a fault-free functionality in the presence of various MTJ defects.

The simulation results demonstrate that our proposed FTNV-L design delivers the required resistance differences in the presence of any single fault to guarantee a fault-free functionality. Moreover, it has almost the same performance and energy for both backup and restores processes as a standard NV flip-flop. In addition, adding MTJ cells has a minimal impact on the overall flip-flop area, as they are fabricated in different layers.

II. EXISTED SYSTEM

A shadow flip-flop architecture using MTJ-based NV storing devices is very effective for leakage power reduction. This is due to the fact that by adopting these designs, the entire logic core can be power gated, unlike for conventional CMOS-based flip-flops. The block diagram of a typical shadow flip-flop architecture is shown in Fig. 2.

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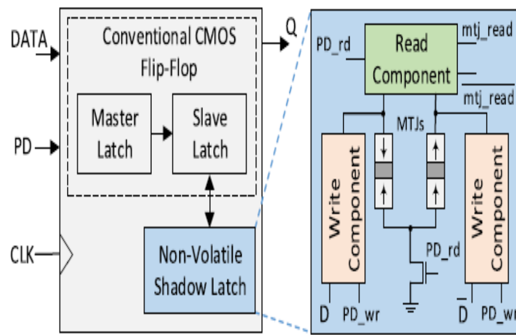

FIG. 1. OVERVIEW OF SHADOW NV FLIP-FLOP ARCHITECTURE

It consists of three components, namely, master latch, slave latch, and NV shadow latch. Here, the master and slave latches are the same as in conventional CMOS flip-flop design, and the NV shadow latch consists of two MTJs as well as read and write components. During power down, the data are stored in the shadow latch before going into the sleep mode, and they are read and restored into the slave latch during wakeup.

This operation is stimulated when the "PD" pin is activated and once when the data are stored in the NV latch, the power supply is disconnected. On the other hand, during wakeup, the NV shadow latch content is read and restored into the slave latch, so that the normal operation can be resumed. The "PD_rd" and "PD_wr" signals, which are generated using the "PD" pin, are employed to activate the read and store operations, respectively. The two MTJs should always store the opposite magnetization, which assists the read process by sensing the resistance differences. If any one of the MTJs is faulty, the entire shadow latch component cannot be used in the given architecture. Hence, our proposed shadow latch component is designed in such a way that it is capable of delivering the correct output in the presence of a single faulty MTJ within each flip-flop.

III. PROPOSED SYSTEM

An MTJ cell stores data as a resistance state. When the magnetic orientation of the two ferromagnetic layers is parallel to each other ("P" configuration), it exhibits a low resistance value. Otherwise, it has a high resistance value, when the magnetic orientations of those two layers are anti-parallel to each other ("AP" configuration). The MTJ cell works on two principles: 1) STT effect to store a value in the MTJ cell and 2) TMR effect to read out a value from the MTJ cell.

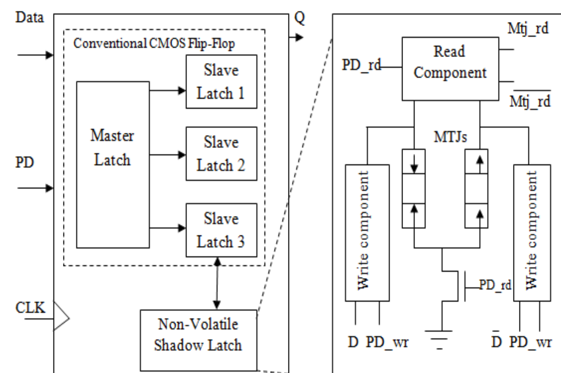

FIG 2. PROPOSED SYSTEM

The STT effect, which is responsible for the magnetic switching in FL, is accomplished by passing a current through the MTJ cell. Here, the magnetic switching happens when the applied current value is more than the critical current (Ic). For instance, if the current flows from the FL to RL for a sufficient duration, the magnetization of the MTJ cell switches to the "P" state. On the other hand, the magnetization of the MTJ cell switches to

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the "AP" state, if the current flows from the RL to FL for a sufficient duration.

A shadow flip-flop architecture using MTJ-based NV storing devices is very effective for leakage power reduction. The block diagram of a proposed system is shown in Fig. 2. It consists of three components, namely, master latch, slave latches, and NV shadow latch. Here, the master and slave latches are the same as in conventional CMOS flip-flop design, and the NV shadow latch consists of two MTJs as well as read and write components. During power down, the data are stored in the shadow latch before going into the sleep mode, and they are read and restored into the slave latch during wakeup. This operation is stimulated when the "PD" pin is activated and once when the data are stored in the NV latch, the power supply is disconnected. On the other hand, during wakeup, the NV shadow latch content is read and restored into the slave latch, so that the normal operation can be resumed. The "PD_rd" and "PD_wr" signals, which are generated using the "PD" pin, are employed to activate the read and store operations, respectively. The two MTJs should always store the opposite magnetization, which assists the read process by sensing the resistance differences. If any one of the MTJs is faulty, the entire shadow latch component cannot be used in the given architecture.

IV. RESULTS

FIG 3. RTL SCHEMATIC

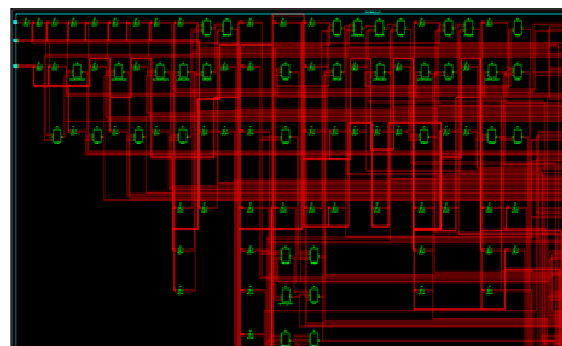

FIG 4. TECHNOLOGY SCHEMATIC

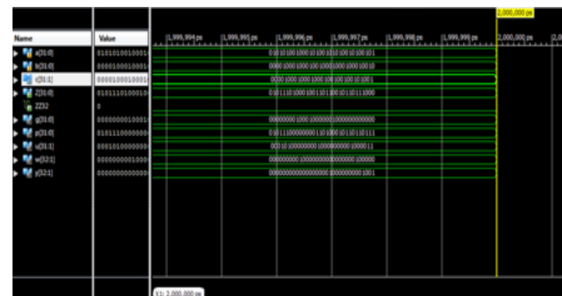

FIG 5. OUTPUT

PROPOSED_DL_FF Project Status			
Project File:	RAMACHANDRA_ENGG.xise	Parser Errors:	No Errors
Module Name:	PROPOSED_DL_FF	Implementation State:	Synthesized
Target Device:	xc3s100e-5vq100	•Errors:	No Errors
Product Version:	ISE 14.7	•Warnings:	2 Warnings (2 new)
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	52	960	5%
Number of 4 input LUTs	93	1920	4%
Number of bonded IOBs	98	66	148%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat 16. Jun 11:36:44 2018	0	2 Warnings (2 new)	0
Translation Report					
Map Report					
Place and Route Report					

FIG 6. REPORT

V. CONCLUSION

Nowadays, spintronic-based shadow latches are gaining attention as these are highly beneficial for leakage reduction. This is because the storing devices of these latches, which are MTJ cells, have attractive attributes such as zero leakage and high access speed. Consequently, these latches very effective for instant-on/normally off computing in an SoC. However, these MTJ cells are highly susceptible to several manufacturing defects such as short oxide, open vias, and magnetic orientation of the FL does not switch. Due to this, the yield of the design is affected since a single defect in a flip-flop can lead to the failure of the entire backup strategy. Therefore, we proposed an FTNV-L, in which MTJs are serially and parallelly connected in a unique way to tolerate MTJ related faults. We have demonstrated the functionality of our proposed design in the presence of all MTJ faults under the influence of process variation and operating temperature. In addition, using the FTNV-L design, any single fault per latch can be tolerated at much reduced costs compared with the traditional solution.

VI. REFERENCES

[1] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, "Scaling, power, and the future of CMOS," in *IEDM Tech. Dig. Papers*, Dec. 2005, pp. 7–15.

[2] N. S. Kim *et al.*, "Leakage current: Moore's law meets static power," *Computer*, vol. 36, no. 12, pp. 68–75, Dec. 2003.

[3] (2013). *International Technology Roadmap for Semiconductors*. [Online]. Available: http://www.itrs.net

[4] F. Oboril, R. Bishnoi, M. Ebrahimi, and M. B. Tahoori, "Evaluation of hybrid memory technologies using SOT-MRAM for on-chip cache hierarchy," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 34, no. 3, pp. 367–380, Mar. 2015.

[5] M.-T. Chang, P. Rosenfeld, S.-L. Lu, and B. Jacob, "Technology comparison for large last-level caches (L3Cs): Low leakage SRAM, low write-energy STT-RAM, and refresh-optimized eDRAM," in *Proc. HPCA*, Feb. 2013, pp. 143–154.

[6] J. M. Slaughter *et al.*, "High density ST-MRAM technology (Invited)," in *IEDM Tech. Dig. Papers*, Dec. 2012, pp. 29.3.1–29.3.4.

[7] M. Gajek *et al.*, "Spin torque switching of 20 nm magnetic tunnel junctions with perpendicular anisotropy," *Appl. Phys. Lett.*, vol. 100, no. 13, p. 132408, 2012.

[8] R. Bishnoi, M. Ebrahimi, F. Oboril, and M. B. Tahoori, "Improving write performance for STT-MRAM," *IEEE Trans. Magn.*, vol. 52, no. 8, Aug. 2016, Art. no. 3401611.

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