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A Novel Approach For Low-Power Sequential Circuits Using Reconfigurable Pulsed Latches

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Abstract: Pulsed latches are gaining increased visibility in low-power ASIC designs. They provide an alternative sequential element with high performance and low area and power consumption, taking advantage of both latch and flip-flop features. While the circuit reliability and robustness against different process, voltage, and temperature variations are considered as critical issues with current technologies, no significant reliability study was proposed for pulsed latch circuits. In this paper, we present a study on the effect of different PVT variations on the behavior of pulsed latches, considering the effect on both the pulsed and the latch. In addition, two novel design approaches are presented to enhance the reliability of pulsed latch circuits, while keeping their main advantages of high performance, low power, and small area. The two proposed designs have negligible power overhead when running at nominal supply voltage, and they have higher yield per unit power when compared with the traditional design at different voltages and temperatures. The advanced pulsed latches can implement up to 256-bit length for advanced pulsed latches.

Index Terms—Pulsed latches, flip-flops, pulsed flip-flops, variability,process variation, voltage scaling, low power

I. INTRODUCTION

Flip-Flops are viewed as the most prominent consecutive components utilized as a part of customary ASIC plans. This is principally a direct result of the effortlessness of their planning model, which makes the outline and timing confirmation forms substantially less demanding. Ace Slave Flip-Flops (MSFFs) are viewed as the most well-known and conventional usage of flip-flops, because of its steady activity and its straightforward planning qualities. Be that as it may, the way that the MSFF smaller scale engineering is typically constructed utilizing two back to back locks, it takes a considerable part of the clock time frame, control utilization, and region. A run of the mill MSFF has a huge ostensible planning overhead (whole of the clock-to-Q postpone and the setup time) of 6 FO4 (fanout-of-4) and can achieve 10 FO4 while considering

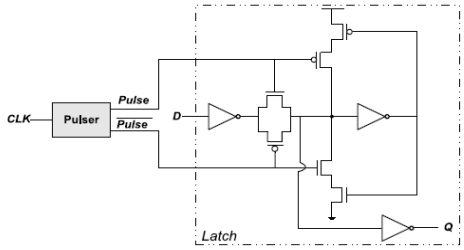

Fig. 1. Simple diagram of a traditional transmission gate pulsed latch.

clock skew and jitter [1]. What's more, the clock organizes, including the failures, frequently expends 33% to one portion of the aggregate unique energy of the chip [2], [3]. Notwithstanding the said overheads related with MSFF, some extra edges, which can

reach up to 15% (contingent upon the close down approach), are generally added to the ostensible planning edges to guarantee remedy activity under various process, voltage, and temperature (PVT) varieties [4]. This, thusly, builds the officially existing high planning and power overheads. For the above reasons, MSFF can be considered as a decent decision for low-to-medium execution outlines as they give a decent harmony between deferral, control, and simple plan and check forms for chips working at a generally low recurrence [5]. Then again, elite hand crafts tend to utilize hooks because of their lower timing overhead that can achieve 2 FO4 in a few outlines [1]. In spite of the fact that hook based outlines are normally powerful to clock skew and jitter (because of the lock straightforwardness period), hooks have a confused planning model, which, thus, convolutes the outline and the confirmation procedures and expands the danger of hold time infringement, particularly with PVT varieties. To fill in the missing hole amongst MSFFs and hooks, beat locks (here and there called beat flip-flops) have been utilized as a part of some elite plans [6]– [8].Beat hooks (PLs) are locks driven by short heartbeats created from the ordinary clock flag utilizing a heartbeat generator circuit called a pulser as appeared in Fig. 1. The pulser can be either inserted in the lock, or can be isolated as an independent circuit as appeared in Fig. 1. In the event that the last approach is utilized, a solitary pulser can be shared by in excess of one hook. In this manner, it has the benefit of territory and power utilization investment funds over the previous approach, and it is the focal point of our talk in this paper. Moreover, the pulser utilization can kill the requirement for a portion of the check cradles utilized as a part of the clock tree, along these lines giving an extra measure of energy and region funds. Having just a single hook between the info and the yield, PLs have bring down planning overhead than MSFFs. In the meantime, since the driving heartbeat is short, the straightforwardness time frame for the lock turns out to be extremely thin, permitting the PLs to have a planning conduct near that of MSFFs, to the degree that they are some of the time arranged among flip-tumble families [9], [10]. Additionally, because of the nearness of the restricted straightforward window of the lock, beat hooks have a natural resistance to clock skew and jitter [2]. Since they have less transistors that are activated by the clock flag, they have the benefit of diminishing a lot of timing power [8], and they devour significantly less spillage control contrasted with MSFFs because of the littler territory and less transistors. One difficulty in PL configuration is the decision of the pulsar yield beat width. Too shy of a heartbeat width may not be sufficient for the hooks to store the info information accurately, while too long of a heartbeat width will bring about a more drawn out lock straightforwardness window; which, thus, increment the planning overhead or can disregard hold time prerequisites [11]. This issue turns out to be more confounded while thinking about various wellsprings of varieties. PVT varieties impact sly affect diverse circuit parts. Since consecutive components, by and large, are by nature time delicate components, they are among the circuit classifications that are exceedingly influenced by any PVT varieties [12]. Since beat locks, specifically, are extremely time touchy, great investigation of the impact of various wellsprings of varieties must be considered. Since a portion of these varieties, for example, voltage and temperature, are worldly varieties that change over the working time of chips, cautious examination and

configuration must be performed to guarantee that solid circuit task can simply be accomplished with no huge misfortune in execution, influence and zone. The investigation exhibited in this paper demonstrates that some variety impacts on PLs can be remunerated with cautious examination amid the plan procedure, while some others can not be repaid without critical debasement in unwavering quality or execution. For instance, beat locks intended to work at certain voltage corner may not work at another voltage corner without debasement in either execution or unwavering quality. Since consecutive components, for example, beat hook are productively utilized inside the bite the dust, any debasement in their execution or dependability can altogether influence the execution of the whole chip or can even reason an expansive yield misfortune. Furthermore, since planning a chip that can consummately work at only one voltage corner isn't a worthy arrangement these days, adding a reconfiguration capacity to PL can achieve the required target outline objectives. With this additional element, PLs can be designed to keep running with the base planning overhead to ensure remedy task at various voltage levels within the sight of various wellsprings of variety. In this paper, we are exhibiting fluctuation investigation of one of the prevalent topologies of beat hooks, Transmission Gate Pulsed Latch (TGPL), examining the impacts of process, voltage, and temperature varieties, and in addition proposing plan adjustments that can help in diminishing the likelihood of circuit disappointment (i.e. upgrading beat lock dependability) at various supply voltage esteems. With the proposed approaches, beat locks show a considerable other option to MSFFs, giving higher execution, bring down region and power utilization, and higher dependability and strength to various types of varieties.

The primary commitment regions of this paper are:

• An investigation of the impact of PVT minor departure from the task of beat locks in cutting edge innovation hubs, considering the consequences for both the pulser and the hooks.

• Two novel heartbeat generator outlines for the beat lock that can be used to expand the dependability of beat hook circuits, while keeping its principle favorable circumstances of superior and low power utilization.

• Comprehensive examinations of unwavering quality, power, and territory between various information registers executed utilizing the customary transmission door beat hooks and the proposed reconfigurable beat locks.

II. PROPOSED MODEL:

Ashift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.

The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

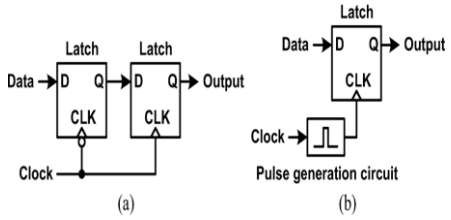

Fig. 2. (a) Master-slave flip-flop. (b) Pulsed latch.

Shift Register working model:

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. The shift register in Fig. consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. show the timing problem in the shifter register.

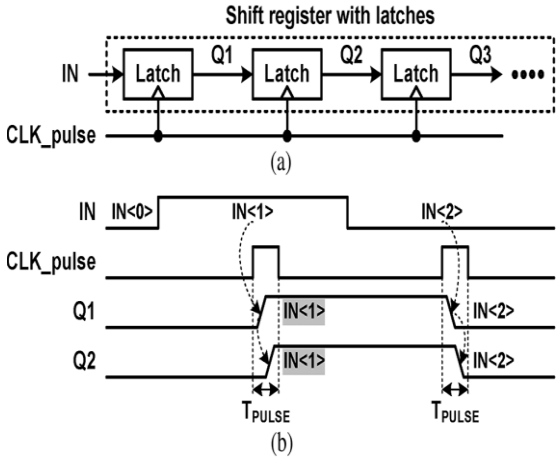

Fig 3: Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

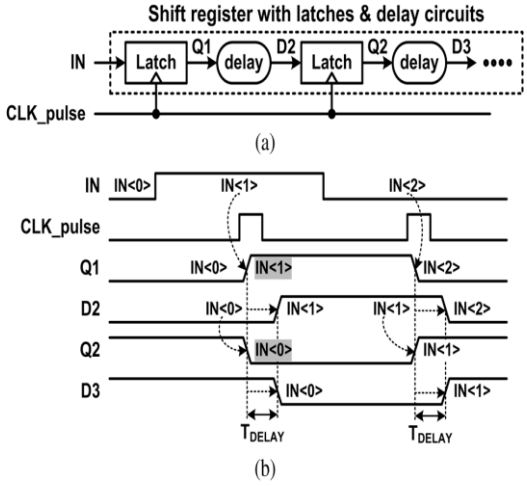

Fig 4. Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.

The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between latches, as shown in Fig. The output signal of the latch is delayed and reaches the next latch after the clock

pulse. As shown in Fig. the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches.

However, the delay circuits cause large area and power overheads. Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. Fig.(a) shows an example the proposed shift register.

III. SIMULATION RESULTS

In this project we implement the design by using sequential circuits. Those are:

1. Latches
2. Registers
3. Pulsed generator

In this first we implement 8-bit shift register. And we can extend the project by increase the bit length by 256.

In this simulation Results first, we give the reset value 1 then we get all are 0 that means we start the cycling by giving initial reset value. When we change the rst value 0 to 1 then only shifting process starts

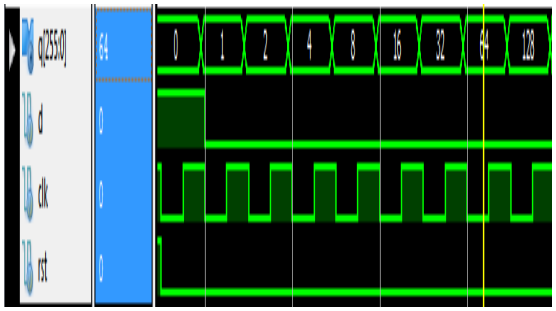

Fig 5: Simulation results when n=8

In this we increase the bit length from 8 to 256 here also the same process repeats means we can shift the values with the help of clock and reset value.

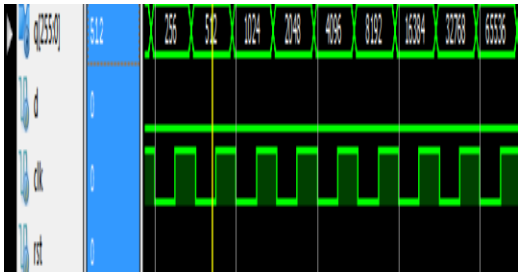

Fig 6: Simulation results when n=256

This is the RTL Schematic diagram for the proposed project. In this clock and reset are the inputs. And we give the data input by giving the D value and we get the final output of q.

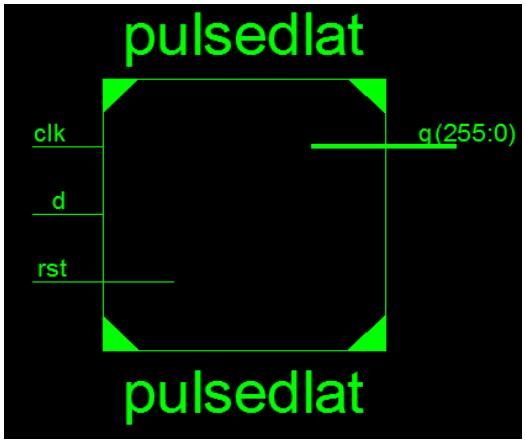

Fig 7: RTL schematic view pin diagram

This is the overall RTL schematic for the proposed project. In this internal we are having 2 sub modules. Those are

1. Shift register
2. dlatch

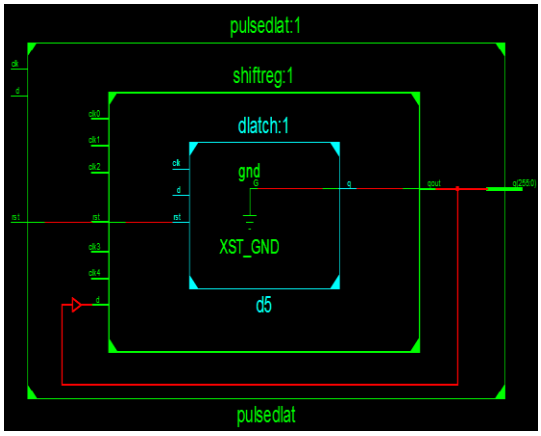

Fig.8. RTL schematic view

IV. CONCLUSION

The benefits of using the proposed design approaches in enhancing the robustness of pulsed latch circuits at different supply voltages were demonstrated using 16-bit registers. Both proposed approaches were able to ensure reliable operation of the pulsed latch-based register under different supply voltages in the presence of process and temperature variations, without any unnecessary timing overhead. Both approaches have a very small area overhead of around 3% or less. In addition, the power overhead of both approaches is minimal when compared to the traditional pulsed latch-based register at the same reliability level. Both approaches are easily scalable to cover different levels of voltage scaling. In addition, they can be applied to any other pulsed latches topology that depends on a delay path to generate the output pulse.In proposed design we are using latches due to the we are getting more delay. In Future Scope we implement the design to reduce the delay by change the architecture.

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