

Implementation of Switching System for 16 User Using VHDL

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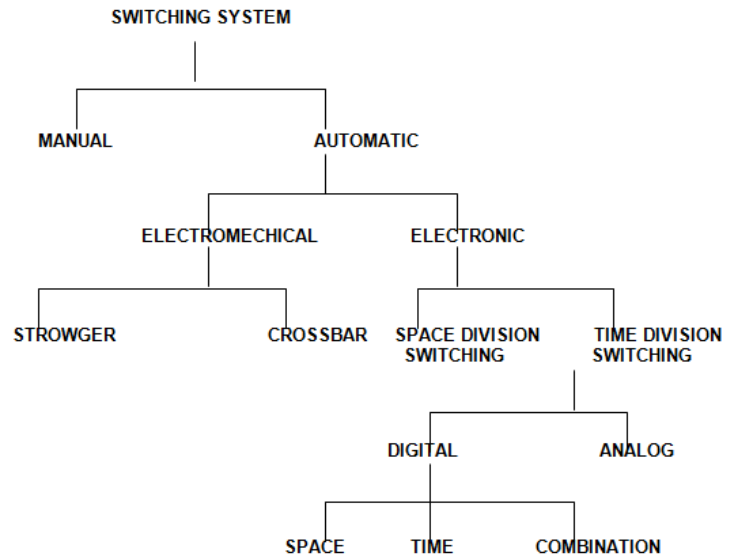
Abstract—switching system is used for data transmission between two communicating Channels. This transmission can be either via trunks (Landline) or it can be completely wireless, technically termed as Telephone Switching and Mobile switching, respectively. We report the implementation of a switching system using very high speed integrated circuit hardware description language (VHDL) which is more reliable and efficient than the present switching system. It converts entire bulky switching unit which consists of routers, multiplexers, decoders, counters in to a single integrated circuit (IC). Simulation results are presented for transfer of data from input subscriber to the output subscriber using sequential write /random read mode with the timing diagram. To verify the transfer of data from input subscriber to the output subscriber a 32 bit op-code is assumed in which each bit represents a specific function.

In this thesis we work on Landline Switching for two different channels using VHDL each channel have 16 users. They can communicate either intra channel or inter channel. We are also providing Caller ID facility in our work. In this work, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets. The incoming and out coming data is usually in serial form whereas the data are written into and read out of the memory in parallel form. It therefore becomes necessary to perform serial to parallel conversion and parallel to serial conversion at the inlets and outlets respectively. We are using 32 bit Opcode for communication between these channels or with in the channel. In this work we can define all the functions by Opcode. Opcode is responsible for caller id also and which data we are going to transmit or receive. We implement our work by Xilinx ISE i.e. responsible for synthesis also. For simulation we are using Modelsim 10.2a.

I. INTRODUCTION

In this switching system only one link per subscriber is required between subscriber and switching system and the total no of such links is equal to the number of subscriber connected to the switching system. Earlier switching system were manual and operator oriented. Limitations of operator oriented switching system were quickly recognized and automatic changes came into existence. Automatic switching systems can be classified as electromechanical and electronic. Electromechanical switching system include step by step and crossbar systems the step by step is common known as stronger switching system. The control functions in a stronger switching system are performed by circuits associated with the system. Crossbar systems had hardwired control systems, which uses relays and latches. These systems have limited

capability and it is virtually impossible to modify them to provide additional functionalities.



. In electronic switching the control functions are performed by a computer or a processor. Hence these systems are called stored program control. The switching system may be either space division switching or time division switching .In space division switching a dedicated path is established between a calling and called subscriber, whereas in time division switching sampled values of speech signals are transferred at fixed time interval. Time division switching may be digital or analog .Digital switching is divided into two parts space switch and time switch. If the coded values are transferred during the same time interval the technique is called space switching. If the values are stored and transferred to the output at a later time interval, the technique is called time switching.

1.2 Basics of Switching System:

A major component of a switching system or an exchange is the input and output circuits called inlets and outlets. The primary function of the switching system is to establish a path between inlet and outlet. The hardware used is the switching network. If there are N inlets and M, outlets, when N=M the network is called symmetrical network. The inlets and outlets may be connected may be connected to local subscriber or trunk from / to other exchanges .when all inlets and outlets are connected to subscriber lines the logical connection appears, In this case the output lines are folded back to input and hence called the folded network.

Four types of connection can be established:

1. Local call connection between two subscribers in the system.

2. Outgoing call connection between an incoming trunk and a local subscriber.
3. Incoming call connection between an incoming trunk and a local subscriber.
4. Transit call connection between an incoming trunk and outgoing trunk.

1.4.3 Point-to-Multipoint Channel:

By using the multi-port and/or port_array feature of VHDL and provide the second parameter of sc_port, the array size parameter can be set. At this point the idea is to provide of a number of like-defined ports. Here we assumed that our communications system has a number of interfaces all with the same connectivity and a number of N devices connected to it. Moreover by using dynamic instantiation feature of the modules and dynamic channel binding to the multiport interface of the transmitter. We can generate as much as we wanted from these devices. Dynamic instantiation and binding must be done before elaboration of the simulation. The multipoint structure of the system is constructed as shown in Fig. 1.3.

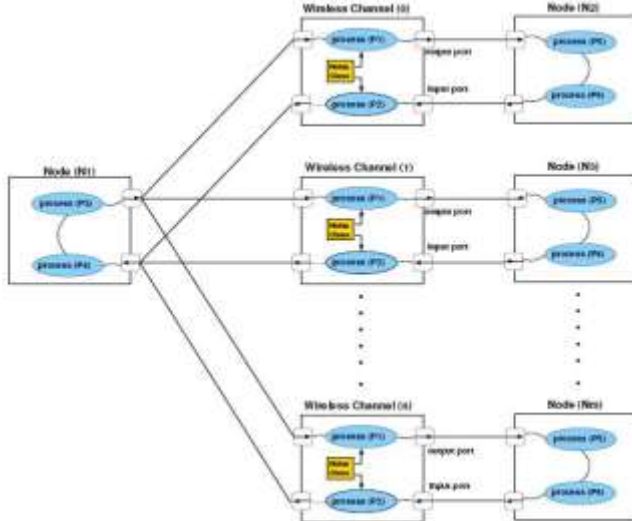


Fig. 1.3: Point to multipoint platform.

1.4.4 Multipoint-to-Multipoint Construction:

At this first stage of the implementation phase, our goal is to construct a channel model that can be used to support contention and noncontention based shared wireless channel access, and includes P2M and Multipoint-to-Multipoint (M2M) communication scenarios. The wireless channel module is responsible for carrying the data packets to all stations, and represents our communication medium in this work. The wireless channel module, as shown in Fig. 1.4, models the communication medium. It behaves like a multi-tap bus, where the multiple nodes are connected through it. The behaviour of the link has been modelled as a wireless communication medium.

In this scenario an external object called a 'mutual exclusion lock', or 'mutex', has been used to control access to the shared medium. The behaviour of a mutual exclusion lock is used to control access to a resource shared by concurrent processes. A mutex will be in one of two exclusive states: unlocked or locked. Only one process can lock a given mutex at one time.

Whenever a node has a packet to send, it tries to lock the mutex. When it locks the mutex it has access to the channel; the rest of the nodes have to wait until the node has released the channel. The other nodes may be subsequently locked by the mutex [7, 2].

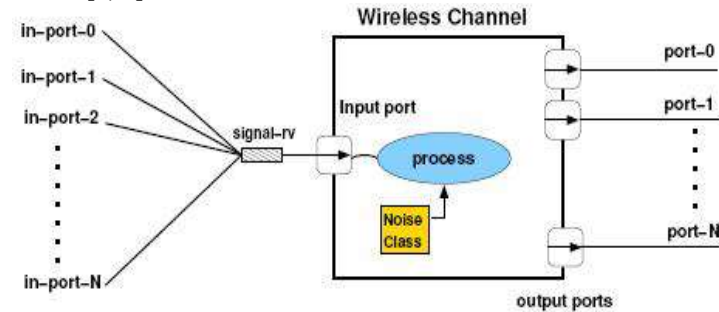


Fig. 1.4: Multipoint-to-Multipoint communication channel.

1.4.5 Data Packatization:

In data transmission process that achieved in this system, there is no mechanism to mark the beginning or end of a packet, so by using HDLC technique, the beginning and end of each packet has to be identified. This is done by using a packet delimiter, or flag, which is a unique sequence of bits that is guaranteed not to be seen inside a packet [8]. In this system, we have used Asynchronous Balanced Mode (ABM) which either combined stations may initiate a transfer.

II. RELATED WORK

2.3 Switching Mode Power Amplifier (SMPA) [3]:

Ahmed F. Aref et al , proposed a fully integrated adaptive multiband multimode switching-mode power amplifier (SMPA) in CMOS technology. The power amplifier (PA) module, consisting of input matching, driver, output stage, load transformation network (LTN), and auxiliary circuitry, utilizes optimized driving waveforms to increase output power and efficiency of a SWPA. The PA module is packaged in a 32 quad flat no-lead package. Based on the detailed analysis on appropriate driving waveforms, the SMPA is designed to maximize its output power and efficiency with minimum on-chip harmonic terminations. Furthermore, an adaptive gain control technique is proposed to control the SMPA gain at back-off while boosting the power-added efficiency (PAE) using a fully integrated tunable LTN. Employing both techniques concurrently enables us to have a multiband multimode SMPA. Measurements on a PA module designed in 90-nm CMOS and incorporating theses findings result in peak PAE of 43% for an output power of 27.1 dBm, associated with a large-signal gain of 22.1 dB at 1.97 GHz, when the devices are biased at 2.8 V. With the tunable LTN PAE at 4- and 6-dB backoff is 30% and 23%, respectively. To our knowledge, this is the first fully integrated multiband multimode SMPA in CMOS technology. [3].

They found a fully integrated adaptive multi band multi mode switching-mode PA is demonstrated in standard CMOS technology. The PA is adaptive in operating frequency and

output power utilizing a tunable LTN and an AGC technique. It exploits the performance improvement originating from the use of a unipolar square wave signal as drive for an inverse class-F PA. The proposed input signal leads to higher output power, lower odd harmonic frequency content in the output current, less input power, and thus improved gain and efficiency compared to other typical driving waveforms used at high frequencies. A prototype designed in 90-nm CMOS demonstrated an operating frequency bandwidth of 1 GHz with constant gain and output power. The PA can be configured to achieve PAE greater than 40% within a frequency bandwidth of more than 350 MHz. The achieved PA efficiency at 4- and 6-dB output power

back-off is 30% and 23%, respectively. Measured with variable supply voltage of the power stage in voltage steps of 0.4 V showed that a significant boost in PAE can be achieved with minimum switching between different LL configurations. A measured PAE of 33% at 6-dB back-off and 22% at 10-dB back-off have been achieved. Based on these results, using the proposed AGC technique in combination with the tunable LL network enables the presented PA module to be the enabling technology for next-generation CMOS fully integrated wideband and efficient wireless transmitters [3].

2.4 Switching Channel Bilateral Control [4]:

Dapeng Tian et al, worked on a switching-channel bilateral control with energy monitor (EM) was newly proposed to realize haptic communication through a wireless network. The varying delay in the communication line and the situation of duplex operation are considered. In such a system, human operators on two sides of the master-slave robots system feel the hardness of the remote environment placed on the contralateral side. The EM approach is presented to judge the role of the robot (manipulated by an operator or contacting an environment), which provides a beacon for the switching algorithm. The position tracking of the system is improved by switching off the channel of force control in the human manipulated robot. The problem of position drift in traditional methods is overcome. Disturbance observer is applied to simplify the design of the bilateral control law, and to guarantee the efficient force switching. Because of improved position tracking and satisfactory force fidelity, the proposed approach achieves more vivid haptic transmission. By experiments, the validity is verified. [4].

They conclude a new switching bilateral control with EM to achieve an effective duplex haptic communication. The study faces to make use of the technique of wireless network, which extends the haptic communication to more flexible implementation. There was varying communication delay in such a system. To achieve satisfactory performance, the EM and the switching-channel bilateral control are proposed. The EM detects the manipulated robot by the work applied on each robot. According to the detection, the bilateral controller switches off the force channels in the human operated robot, and exerts the human force directly on the remote robot via a communication line. The algorithm guarantees both force

fidelity and tracking between the robots. The stability of the system is ensured by the damping in each robot. Not only the theoretical work, experiments are also implemented. Two single-degree-of-freedom robots are employed. A cable/wireless combined network is organized as the communication line. According to the results, the proposal effectively avoids the problem of position drift or overshoot of traditional methods, and provides vivid feeling of the hardness of the remote environment. In future work, the proposal will be extended to the situation of a multidegree-of-freedom robots system. In addition, other tools will be considered to optimize the communication lines, such as using Fourier analysis to check the characteristic of the delay variation, and using the Kalman filter to improve the network communication in practice [4].

2.6 Switching IC's [7]:

Rajitram Singh et al, they focused on the programming part as well as the hardware, thus proving a step towards the future development of 'Switching ICs'. Here they explain every model in detail with their opcodes (user defined), underlying architecture and programming. Along with are also provided the simulation results showing transfer of signals and data. Simulator also provides the timing information. This work is an outcome of the comprehension and utilization of many recent subjects they have studied and is in itself an original concept [7].

The aim of work was to enable us to design ICs for the Switching System. Presently switching systems use multiplexers, routers, switches etc that leads to low efficiency as they are analog in nature and have a high power requirement. In contrast they have tried to make this whole system digital to increase the efficiency, lower the power requirement, and reduce the delay. VHDL has been used to write all the programs for the ICs because of its user-friendly nature and thus modifications if required for further development shall not prove to be an obstacle. As they know, the process of making ICs is time consuming and an expensive venture so they must be sure about the working results of the ICs in advance as they can't accept errors later. Thus the work focuses on simulation prior to fabrication. Burning these programs on FPGA (Field Programmable Gate Array) will help us to see the functional design of ICs. These results in addition to the systematic view generated would help us to design Application Specific (AS ICs) [7].

III. Methodology

3.1 Introduction:

In present scenario of the technology, there are two fields in engineering that hold great demand in the industry; communication and VLSI. The people want to connect themselves to anyone, anytime and anywhere. We have already experienced a huge development from a simple morse code telegram to the highly sophisticated triple play broadband ISDN, or nonetheless the Satellite Communication. This might give you ways to communicate with speech, that's

no big deal; in fact the amazing part starts when real time audio, video and data can be integrated for communication. But at present there is also a second stringent demand that is miniaturization. The race is on for reaching the minimum space as much as possibly occupied by the systems. This paper, keeping an eye wide open on the future, has mixed both fields enabling us to communicate, in a digital manner, by using systems that would be integrated on an IC through programming of the IC using VHDL.

VHDL is a language for describing digital electronic systems. There was a need for a standard language for describing the structure and function of integrated circuits (ICs). Hence the VHDL was developed, and subsequently adopted as a standard by the Institute of Electrical and Electronic Engineers (IEEE) in the US. VHDL is designed to fill a number of needs in the design process. Firstly, it allows description of the structure of a design that is how it is decomposed into sub-designs, and how those sub-designs are interconnected. Secondly, it allows the specification of the function of designs using familiar programming language forms. Thirdly, as a result, it allows a design to be simulated before being manufactured, so that designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping [1].

This work focuses more on the programming part rather than the hardware. We have explained every model in detail with their opcodes (user defined), underlying architecture and programming. Along with that the simulation results are also provided, showing transfer of data from input subscriber to output subscriber using sequential write/ random read method with timing information. To verify the transfer of data from input subscriber to the output subscriber a 16 bit op-code is assumed in which each bit represents a specific function.

1.2 Proposed Work:

A major component of a switching system or an exchange is the input and output circuits called inlets and outlets. The primary function of the switching system is to establish a path between inlet and outlet. The hardware used is the switching network. If there are N inlets and M, outlets, when $N=M$ the network is called symmetrical network. The inlets and outlets may be connected may be connected to local subscriber or trunk from / to other exchanges .when all inlets and outlets are connected to subscriber lines the logical connection appears, In this case the output lines are folded back to input and hence called the folded network.

Four types of connection can be established:

1. Local call connection between two subscribers in the system
2. Outgoing call connection between an incoming trunk and a local subscriber
3. Incoming call connection between an incoming trunk and a local subscriber
4. Transit call connection between an incoming trunk and outgoing trunk

1.2.1 Principle of Landline Switching

In this design, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets. The incoming and out coming data is usually in serial

form whereas the data are written into and read out of the memory in parallel form. It therefore becomes necessary to perform serial to parallel conversion and parallel to serial conversion at the inlets and outlets respectively.

For convenience, the in and data out parts of the MDR are shown separately for the data memory. Since there is only one MDR a gating mechanism is necessary to connect the required inlet/outlet to MDR. This is done by the in gate and out gate units. The information is not transferred in real time: it is first stored in the memory and later transferred to the outlet.

There is a time delay between the acquisition of a sample from an inlet and its delivery to the corresponding outlet. This switching system can be controlled in following three ways:

1. Sequential write/Random read.
2. Random write/Sequential read.
3. Random input/Random output.

In the first two methods of control, the sequential / random read / write operations refer to the read / write operations associated with the data memory. In both these cases, the inlets and outlets are scanned sequentially. In the last case, the inlets and outlets are scanned randomly, and the data memory is accessed sequentially.

1.3 Working Specifications:

Phase 1: Input Subscribers in both the exchanges are scanned sequentially. It takes 16 clock cycles to scan 32 subscribers in order to know their status, that is they want to transmit or not. This is called a sequential scanning. The data to be transmitted is stored in data memory in sequential order. The information relating to the called subscriber is stored in control memory in sequential order and caller id number is stored in the caller id memory in the same way. Thus we can say system is sequential write.

Phase 2: When all the scanning is finished the location of the data memory is read according to the corresponding location of the control memory. For example, if first location of data memory has data 'd' and corresponding location in control memory is 2, this means that 'd' will be communicated to the 2nd user of the exchange, thus we can say the system is random read.

To decide where the data will be communicated we use a bit in our op code as 'I' bit. If 'I' =1, then it is interexchange, i.e. the read out data will be given to user of other exchange. Thus communication between the subscriber of two exchanges can be made possible and hence the name interexchange.

IV. Result and Discussion

4.1 Simulation Results:

There are two exchange centers which taken as 'din' and 'dout'. Our work has been implemented for inter exchange and Intra exchange both. If we take 'I' is one then our design will work for inter exchange. If we take 'I' is zero then our design will work for Intra exchange. Our design is depend on some more inputs clock, reset and enable. If reset is high then our design will not perform any function, all functions performed on low reset and positive edge of clock. If enable is

zero then there is no exchange of data. Our exchanges are work on high enable bit.

In this case we shows the inter exchange for second exchange. Here we take enable bit 1, I as 1, source address is 1100, and destination address is 0010 data for transmission is "1234". We receive that data on second exchange din on 2nd address shown in fig 4.3

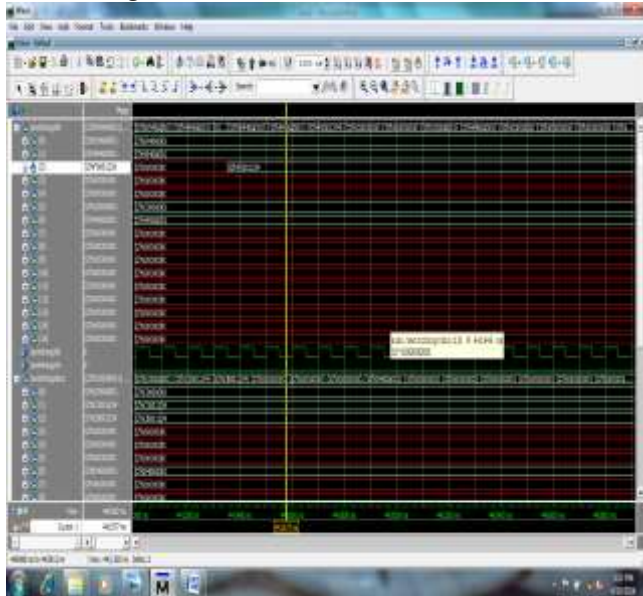
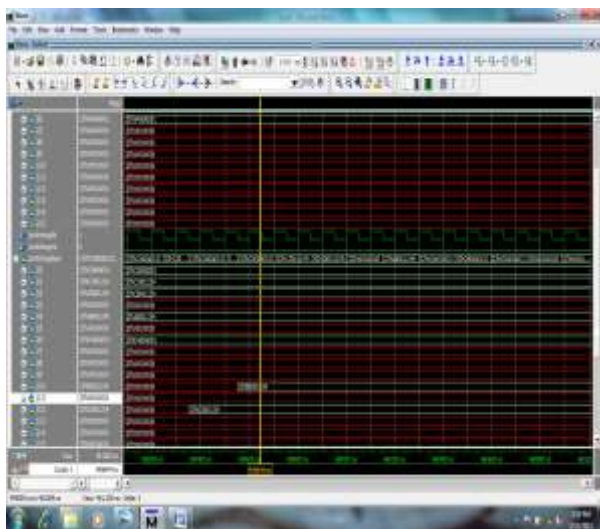


Fig 4.3: Simulation result for Second Exchange (Inter Communication)

In this case we shows the intra exchange for second exchange. Here we take enable bit 1, I as 0, source address is 1100, and destination address is 1010 data for transmission is "1234". We receive that data on second exchange dout on 10th address shown in fig 4.4.



4.2 Synthesis Results:

Fig 4.5 shows the RTL of our code, fig 4.6 shows the internal RTL and fig 4.7 shows the devices utilized in our work. Here we attach the synthesis report of our code.

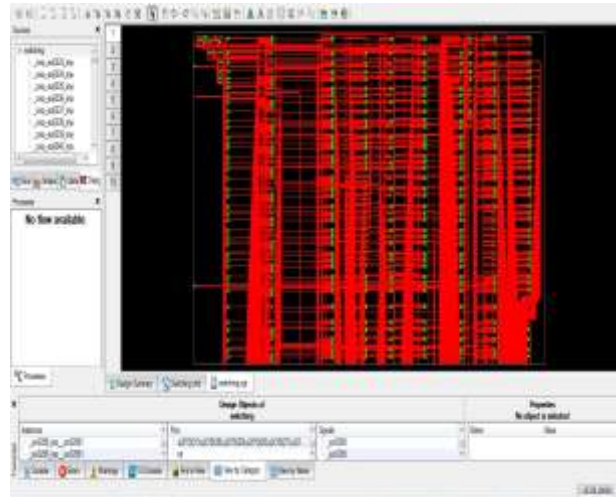


Fig 4.6: Internal RTL

V. Conclusion:

The aim of work was to enable us to design ICs for the Switching System. Presently switching systems uses multiplexers, routers, switches etc that leads to low efficiency as they are analog in nature and have a high power requirement. In contrast we have tried to make this whole system digital to increase the efficiency, lower the power requirement, and reduce the delay. VHDL has been used to write all the programs for the ICs because of its user-friendly nature and thus modifications if required for further development shall not prove to be an obstacle. As we know, the process of making ICs is time consuming and an expensive venture so we must be sure about the working results of the ICs in advance as we can't accept errors later.

In our design we used 3659 slices out of 192 i.e. only 1905% we used in our design, 2678 slices of flip flop used out of 384 i.e. only 697% utilized, 6267 Look Up Tables (LUT) are used out of 384 i.e. 1632% utilized in our design and 1 global clock we have used out of 4 i.e. 25% we used in our design then we conclude that it will take less hardware to perform whole operations. We get total delay of our design is 7.148ns if describe that delay i.e. 5.753 ns is from logic delay means which component used in our design that are taking delay to perform operation and 1.665 ns for routing delay means connection delay of our design. So we conclude that our design is fast and taking less hardware.

5.2 Future Scope:

Despite the revolutionary talk of all IP networks, such are the capabilities of Switching System that it will become an integral part of Network infrastructure. More importantly, however, there is a tremendous investment in the conventional network that has not stopped. Switching System requirements continue to grow and access to Switching System signaling remains as essential as ever. Indeed, with a growing set of

service providers and operators emerging, its importance is almost certainly increasing.

Switching System allows a service provider to maximize connectivity options and it remains the best way to access the large subscriber bases that connect to the PSTN. Indeed, for most operators it is the preferred means of network connectivity and is not a matter of choice. New standards that built on its proven capabilities are emerging, such as WIN and CAMEL, and it is destined to play a huge role in 3G Mobile networks. In the network core it is likely to remain unchallenged for some considerable time and with the advent of new IP-based networks, it is likely to play a key role in the next generation of public networks.

Thus the work focuses on simulation prior to fabrication. In future this work can program on FPGA (Field Programmable Gate Array) will help us to see the functional design of ICs. These results in addition to the systematic view generated would help us to design Application Specific (AS ICs).

REFERENCES

- [1] Rajeev Sivaram et al, "Implementing Multidestination Worms in Switch-Based Parallel Systems: Architectural Alternatives and Their Impact", *IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS*, VOL. 11, NO. 8, AUGUST 2000.
- [2] Krishna V. et al, "Energy Aware Computing through Probabilistic Switching: A Study of Limits" *IEEE TRANSACTIONS ON COMPUTERS*, VOL. 54, NO. 9, SEPTEMBER 2005.
- [3] Ahmed F. Aref et al, "A Fully Integrated Adaptive Multiband Multimode Switching-Mode CMOS Power Amplifier" *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, VOL. 60, NO. 8, AUGUST 2012.
- [4] Dapeng Tian et al, "Wireless Haptic Communication Under Varying Delay by Switching-Channel Bilateral Control With Energy Monitor" *IEEE/ASME TRANSACTIONS ON MECHATRONICS*, VOL. 17, NO. 3, JUNE 2012.
- [5] Prashant Rai et al, "VHDL Implementation of a prototype switching system" Department of ECE, Dehradun Institute of Technology, Mussoorie Diversion Road Dehradun, Uttarakhand-248009, India (CAC2S 2013).
- [6] Gopinath Chakraborty et al, "HUMAN NETWORK COMMUNICATION" *International Conference on Information Systems and Computing (ICISC-2013)*, INDIA.
- [7] Rajitram Singh et al, "FPGA Implementation of Switching System Using VHDL" *International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459 (Online), An ISO 9001:2008 Certified Journal, Volume 3, Special Issue 2, January 2013)*.
- [8] R. Nandhini et al, "PERFORMANCE ENHANCEMENT OF LAND MOBILE SATELLITE SYSTEM", *International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459 (Online), An ISO 9001:2008 Certified Journal, Volume 3, Special Issue 1, January 2013)*.
- [9] Huaqing Li et al, "Second-Order Consensus Seeking in Multi-Agent Systems With Nonlinear Dynamics Over Random Switching Directed Networks" *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS*, VOL. 60, NO. 6, JUNE 2013.
- [10] Roberto Conti et al, "Simulation and Optimization of Railway Traction Systems Respect to an Expected Mission Profile" University of Florence, Dept. of Industrial Engineering, Via Santa Marta 3, 50139 Firenze, Italy.
- [11] Ibrahim Aref et al, "System Level Modeling of a Digital Communication Channel Based on SystemC" *International Journal of Future Computer and Communication*, Vol. 2, No. 3, June 2013.