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High Speed Vlsi Architecture For Proposed Novel Adiabatic Encoder And Decoder

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ABSTRACT: *In this paper Sample adaptive encoder architecture is used as new in-loop filtering block. Exhaustive operations are performed to get the optimum AO parametersbecause of the huge amount of samples. In this paper we propose an High speed and low power Encoder Decoder of rate ½ convolutional coding with a constraint length K = 3. At last we justify that using both logics in one Integrated Circuit (IC) we can create a high speed and low power Proposed encoder decoderwith some extra hardware area*

KEY WORDS: in-loop filtering, sample adaptive encoder, high efficiency video coding.

I.INTRODUCTION

One of the main problem in real time communication is repetition of corrupt messages. Here the data should be delivered with low delay and the use of techniques will avoid the overloads by transmitting. During the digitalinformation transmitting through a channel, practicallyinevitable errors are produced. To ensure reliable transmission,the data are further encoded via Error Correcting Code (ECC).This could be used to recognize and correct errors. In this workthe well-known binary linear block Hamming codes are usedbecause they have been used in the optimization problems that we accelerate thanks to the circuitexplained further on.A binary linear (N, k) code is a k-dimensional subspaceof the space of N-bit codewords, and therefore has 2^Kcodewords. But we solve for blocks or subsets of Mcodewords in the code, where $M \leq 2^K$, used to transmit amessage. When a message is transmitted, its binary stringcan suffer modifications (changed bits), arriving an incorrectcodeword in the receiver side.

As technology scales, reliability becomes a challengefor CMOS circuits. Reliability issues appear, for example during device Manufacturing, as defects that can compromiseproduction yield. Once the devices are in thefield, other reliability issues appear in the form of soft errors or age induced permanent failures. Memory devices are among those affected bythose issues due to their high level of integration. Current techniques to address those reliability issues in memories includethe use of redundant elements to repair manufacturing defects,and the use of Error Correcting Codes (ECC) to deal with softerrors once the device is in operation. Different techniques areused to deal with defects versus soft errors. ECC can also beused to correct errors caused by defects, but then their abilityto correct soft errors may be compromised leading to a reducedreliability. However, to the best of our knowledge, there is noprevious work on how the use of ECC to deal with defects affects the reliability of memory in thefield.

Networking applications require high-speed processing of data and thus rely oncomplex integrated circuits. In routers and switches, packets typically enter the devicethrough one port, are processed, and are then sent to one ormore output ports. During this processing, data are stored and moved through the device. Reliability is a key requirement for networking equipment such as core routers. Therefore, the stored data must beprotected to detect and correct errors. This is commonly doneusing error-correcting codes (ECCs.One problem that occurs when protecting the data in networking applications is that, to facilitate

its processing, a fewcontrol bits are added to each data block. For example, flags tomark the start of a packet (SOP), the end of a packet (EOP), oran error (ERR) are commonly used. These flags are used todetermine the processing of the data, and the associated control logic is commonly on the critical timing path. To access thecontrol bits, if they are protected with an ECC, they must firstbe decoded. This decoding addsdelay and may limit the overallfrequency.Several codes are used to evaluate the proposed method. After evaluation it is compared with the existing solutions in terms of decodingdelay and area.

II. EXISTED SYSTEM

The below figure (1) shows the architecture of existed system. The existed architecture of SAO encoder is divided to three modules they are Statistics collection module, parameters determination module and controller. Let us discuss each module in detail.

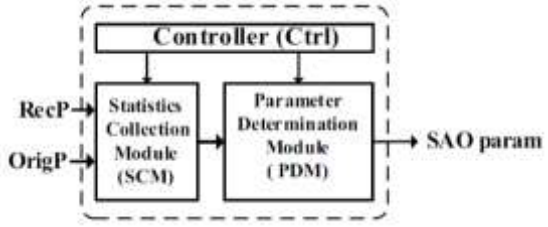

Fig. 1. Existed system

The SCM produces N and E of 4X4 pixels per cycle as follows. Each cycle consists of 6X6RecP and 4X4OrigP. These are registered to SCM. A signed difference (D)
Between OrigPand RecPis generated and clipped into −7∼7 through subtractor and clipper module. An *a*llocatoris used to reorder RecP and D to be inputted to both EO and BO engines. Each EO class x engine works on the corresponding allocator output, it mainly consists of four Cat.x matching sub modules. This is about SCM module, let us discuss about PDM module.

PDM works for 56 cycles to produce the optimum SAO parameters of the current CTB. Parameter determination moduleconsists of four cores, E and N components. This components generates Minimum cost and offset generator and Group & Compare core (GAC) plus storage elements. Next one is controller, itworks for reducing switching activity and the power consumption of the SAO encoder. Controller inputs data and triggers clock when required. The Clock gating technique is adopted to ensure pipelining. But this system does not produce better results so a new system is proposed which is discussed in below section.

III. PROPOSED SYSTEM

In this paper we proposed a design of high speed low power encoderdecoder at the RTL level in the standard cell designenvironment. In the standard cell designenvironment, the behaviour of a design is described inVHDL. The behavioural design is synthesized togenerate a gate level design. The gate-level design isplaced and routed to generate a layout of the design. Theadvantages of a standard cell based design over full custom design are faster turnaround time for thedesign, ease in design verification and more accuratemodelling of the circuit. From below figure (2) we can observe the proposed encoder architecture.

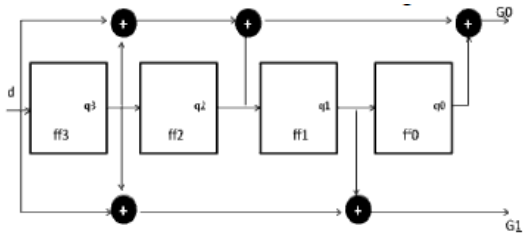

Fig. 2. . Proposed encoder

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The encoder produces two bits ofencoded information for each bit of input information, so itis called a rate 1/2 encoder. A convolutional encoder isgenerally characterized in (n, k, m) format, where n isnumber of outputs of the encoder; k is number of inputs ofthe encoder; m is number of memory elements (flip-flops)of the longest shift register of the encoder.The rate of a (n, k, m) encoder is k/n. from below figure (3) we can observe the proposed decoder architecture.

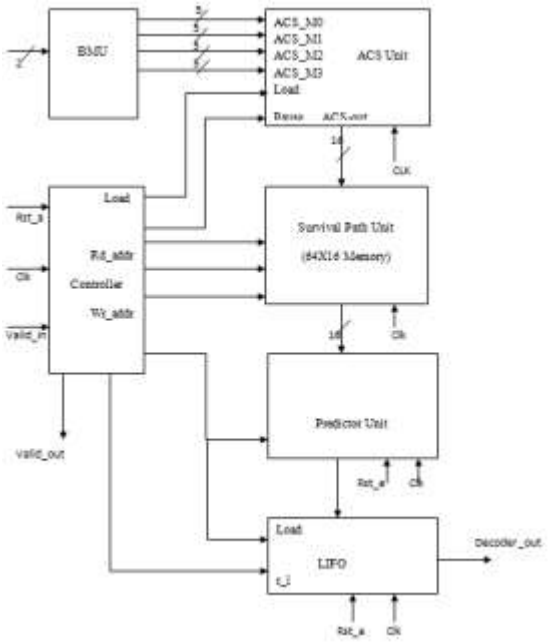

Fig. 3. Proposed decoder.

This sectiondiscusses the different parts of the proposed decodingprocess. Analog signals are quantized and converted intodigital signals in the quantization block. We assume that a proposed decoder receives parallel successive code symbols,in which the boundaries of the symbols and the frameshave been identified. Let us discuss about each unit in detail manner.

The BM unit is used to calculate branch metric for all trellis branches from the input data. We choose absolute difference as measure for branch metric. These branch metrics are viewed as being the weights of the branches.The Add-Compare-Select (ACS) unit is the module that consumes the most power and area.Memory is required to store the survivor Path Matrix Unit (PMU) and the memory used is dual port. One port for writing the data and other for reading the data.A controller is used to synchronize between the different modules of the system.Predictor unit uses the state value to access a bit from the path metric memory unit (PMM). LIFO unit has 2 32-bit registers in which one of the register is read while the other is written.

IV. RESULTS

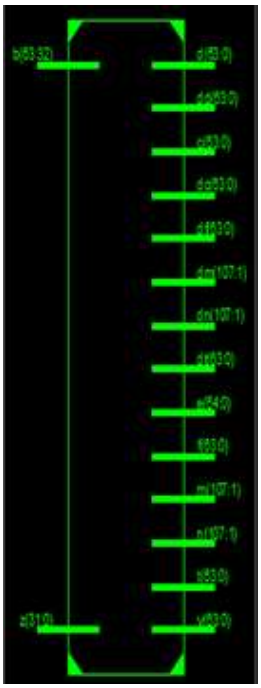

Fig. 4. RTL Schematic

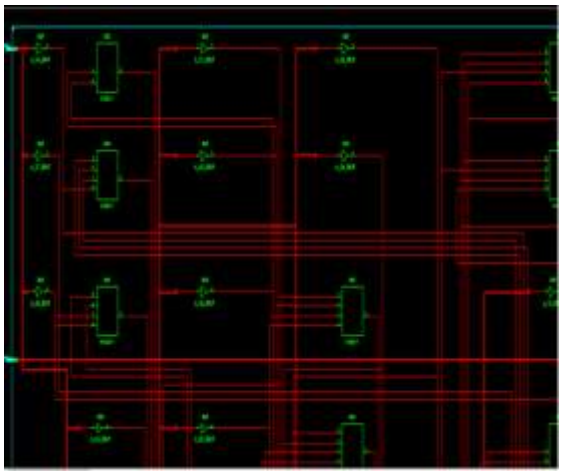

Fig. 5. Technology schematic

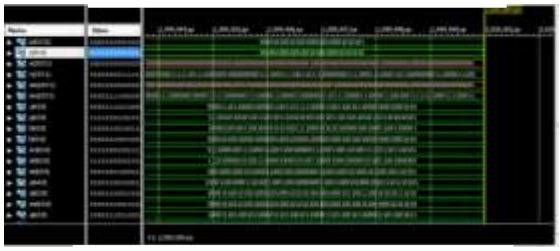

Fig. 6. Output waveform

V. CONCLUSION

In this paper a low cost high throughput high performance VLSI architecture for SAO encoding stage is presented. Our proposed encoder decoderarchitecture designs a high speed and power consumptiondecoder. For high speed datatransmissioncommunicationprotocols are used. At last compared to existed system, the proposed system gives better efficiency.

VI. REFERENCES

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