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Design and Implementation of a High Speed CSKA Brent Kung Adder

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ABSTRACT: In order to perform the addition of two numbers adder is used. Adder also forms the integral part of ALU. Besides this application of adder in computer, it is also employed to calculate address and indices and also operation codes. Different algorithm in Digital Signal Processing such as FIR and IIR are also employed using adder. The important areas of VLSI areas are low power, high speed and data logic design. In Carry Select adder the possible value of input carry are 0 and 1. So in advance, the result can be calculated. Further we have the multiplexer stage, for calculating the result in its advanced stage. The conventional design is the use of dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA (Cin=l) is replaced by Brent kung adder. As, RCA (for Cin=O) and Brent Kung adder (for Cin=l) consume more chip area, so an add-one scheme i.e., Binary to Excess-l converter is introduced. Also the square root adder architectures of CSA are designed using Brent Kung adder in order to reduce the power and delay of adder.

Keywords- Brent Kung (BK) adder, Carry Select Adder, Delay, Area

I. INTRODUCTION

Binary adders are one of the most basic and widely utilized arithmetic operations in modern integrated circuits. They play a critical role in determining the performance of the design. Arithmetic operations are the regular common operations in digital integrated circuits. The simplest circuit adds, subtracts, and multiplies or divides. The computation should be very fast and the area consumed by the arithmetic units should be small. These are the two basic requirements for any adder.

Ripple carry adder is the first and most fundamental adder which is capable of performing binary number addition. Since, its latency is proportional to the length of its input operands, it is not very useful. Carry look ahead adder is introduced to speed up the addition. Parallel prefix adders produce good results as compared to the conventional adders. The adders with the large complex gates will be too slow for VLSI, so the design is modularized by breaking it into trees of smaller and faster adders which are more readily implemented.

High speed adders depend on the previous carry to generate the present sum. In integer addition any decrease in delay will directly relate to an increase in throughput. In nanometer range, it is very important to develop addition algorithm that provide high performance while reducing power. Parallel prefix adders are more suitable for VLSI implementation because they rely on the utilization of simple cells and maintain regular connection among them. We can define each prefix.

In ripple carry adder each bit full adder operation contains sum and carry, that carry will be given to next bit full adder operation, that process is continuous till

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the Nth bit operation. The N-1th bit full adder operation carry will be given to the Nth bit full adder operation which is present in the ripple carry adder.

For 16-bit ripple carry adder, the first bit carry is given to second bit full adder, second bit carry is given to the third bit full adder, similarly the operation is continue till fifteenth bit carry is given to sixteenth bit full adder. The addition operation is performed from least significant bit to most significant bit in ripple carry adder.

Carry look ahead adders are based on parallel prefix computation which gives better performance than ripple carry adder. After so many years of research, focus is kept on improving the delay performance of the adder. The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including Arithmetic and Logic Unit (ALU), microprocessors and Digital Signal Processing (DSP). At present, the research continues on maximizing the adder's delay performance.

In many practical applications such as mobile and telecommunications, the Speed and power performance improvement in FPGAs is better than microprocessor and DSP's based solutions. Additionally, power is also a most important aspect in growing trend of mobile electronics, which makes large-scale use of DSP functions.

II.EXISTED SYSTEM

The existed structure is based on combination of the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, it is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates.

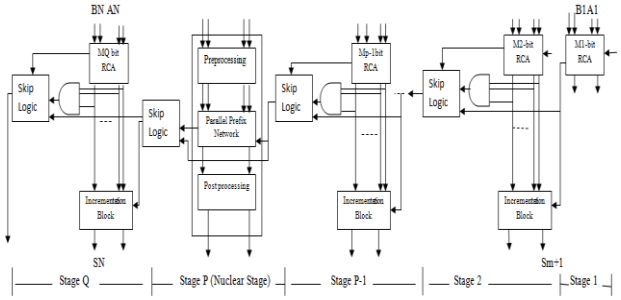

Fig. 1 Structure of the existed hybrid variable latency CSKA

The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented.

Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the existed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

III. PROPOSED SYSTEM

Brent Kung adder is used for high performance addition operation. The Brent-kung is the parallel prefix adder used to perform the addition operation. It is looking like tree structure to perform the arithmetic operation. The Brent-kung adder consists of black cells and gray cells. Each black cell consists of two AND gates and one OR gate. Each gray cell consists of only one AND gate. pi denotes propagate and it consists of only one AND gate given in equation 1. gi denotes generate and it consists of one AND gate and OR gate given in equation 2.

pi= Ai XOR Bi -------- (1)
gi= Ai AND Bi ---------- (2)

Gi denotes carry generate and it consists of one AND gate and OR gate given in equation 3 used for first black cell.

Gi=pi OR [gi AND cin] --- (3)

The proposed Brent-kung adder is more flexible to speed up the binary addition and the arrangement is like tree structure for the high performance of arithmetic operations. In recent years, Field programmable gate arrays are mostly utilized because they improve the speed of microprocessor based applications such as mobile communication, DSP and telecommunication. The efficient Brent-kung adder contains two stages. They are pre-processing stage and generation stage.

Pre-Processing Stage: In the pre-processing stage, generate and propagate are from each pair of the inputs. The propagate gives “XOR” operation of input bits and generates gives “AND” operation of input bits. The propagate (Pi) and generate (Gi) are shown in below equations 4 & 5.

Pi=Ai XOR Bi ------ (4)
Gi=Ai AND Bi ----- (5)

Generation Stage: In this stage, carry is generated for each bit is called carry generate (Cg) and carry is propagate for each bit is called carry generate (Cp). The carry propagate and carry generate is generated for the further operation, final cell present in the each bit operate gives carry. The last bit carry will help to sum of the next bit simultaneously till the last bit. The carry generate and carry propagate are given in below equations 6 & 7.

Cp=P1 AND P0 ---------- (6)
Cg=G1 OR (P1 AND G0) ------ (7)

The above carry propagate (Cp) and carry generation (Cg) is black cell and the below shown carry generation in equation 8 is gray cell. The carry propagate is generated for the further operation. The final cell which present in the each bit operation provides carry. The last bit carry will lead to sum of the next bit simultaneously till the last bit. This carry is used for the next bit sum operate, the carry generate is given in below equations 8.

Cg=G1 OR (P1 AND G0) ------ (8)

The carry of a first bit is XORed with the next bit of propagates then the output is given as sum and it is shown in equation 9.

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Si=Pi XOR Ci-1 ------ (9)

It is used for two thirty-two bit addition operations and each bit undergoes preprocessing stage and generation stage then gives the final sum. The first input bits goes under pre-processing stage and they will produce propagate and generate. These propagates and generates undergoes generation stage produces carry generates and carry propagates then gives final sum.

The efficient Brent-kung adder arrangement is look like tree structure for the high performance of arithmetic operations and it is the high speed adder which focuses on gate level logic. The proposed adder design reduces the number of gates. So, it decreases the delay and memory used in this architecture. The efficient Brent-kung adder is shown in fig.3 which improves the speed and decrease the area for the operation of 32-bit addition. The input bits Ai and Bi concentrates on generate and propagate by XOR and AND operations respectively. The propagates and generates undergoes the operations of black cell and gray cell and produce the carry Ci. That carry is XORed with the propagate of next bit, that gives sum.

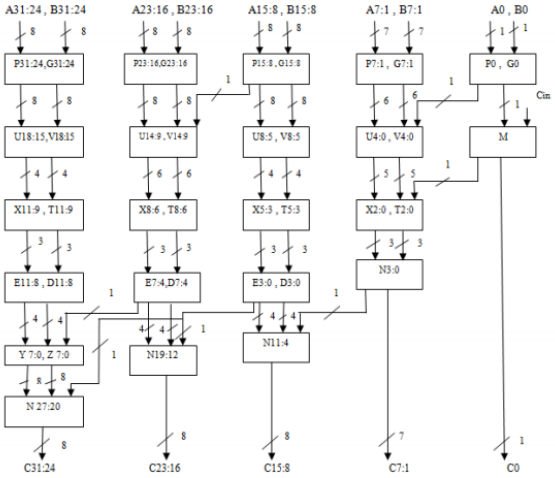

Fig 3. 32- bit Brent Kung Adder

The architecture of 32-bit Efficient Brent-kung adder is shown in Fig.4. The logical circuit is using multiple adders to find the ans i.e., sum of N-bit numbers. Each addition operation has a carry input (Cin) which is the previous bit carry output (Cout). Research on binary addition innovatively motivates gives development of devices.

IV. RESULTS

Fig 4. RTL Schematic

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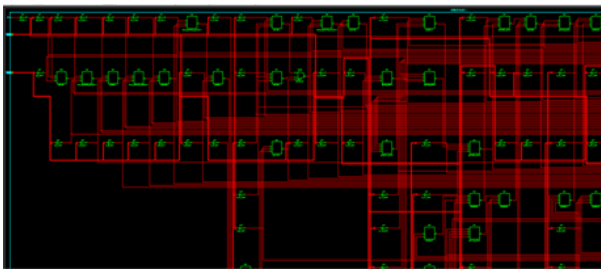

Fig 5. Technology Schematic

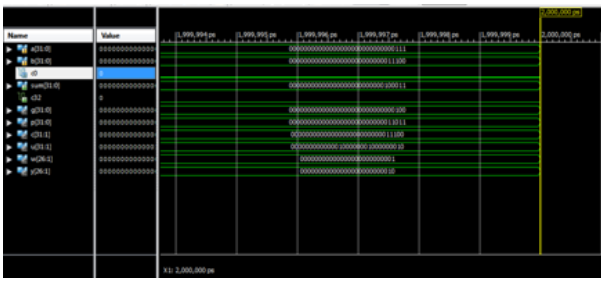

Fig 6. Output

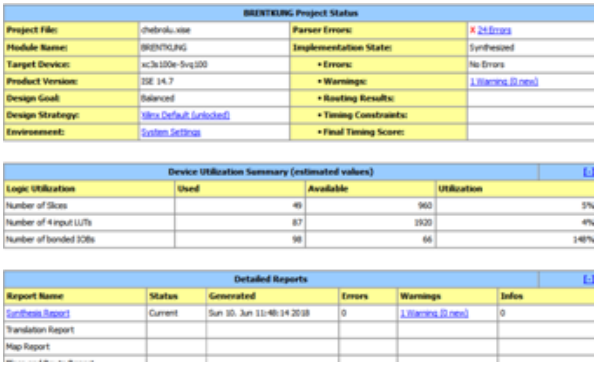

Fig 7. Report

V. CONCLUSION

In this paper, new approach is to design an efficient Brent-kung adder look like tree structure and cells in the carry generation stage are decreased to speed up the binary addition. It concentrates on gate levels to perk up the speed and decreases the memory used. The proposed adder addition operation offers elude great advantage in reducing delay.

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