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Reliable Low- Latency Viterbi Algorithm Architectures Using LFSR

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ABSTRACT: Viterbi algorithm [V.A] is utilized in various applications such as cellular relay, satellite communication, and networks of wireless local area. This algorithm is mainly applied to the decoding conventional codes and also to automatic speech recognition and storage devices. In architecture of Viterbi algorithm, we are utilizing scheme of error detection which is based on the low complexity and low latency. The main benefit of this proposed system is that it gives reliable requirements and as well as performance degradation. We utilize three variants in the system which is recomputed with the encoded operands. Thus, this system is modified when we detect the both permanent faults [P.F] and transient faults which are mixed with signature based methods. Here, we are utilizing architecture of instrumented decoder for the motive of extensive error detection assessments. For the motive of bench mark we are improving the both application specific integrated circuit and field programmed gate array. Depend upon the reliability objectives and performance degradation tolerance, the proposed system is utilized.

KEY WORDS: Viterbi algorithm[V.A], permanent faults[P.F]

I.INTRODUCTION

The main intent of this Viterbi algorithm is to decode the convolution codes. Decoding of this algorithm is utilized in many applications such as satellite communication, cellular and radio relay. Generally this Viterbi algorithm is implemented with serializer and deserializer constraints which have critical latency.

This serializer and deserializer are widely used in local area and synchronous optical networks. In the same way it is used in the magnetic storage systems like hard disk drive or digital video disk. This algorithm consists of possible number of states.

Branch metric unit (BMU) and add-compare-select (ACS) and survivor path memory (SPM) are the three components of Viterbi algorithm. Coming to the branch metric unit, it produces

the metrics which are corresponded to the binary trellis and all this process will depends upon the received signal. Next one is survivor path memory, it manage the paths and gives the decoded data as output. An add-compare-select component consists of feedback loops. By using the iteration schemes we can limit the speed of the system.

In the Viterbi decoder we are using M-step look ahead technique to break the iteration bound. Here the look head technique will combine the several trellises Step to one trellis step. Branch metric pre-computation technique will dominates the entire complexity of the system. For every two consecutive steps there are pipelined registers in the BMP. Add operation is performed before the saturation of trills but after the saturation of trills the add operation is followed by compare operation. In this compare operation we need a parallel path which consists of less metrics.

The Viterbi algorithm is used in convolution codes, this convolution codes produces the output which degrade the accuracy of decoding. Basically, the errors will occur in digital systems because of logic delay, alpha particles. In the same way, in advanced process technologies the errors are obtained due to the device shrinking, reduce power supply voltages and higher operating frequencies. Here the energetic protons and electrons are obtained due to the cosmic rays in single transients. So to avoid these errors we use the error detection scheme. This error detection technique is used in hardware architecture with various domains.

Now, this proposed Viterbi architecture is divided into two approaches for measuring both

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area and power consumption. By using these approaches we should minimize the efficiency of degradations. After this process the signature based approach is followed to get the acceptable efficiency and in the same way to detect the errors that is permanent and transient errors we should use the encoded operands. Now to detect errors in the ACS we use the variants which are recomputed with shift operations (RESO).In the same way to get the less faults we use the recomputed with rotated operands. In the proposed Viterbi algorithm architecture we use the redundancy techniques. At last we conclude this proposed system in three contributions which are given below

- At first we proposed an error detection method for the proposed Viterbi decoder. By using this detection technique we can get high error coverage as well as the performance also boosted. Signature based approaches are used to recomputed the encoder operands.
- Now the proposed error detection technique is simulated and results are obtained in the bench marking. In bench marking we can observe the results of our simulation and reliability of our proposed structure.
- At last the proposed error detection Viterbi decoder is implemented on the application specific integrated circuit and field programmable gate array. From the results we can observe that the proposed architecture is used reliably.

II.EXISTED SYSTEM

In the existed system, the error detection carry-select-add (CSA) and pre-computed CSA (PCSA) architectures are designed through recomputing with encoded operands. Since this approach consider more number of cycles for completion, to alleviate the throughput degradation, the architecture is pipelined. Initially, pipeline registers are added to sub-pipeline the architectures, assisting in classifying the timing into sub-parts. The original operands are fed in during the initial cycle. During the second cycle, the second half of the circuit operates on the original operands and the initial half is fed in with the rotated operands.

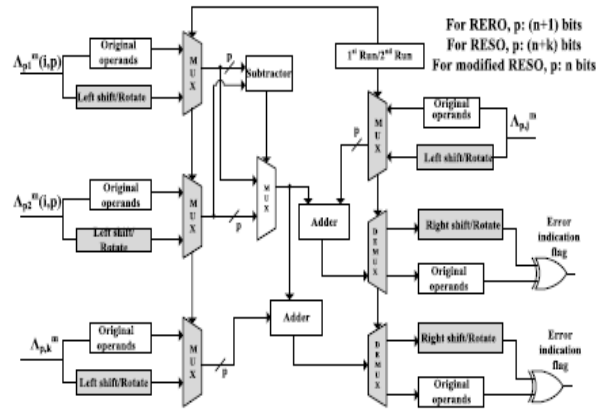

Fig 1. Recomputing with encoded operands for CSA

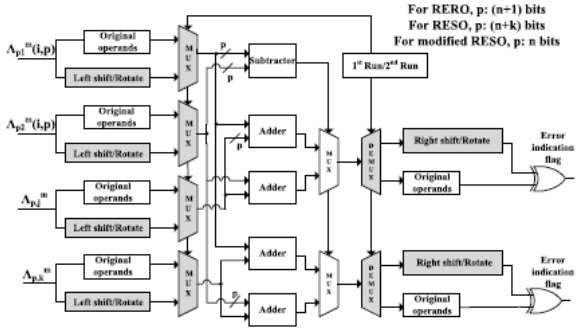

Fig 2. PCSA error detection through recomputing with encoded operands.

Both CSA and PCSA units contain four inputs and each of them is passed in its original form and in the left shifted or rotated form to one of the multiplexers. If the select lines of these multiplexers are set to the initial run, without any change the original operands are passed. If these are set to second run, the second operands are passed.

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For the CSA unit, the inputs are given to the subtractor and also to the multiplexer whose select line is set by the comparator. This performs as the design of compare-select unit. The output of the multiplexer is replicated and asserted as one of the inputs to two adders which are involved in the design. The outputs of both of the adders are the outputs of the CSA unit. These are passed through the demultiplexers and the outputs of the demultiplexers are compared using an XOR gate, and the error indication flag is raised in case of an error.

For the PCSA unit, the first two inputs are fed to the comparator which acts as the select line for the two multiplexers driven by the four adders used in the design. The other two inputs in combination with the previous inputs are given to the adders. The outputs of the two multiplexers are the outputs of the PCSA unit and to secure that they are error-free, the outputs are passed through separate demultiplexers. We have utilized RESO that performs the recomputation step with shifted operands that is all operands are shifted left or right by *k* bits.

III.PROPOSED SYSTEM

The input bits are provided with the (Linear Feedback Shift Register) LFSR process. An LFSR is a linear feedback shift register, when clocked; the signal is advances, through the register from one bit to the next most-significant bit. The outputs are combined in configuration of exclusive-OR to produce a feedback mechanism. A linear feedback shift register (LFSR) can be attained by accomplishing exclusive-OR on the outputs of two or more of the flip-flops which are together and feeding those outputs back into the input of one of the flip-flops.

The message bits are provided with Cyclic Redundancy Check (CRC) generation. It is the one powerful error-detection method which is a generalization of parity checking. One appends a few bits to the end of the bit string for a message and sends out the extended string.

The receiver then executes a computation which is yield 0 if bits of the message had been not in error; if the result is not 0, then the receiver realize that there has been an error in one or more bits.

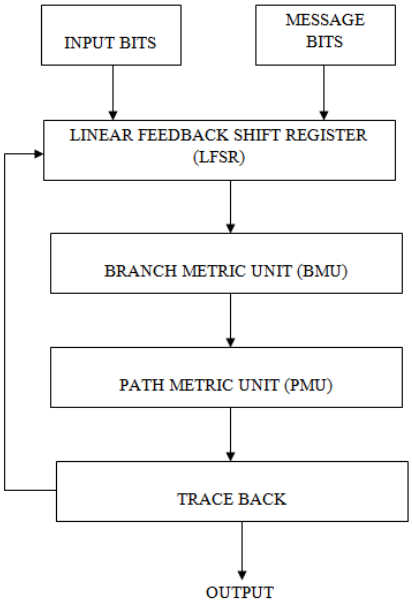

FIG 3. PROPOSED SYSTEM

The proposed adaptive viterbi algorithm are as follows:

1) Branch metric computation.

2) State metric update: Update the state metric by utilizing the modern branch metric.

3) Survivor path recording: At each node tag the surviving path.

4) Output decision generation: Generation of the output sequence which is decoded is depends on the survivor path information. Analog signals are quantized and converted which depends into

digital signals in the quantization block. The frame boundaries of code words and symbol boundaries are detected by synchronization block. We assume that a proposed decoder receives parallel successive code symbols, in which the boundaries of the symbols and the frames have been identified.

A. Branch Matrix Unit: It is utilized to generate branch metrics, which are hamming distances of input data from 00, 01, 10 and 11. The BM unit is utilized for measuring branch metric for trellis branches from the input data. We select the absolute difference as measure for branch metric. These branch metrics are viewed as the weights of the branches.

B.ACS (Add Compare Select) Unit: The state metrics modern value has to be determined at each time instant. For every clock cycle the state metrics should be updated. Because of recursion, pipelining, a frequent approach is to increase the throughput of the system which is not applicable. The Add-Compare-Select (ACS) unit is the module which consumes the high power and area. In order to obtain the required precision, a resolution of 5 bits for the state metrics is essential, while 5 bits are needed for the branch metrics. Since the state metrics are positive numbers always and only positive branch metrics are combined to them, the accumulated metrics grow indefinitely without normalization.

C. Survivor Management Unit (SMU): This is responsible for keep track of the information bits which are related with the surviving paths. The designation is done by the path metric Calculation.

There are two basic design approaches: Register Exchange and Trace Back. In both techniques, a shift register is related with every trellis node throughout the operation of decoding.

Since one of the major benefits is the low power design. By utilizing the trace back approach the proposed decoder has been implemented which dissipates the low power.

D. Path Metric Unit (PMU): It computes the partial path metrics at each node in the trellis. A path metric unit summarizes branch metrics to get metrics for paths, where K is the constraint length of the code, one of which can eventually be chosen as optimal. Every clock it makes decisions, throwing off wittingly non-optimal paths. The results of these decisions are written to the memory of a trace back unit. The core elements of a PMU are ACS (Add-Compare-Select) units. The way in which they are connected between themselves is defined by a specific code's trellis diagram.

Since branch metrics are always , there must be an additional circuit preventing metric counters from overflow (it isn't shown on the image). An alternate method that eliminates the need to monitor the path metric growth is to allow the path metrics to "roll over"; to use this method it is necessary to make sure the path metric accumulators contain enough bits to prevent the "best" and "worst" values from coming within $2^{(n-1)}$ of each other. The compare circuit is essentially unchanged.

It is possible to monitor the noise level on the incoming bit stream by monitoring the rate of growth of the "best" path metric. A simpler way to do this is to monitor a single location or "state" and watch it pass "upward" through say four discrete levels within the range of the accumulator. As it passes upward through each of these thresholds, a counter is incremented that reflects the "noise" present on the incoming signal.

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E. Trace Back Unit (TBU): Back-trace unit restores an (almost) maximum-likelihood path from the decisions made by PMU. Since it does it in inverse direction, a viterbi decoder comprises a FILO (first-in-last-out) buffer to reconstruct a correct order.

IV.RESULTS

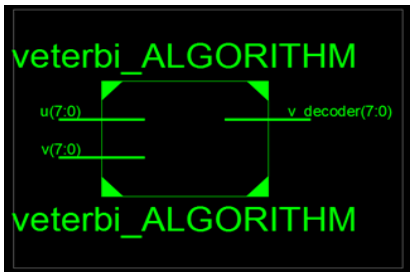


FIG 4. RTL SCHEMATIC

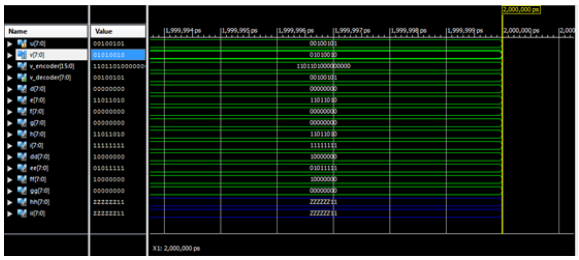
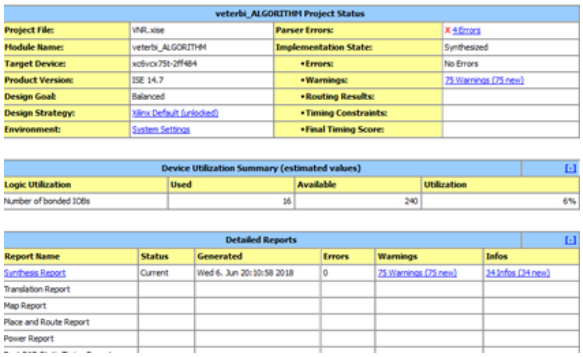


FIG 5. OUTPUT



veterbi_ALGORITHM Project Status			
Project File:	VNR.xise	Parser Errors:	X 4 Errors
Module Name:	veterbi_ALGORITHM	Implementation State:	Synthesized
Target Device:	xc6vcx75t-2ff484	•Errors:	No Errors
Product Version:	ISE 14.7	•Warnings:	75 Warnings (75 new)
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of bonded IOBs	16	240	6%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed 6. Jun 20:10:58 2018	0	75 Warnings (75 new)	34 Infos (34 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					

FIG 6. REPORT

V. CONCLUSION

In this paper, a high speed implementation of an adaptive Viterbi decoder is presented. In digital communication channels, error-correcting codes utilization has achieved to be an effective way for overcome data corruption. Power and area has been decreased by classifying the Trellis Coding structure into two segments. Significant amount of power has been reduced in the design by modifying branch metric architecture. The proposed work can be extended for soft decision based adaptive Viterbi decoder that suitable for multiple quantization level by modifying Branch metric computation unit.

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