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Design an Efficient Fault Tolerant Kogge Stone Adder

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ABSTRACT: Adder is one of the basic arithmetic operation. Currently implementing a high speed VLSI style could be an important topic and as adders are utilized in various fields of applications, coming up with a high speed adder is one among the necessary facets. To increase the speed in DSP processor Parallel prefix adder is used. In this paper we designed and enforced a high speed Kogge Stone parallel prefix adder. KSA is a parallel prefix adder and it is the form of carry look ahead adder. This is the fastest adder and it is used the industry for high performance arithmetic circuits. In KSA, carries are computed fast by computing them in parallel at the cost of increased area. We simulate and synthesis kogge stone adder by using Xilinx ISE tool.

KEY WORDS: Parallel prefix adder, digital signal processor, kogge stone parallel prefix adder.

I.INTRODUCTION

In microprocessor, digital signal processor, especially in digital computers, addition plays crucial role to perform arithmetic operations and it is a basic building block. Here to implement the athematic unit, the binary adder structures become a very critical hardware unit. There are large number of different circuit architectures with different performance characteristics to perform athematic operations. But in this the researches mostly deals with the binary adder structures which are based onthe studies of their comparative performance analysis.

In this paper, qualitative evaluations of the classified binary adder architectures are given. To reduce the supply voltage effective techniques are being used.
Supply voltage is increaseddue to quadratic dependence of the switching energy on the voltage. So the subthreshold current is the main leakage component in OFF devices and it has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect. The operation of ON devices may reside in the superthreshold, near-threshold, or subthreshold regions based on the reduction of supply voltage. Compared with the near/sub threshold regions the superthreshold region provides us with lower delay and higher switching and leakage powers.

The logic gate delay and leakage power produces exponential dependences on the supply and threshold voltages in sub threshold region. But In Nano scale technologies these voltages are potentially subject to process the environmental variations. Due to this variations are increased in the region. In addition, the small subthreshold current causes a large delay for the circuits operating in the subthreshold region.

Recently, the near-threshold region has been considered as a region that provides a more desirable tradeoff point between delay and power dissipation compared with that of the subthreshold one, because it results in lower delay compared with the subthreshold region and significantly lowers switching and

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leakage powers compared with the superthreshold region. In addition, near-threshold operation, which uses supply voltage levels near the threshold voltage of transistors, suffers considerably less from the process and environmental variations compared with the subthreshold region.

The CSKA structurewill reduces the delay by modifying and depending up on the static CMOS logic it is implemented. Byoperating the circuit under a wide range of supply voltages in highly scaled technologies the CMOS will be originated. The existed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA.

II.EXISTED SYSTEM

From below figure (1) we can observe the architecture of existed system. In the below architecture they are chain of full adders (FAs), RCA block and 2:1 multiplexer (carry skip logic). Coming to the RCA block, it is connected with each other through 2:1 multiplexers and placed on the one or more level structures. The entire CSKA configuration depends up on the speed of the adder. To find the optimum number of the variables, various number of methods are introduced. To minimize the delay of adders based on a singlelevel carry skip logic, various techniques are used. Basically, to increase the speed, multilevel CSKAs are existed in the system. But this techniques will increase the area and power considerably and occupies less regular layout. Variable sizes are suggested in the design of a static CMOS CSKA.

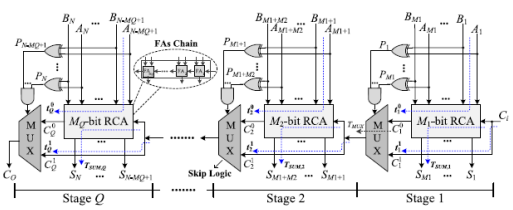

Fig. 1. Existed system

In addition, to lower the propagation delay of the adder, in each stage, the carry look-ahead logic is utilized. Again, it had a complex layout as well as large power consumption and area usage. In this paper, the design approach is presented only for the 32-bit adder and it is not general to be applied for structures with different bits lengths. Alioto and Palumbo proposes the design of a single-level CSKAdepending upon the VSS technique and skip time. Here the near-optimal numbers of the FAs are determined based on the VSS technique and skip time.The ripple time means the time required by a carry to ripple through a FA. The main intent of this system is to decrease the critical path delay. But this system increases the delay and as well as errors also occurred. So a new system is proposed to decrease the delay and reduce the errors which is discussed in below section.

III. PROPOSED SYSTEM

The below figure (2) shows the block formation of proposed system. The addition of RCA in the lower half makes it possible to use similar testing methodology as used in TMR-RC adder. In order to detect error in any of the RCA, two Test RCA are included as shown in the Figure (2).Some multiplexers and a bit counter are also added for fault detection and correction. During each input clock cycle one of the four RCA (RC0 – RC3) is selected for testing. The corresponding carry input and the operand A and B are routed to both Test RCA by a multiplexer. The selection of a RCA is controlled by a 2-bit counter. Due this even if one of the selected RCA becomes faulty, the correct output is available at the comparator output.

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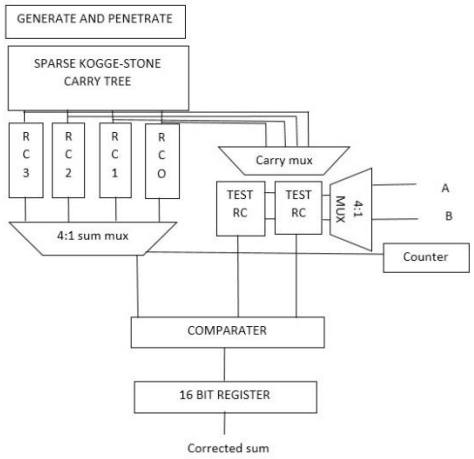

Fig. 2. Proposed system

The desig correct error only if any one of the RCA becomes faulty as the clock signal to the bit counter is stopped if the fault is found in any of the RCA. In order to correct the errors in more than one RCA a 16-bit register is added to the design which holds the sum output from the comparator. For each count value starting from 00 to 03 of a bit counter a corrected sum from the comparator is stored in the register. Thus allowing error correction in case more than one RCA becomes faulty. The improvement introduced in the proposed design is the reduction in the error recovery time which is very critical in any fault tolerant circuit. As the corrected sum output is available in the register after all the RCA are tested the final sum output can be sampled from the register and no extra clock cycles are required to correct error after fault detection as required in the design proposed. From below figure (3) we can observe the architecture of kogge-stone adder. So the final design is coded in verilog and simulated using ISim.

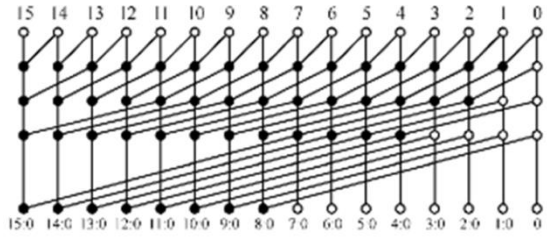

Fig. 3. Kogge stone adder architecture

IV.RESULTS

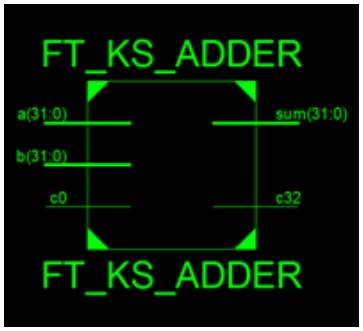

Fig. 4. RTL schematic

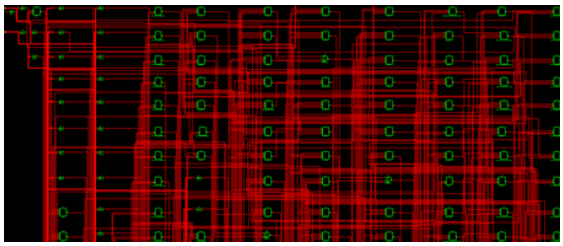

Fig. 5. Technology schematic

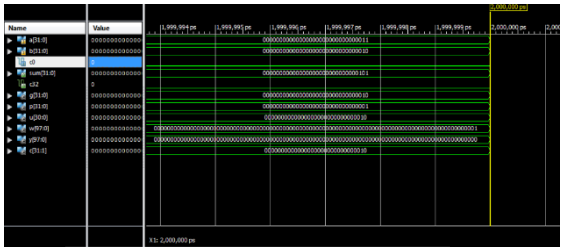

Fig. 6. Output

The primary objective of this paper is to design, implement and analyses the performance of 32-bit Kogge-Stone Adder. The performance analysis was based on the power consumption and the worst case delay in performing the operation.. This paper gives better result than other adder apart from that it gives less area and low propagation delay. In future this adder can be helped to design a high speed multiplier which is essential for digital processor.

VI. REFERENCES

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