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Design a High Speed and Energy Efficient Novel FFT Using CSKA

[1] GARLAPATI SRAVANTHI, [2] SHAIK KHAMURUDDEEN
[1]M.tech-Scholar, Dept of ECE, KKR & KSR Institute of Technology and Sciences, Guntur, A.P.
[2]Associate Professor, Dept of ECE, KKR & KSR Institute of Technology and Sciences, Guntur, A.P.

ABSTRACT: ***The DFT (Discrete Fourier Transform) is a significant technique in the fields such as Telecommunications and Digital Signal Processing (DSP). An efficient algorithm for enumerating the DFT and its inverse is Fast Fourier Transform (FFT). The FFT processor plays a key role in the field of communication systems such as Digital Video or Audio Broadcasting, Wireless LAN with Standards of IEEE 802.11, High Speed Digital Subscriber Lines etc. The existed structure utilizes AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) compound gates for the skip logic. The existed system is complex in area. Hence, we propose an algorithm which is area efficient and consumed delay in previous algorithm. The proposed design is implementation in Xilinx software.***

KEY TERMS: ***Single Path Delay Feedback (SDF), Serial in Serial out Shift Register, Fast Fourier Transform (FFT), CSKA, Folding Technique.***

I. INTRODUCTION

The Fourier Transform is an inevitable approach in signal processing. The Discrete Fourier Transform decomposes a set of values into different components of frequency. The Fast Fourier transform (FFT) is an appropriate technique to do manipulation of DFT. The algorithm of FFT was devised by Cooley and Tukey in order to decrease the amount of complexity with respect to time and computations.

The hardware of FFT can be implemented by two types of classifications- memory architecture and pipeline architecture. The memory architecture comprises a single processing element and various units of memory.

The merits of memory architecture include low power and low cost when compared to that of other styles. The specific demerits are greater latency and lower throughput. The above demerits of the memory architecture are totally eliminated by pipeline architecture at the expense of extra hardware in an acceptable way.

The various types of pipeline architecture include Single delay feedback (SDF), Single delay commutator (SDC) and multiple delay commutator (MDC). The pipeline architecture is a regular structure which can be adopted by using hardware description language in an easy manner. In the recent years, the communication systems need to transmit voice and video signals of high quality in an efficient manner. In present day the efficient module is a high speed, reliable technology of communication. The algorithms of FFT can be grouped into fixed-radix, mixed radix and split radix algorithms in a rough manner. The basic categories of algorithms of FFT include - Decimation infrequency (DIF) and the Decimation-in-time (DIT) as shown in Figure 1.

Both of these algorithms depend on disintegration of transformation of an N-point sequence into many subsequences in

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a successive manner. There is no major difference between them as far as complexity of computation is concerned. Generally DIT deals with the input and output in reverse sequence and normal sequence respectively, while DIF deals with input and output in normal sequence and reverse sequence respectively. Only Decimation-in-frequency (DIF) algorithm will be taken into consideration.

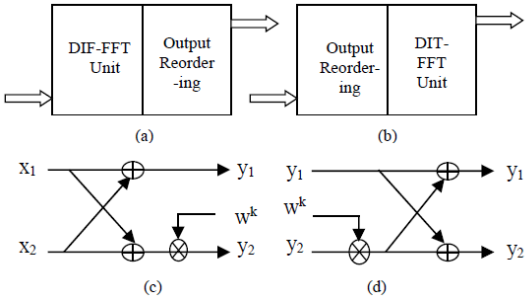

Figure 1: (a) DIF FFT processing (b) DIT FFT processing(c) DIF FFT butterfly (d) DIT FFT butterfly

II.EXISTED SYSTEM

The existed structure is depends on uniting the incrementation and the concatenation schemes with the Conv-CSKA structure, and hence, it is indicated as CI-CSKA. The existed hybrid variable latency CSKA structure is exhibit in below figure 2.

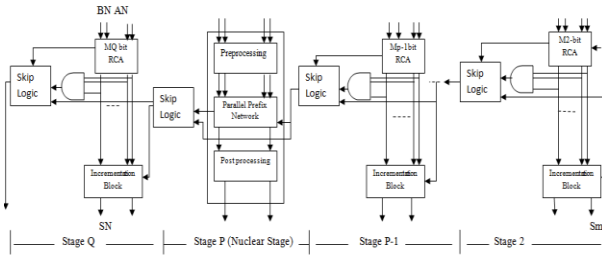

Fig 2. The structure of the existed hybrid variable latency CSKA

It gives us with the ability to utilize simpler carry skip logics. The logic utilized is AOI/OAI compound gates which replaces 2:1 multiplexers. The gates, which contain fewer transistors, have lower area, delay and less power consumption when compared with the 2:1 multiplexer. Hence, in this existed structure, through the skip logics, the carry propagate so, it becomes more complemented. Therefore, the complement of the carry is generated at the skip logic output of even stages.

The existed structure has a less propagation delay with a slightly less area. Hence, while the AOI (or OAI) gate power consumptions are smaller than that of the multiplexer, the existed CI-CSKA power consumption is a little more than that of the conventional one. This is because of the maximize in the number of the gates, which imposes a higher wiring capacitance.

III.PROPOSED SYSTEM

Proposed method are used in binary input is going to the serial input serial output (SISO) shift register as shown in Figure 3. In proposing algorithm consist of SISO, and carry skip adder (CSKA), adder, Subtractor, Single path Delay Feedback (SDF) Pipeline, Folding architecture. SISO: - SISO technique depends on the binary input. Suppose the binary input of the system is 8 word length, then eight delay flip flops are utilized in SISO register.

The algorithm specifies that all possible AND terms are created white cell and all possible NAND terms are created gray cell. The white cell consists of full adder

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and AND gate, but the gray cell consists of full adder and NAND gate.

Complex multiplication is consisting of 4 multiplications, 2 adders and 1 subtraction. But in the proposed complex multiplication is consisting of 3 multiplications, 1 adder and 1 subtraction in shown in figure 4.

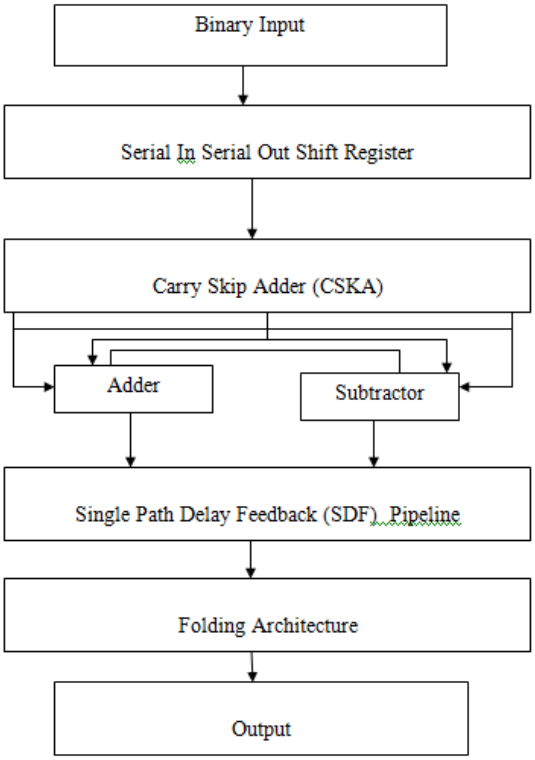

Figure 3: Flow Chart of Proposed Algorithm

Subtractor: Subtractor is consist of half subtractor and full subtractor depends on word length in proposed algorithm.

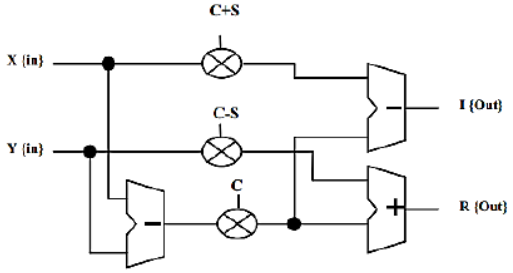

Figure 4: Block Diagram of Complex Multiplication

Single-path Delay Feedback Pipeline Architecture:- Herbert L. Groginsky and George A. Works introduced a feedback mechanism in order to minimize the number of delay elements. In the proposed architecture, when the data of input are instantly sent to the butterfly one half of outputs from each stage are fed back to the input data buffer.

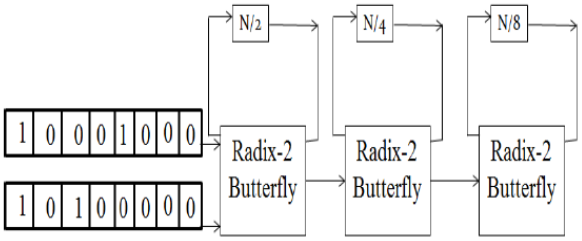

Figure 5: Flow Graph of the Radix-2 SDF Pipeline Architecture

Folding Architecture: Folding is a transformation technique which is utilizing in DSP architecture, implementation for reducing the number of functional blocks in synthesizing DSP architecture. In 1992, Folding was first implemented by Keshab K. Parhi and his students.

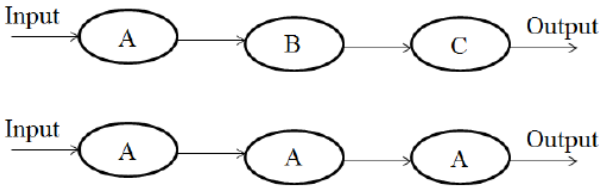

Figure 6: (a) Without folding technique (b) With folding technique

IV.RESULTS

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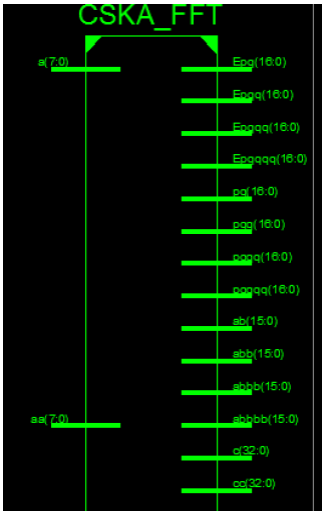

Fig 7: RTL Schematic Diagram

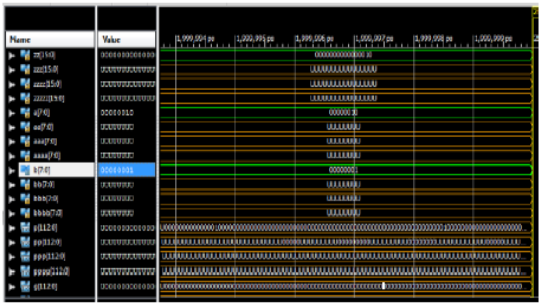

Fig.8 Input Waveform Of FFT

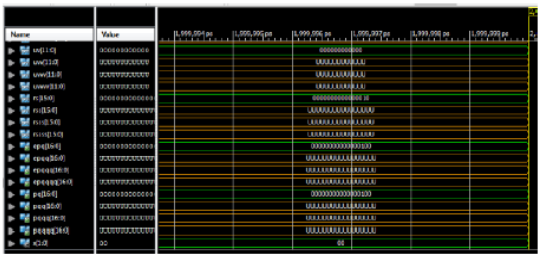

Fig 9: Output Waveform Of FFT

V. CONCLUSION

This paper has reported two efficient VLSI architectures of DIT-FFT. Both proposed architectures are designed for complex inputs with a data width of 16 bits, maintained constant all along. The simulation outputs of proposed architectures have not shown much deviation from numerical values. But, proposed architecture utilizing Radix-2 algorithm has high memory usage and also has huge number of arithmetic operations which causes the delay to be maximum as the signal length increases; this drawback has been overcome in the later VLSI architecture using Radix FFT Algorithm. This research work involved the implementation of a low delay and area efficient pipelined FFT processor using radix-2 algorithm.

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