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Improved 32-Bit Radix-16 Booth Multiplier Based On Partial Product Dynamic Accuracy Configurable Multipliers

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ABSTRACT: A dual quality 4:2 compressors is proposed in this paper.This compressors will switches between two operating modes they are exact and approximate operating modes.Higher speeds and lower powerconsumptionsare obtained from the compressor at low cost. In approximate mode, compressors has its own level of accuracy and different delays and power dissipations.In this the accuracy changes dynamically, because the multiplier provides particular configuration. The efficiencies of these compressors is evaluated in 32-bit Dadda multiplier. Compared to existed system effective results are obtained in proposed system.

KEY WORDS: 4:2 compressor, accuracy, approximate computing, configurable, delay, and power.

I.INTRODUCTION

Among different arithmetic blocks, the multiplier is one of the main blocks, which is widely used in different applications especially signal processing applications. There are two general architectures for the multipliers, which are sequential and parallel.

While sequential architectures are Low power, their latency is very large. On the other hand, parallel architectures (such as Wallace tree and Dadda) are fast while having high-power consumptions. The parallel multipliers are used in high-performance applications where their large power consumptions may create hot-spot locations on the die. Since the power consumption and speed are critical Parameters in the design of digital circuits, the optimizations of these parameters for multipliers become critically important. Very often, the optimization of one parameter is performed considering a constraint for the other parameter. Specifically, achieving the desired performance (speed) considering the limited power budget of portable systems is challenging task.

In addition, having a given level of reliability may be another obstacle in reaching the system target performance. To meet the power and speed specifications, a variety of methods at different design abstraction levels have been suggested. Approximate computing approaches are based onachieving the target specifications at the cost of reducing the computation accuracy. The approach may be used for applications where there is not a unique answer and/or a set of answers near the accurate result can be considered acceptable. These applications include multimedia processing, machine learning, signal processing, and other error resilient computations. Approximate arithmetic units are mainly based on the simplification of the arithmetic units circuits. There are many prior works focusing on approximate multipliers which provide higher speeds and lower power consumptions at the cost of lower accuracies.

Almost, all of the proposed approximate multipliers are based on having a fixed level of accuracy during the runtime. The runtime accuracy reconfigurability, however, is considered as a useful feature for providing different levels of quality of service during the system operation. Here, by reducing the quality (accuracy), the

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delay and/or power consumption of the unit may be reduced.

An approach for achieving this feature is to use an approximate unit along with a corresponding correction unit. The correction unit, however, increases the delay, power, and area overhead of the circuit. Also, the error correction procedure may require more than one clock cycle, which could, in turn, slow down the processing further.

II. EXISTED SYSTEM

The below figure (1) shows the architecture of existed system. The diagram consists of two main parts of approximate and supplementary. Duringthe approximate mode, only the approximate part is exploited while the supplementary part is power gated.

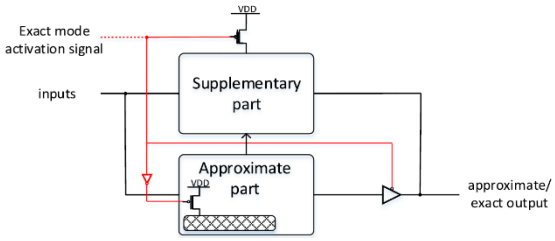

FIG. 1. EXISTED SYSTEM

In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, as is evident from figure (1) in the exact operating mode, tristate buffers are utilized to disconnect the outputs of the approximate part from the primary outputs. In this design, the switching between the approximate and exact operating modes is fast. Thus, it provides us with the opportunity of designing parallel multipliers that are capable of switching between different accuracy levels during the runtime.

Next, we discuss the details of our four DQ4:2Cs based on the diagram shown in figure (1). The structures have different accuracies,delays, power consumptions, and area usages. Note that the *i*th proposed structure is denoted by DQ4:2C*i*. The basic idea behind suggesting the approximate compressors was to minimize the difference (error) between the outputs of exact and approximate ones. Therefore, in order to choose the properapproximate designs for the compressors, an extensive search was performed.

III.PROPOSED SYSTEM

The below figure (2) shows the architecture of proposed system. It shows that the recoding and partial product generation stage including the high level view of the hardware scheme proposed. The way we compute part Bmay still lead to an inconsistencywith the computation of the most significant part of partial product 15. Specifically, when partial product 15 is the result of an odd multiple, a possible carry from the 7 least-significant bits is already incorporated in the most significant part of the partial product. During the computation of part B we should not produce again this carry.

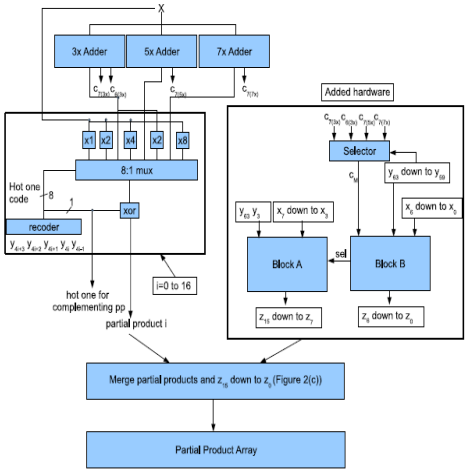

FIG. 2. PROPOSED SYSTEM

For negative odd multiples we use a similar scheme. In this case the output of

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adder is complemented, but the only information available about the carry to position 7 is obtained directly from the adders that generate the positive odd multiple. Next, we show how to obtain the carry to the most significant part of the resultant complemented odd multiple from the carry to position 7 obtained from the adders. The computation of part B may generate two carry outs: the first from the 3:2 carry-save adder (*C*out1), and the second from the carry-propagate adder (*C*out2). To avoid inconsistencies, we detect the carry propagated to the most significant part of the partial product 15 (we call this *CM*) and subtract it from the two carries generated in part B. so from this it can observe that it occupies less area and produces low power consumption.

IV.RESULTS

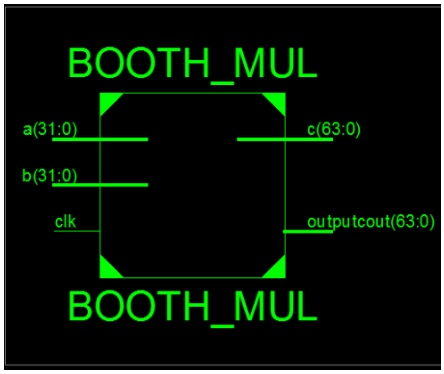

FIG. 3. RTL SCHEMATIC

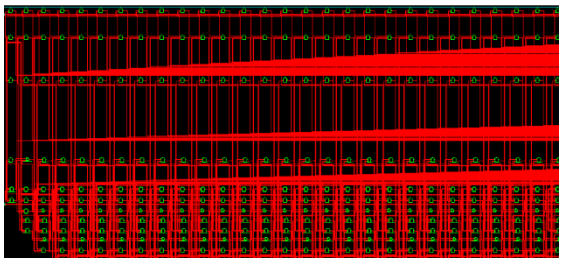

FIG. 4. TECHNOLOGY SCHEMATIC

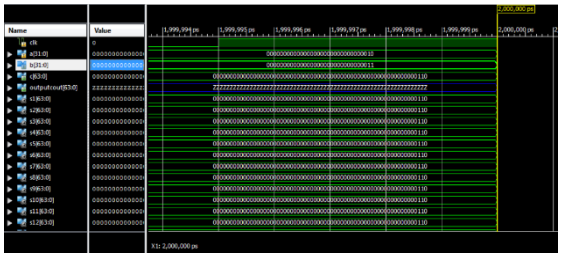

Fig. 5. OUTPUT WAVEFORM

V.CONCLUSION

In this paper, we presented four DQ4:2Cs, which had the flexibility of switching between the exact and approximate operating modes. The compressors provides higher speeds and lower power consumptions at thecost. These compressors were employed in the structure of a 32-bit Dadda multiplier to provide a configurable multiplier. When comparing with non-compressor-based approximate multipliers, the errors of the proposed multipliers were higher while the design parameters were considerably better. Finally, our studies showed that the multipliers realized based on the suggested compressors have, on average, about 93% smaller FOM value compared with the considered approximate multipliers. Whose accuracy (as well as its power and speed) could be changed dynamically during the runtime

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