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Design an Area Efficient CSKA Brent Kung Adder

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ABSTRACT: In this paper we propose aBrent Kung parallel prefix adder.In this carry select adder is used and it provides fast adder which improves the speed of addition. From the proposed structure it is clear that there is a chance to reduce the area.To avoid the high power consumption obtained in the system, a Brent Kung parallel prefix adders is proposed. In the existing adder design, the carry select operation is involved. But it doesn't gives effective results. So the Proposed Adder addition operation offers great advantage inreducing delay.The performance of the reverse converter is based on the target application and existingConstraints.

KEY WORDS: parallel prefix adder, carry select adder, Brent Kung parallel prefix adder.

I.INTRODUCTION

Addition operation is the main operation in digital signal processing and control systems. The fast and accuracy of a processor or system depends on the adder performance.Ripple carry adder is taken generally from the general purpose processors and DSP processors. It is used for the addition operation i.e., if N-Bits addition operation is performed by the N-Bit Full Adder. Basically, the sum and carry will be given to next bit full adder operation. The N-1thBit Full Adder operation carry will be given to the NthBit Full Adder operation present in the Ripple Carry Adder.

Adders are commonly found in the critical path of many building blocks of microprocessors and digital signal processing chips. Its purpose is to form the arithmetic sum of two binary numbers.By using propagation, the quality,Delay, and area is measured.

Instead of waiting for the carry propagation of the first addition, the main idea is to overlap the carry propagation of the first addition and then compute the second addition.Since repetitive additions will be performed by a Multiplierand adder. In multiplication and division, multi operand addition is often encountered. To add more number of numbers together powerful adders should be used. Basically, parallel prefix adder produces high speed multi operands.

Based on the inputs given the outcome of operation is performed. As we know that the parallel prefix adder performs and executes the operation in parallel. The obtained output will be segmented into smaller pieces. There are different topologies used in parallel prefix adder, but the operator is associative. Based on topology the operation is performed..

By using the associative binary operations, the algorithms will be generalized. This generalized algorithms performs certain operations and computed with particular efficiency. Basically there are two procedures followed in the system, they are in first pass the prefix sum as are calculated from the processing unit. And in second pass known prefix values are computed from processing unit to get initial value. So along with that the system performs two read operations and one write operation.

Here a methodology is employed to design fast reverse converters. The experimental results mainly, depends on area, delay, and power consumption. The expenseof additional area and remarkable will increase

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the power consumption.The significant growing of power consumptionmakes the reverseconverter not competitive.

Compared with VLSI implementations, the Brent Kung Parallel-prefix adders will produce performance differently.The modern FPGAs employ the fast-carry chain process to get faster results. The Ladner-Fischer is the Parallel Prefix Adders used to done the addition operation. It is look like tree structure to perform the high speed arithmetic operation. Ladner Fischer Adder is used for high performance addition operation.

II. EXISTED SYSTEM

The Chinese remainder theorem, or other related improved approaches and techniques underlie the RNS reverse conversion,whose formulation can be directly mapped to ripple-carry adders (RCA). However, this leads to significant speed degradation, due tothe linear increase of the delay in the RCA with the number of bits. The delay of RNS reverse converters will bind the growth of logarithm in Brent Kung Parallel prefix adder. Basically, in reverse converters large number of adders will be used. Even when onlyone adder is used, the bit length of this adder is quite large.

To perform the first part of addition in the system, a desired structure with particular operands are used. This operands are fullyvariable, and a RCA with simplified logic to do the second part (fulladder becomes XNOR/OR gates because of the constant operand). High power consumption is obtained due to the recursive effect. Recursive effect is obtained while generating and propagating the signals at prefix level. An optimized approach is proposed which uses an extra prefix level to add theoutput carry. However, this method suffers from high fan-out, whichcan make it usable only for small width operands. However, this problem is eliminated by using additional prefixlevel. In contrastto the BEC, this modified unit is able to perform a conditionalincrement based on control signals as shown in Fig. 1.

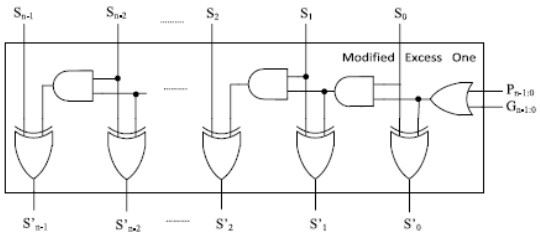

FIG. 1. EXISTED SYSTEM

III. PROPOSED SYSTEM

The Proposed Brent Kung parallel prefix adder will speed up the binary addition. Coming to the structure it looks like tree structure which gives high performance of arithmetic operations. In Ripple Carry Adders each bit wait for the last bit operation. In Parallel Prefix Adders instead of waiting for the carry propagation of the first addition, the idea here is to overlap the carry propagation of the first addition with the computation in the second addition, and so forth, since repetitive additions will be performed by a multioperand adder.

Research on binary operation elements and motivation gives development of devices. Field programmable Gate arrays [FPGA's] are most popular in recent years because they improve the speed of microprocessor based applications like mobile DSP andtelecommunication. Basically, in Brent Kung parallel prefix adder they are three stages which are given asPre-Processing Stage, Carry Generation Stage, and Post-Processing Stage.

The first input bits goes under Pre-Processing Stage and it will produce propagate and generate. Here the process of propagation and generationwill produce the final result as sum. From below figure (2) we can observe the proposed system block diagram.The Efficient Brent Kung parallel prefix Adder structure is looking like tree structure for the high performance of

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arithmetic operations and it is the fastest adder which focuses on gate level logic. It designs with less number of gates.

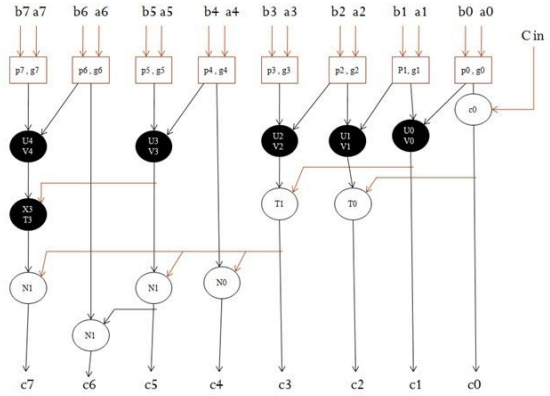

FIG. 2 PROPOSED SYSTEM

So, it decreases the delay and memory used in this architecture.In Efficient Ladner-Fischer Adder, black cell operates three Gates and gray cell operates two Gates. The gray cell reduces the delay and memory because it operates only two Gates. The Proposed Adder is design with the both black and gray cells. By using gray cell operations at the last stage of Proposed Adder gives an enormous dropping delay and memory used.

IV.RESULTS

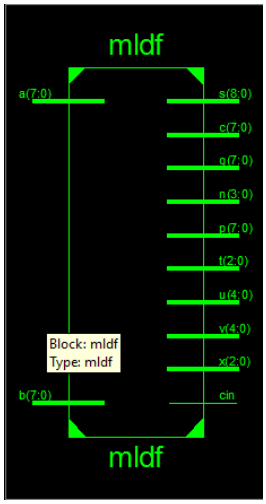

FIG. 3. RTL SCHEMATIC

FIG. 4. TEST BENCH WAVEFORM

V.CONCLUSION

In this paper, a new approach to design an Efficient Brent-Kung Adder concentrates on gate levels to improve the speed and decreases the memory. To speed up the operation of addition, the cells of carry generation stage is decreased. The Proposed Adder addition operation offers great advantage in reducing delay. The future scope is to design 32 Bit Proposed Adder with less number of black cells to improve the area and delay performance of the adders.

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