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Design and Implementation of a Memory-Reduced Turbo Parallel Decoding

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ABSTRACT: Turbo-decoding for the Long Term Evolution (LTE) wireless communication standard is the most challenging tasks in terms of computational complexity and power consumption of corresponding cellular devices. This paper represents a parameterized parallel Turbo decoder for LTE terminals. For supporting the high peak data-rate defined in the forthcoming 3GPP LTE standard, Turbo decoder is needed as a key component of the radio baseband chip. By exploiting the trade-off of precision, speed and area consumption, a Turbo decoder with eight parallel SISO units is implemented to meet the throughput requirement.

Key Words: ASIC implementation, low-power, LTE, parallel turbo-decoder, radix-4, 3G mobile communication.

I. INTRODUCTION

The wireless communication technology which has connected the people all over the World from anywhere anytime is now rapidly growing on demand to achieve high data rate transmissions. To accomplish a reliable channel coding scheme has to be adopted. Turbo codes are one of the high performance channel codes with forward error correction (FEC) provides optimal performance which is approaching the Shannon limit. This scheme is mainly utilized in the digital communication systems where the transmitted signals often get corrupted by noise due to their non-ideal behaviour in realistic communication channels. So, turbo codes are used at the most in long term evolution (LTE) systems. In this paper, the architecture of turbo encoder and turbo decoder are proposed.

The main aim is to reduce the area which is occupied by computational units in decoder block by employing the ACS 4 unit along with MSR (Maximum Shared Resource) architecture by simplifying the computations.

The turbo code is one of the most attractive forward error correction codes, which can provide near-optimal bit error rates (BERs) of Shannon's limit. Due to the fascinating error correcting performance, the turbo codes have been applied to various wireless communication systems. For achieving a high decoding throughput, an aggressive puncturing on long turbo codes is normally defined at the recent wireless standards. The extreme case of 3GPP LTE-advanced specification, for example, necessitates a code length of 6144 bits and a code rate.

To minimize the performance loss in decoding of high rate code words, the next iteration initialization (NII) scheme is widely accepted for the initialization of backward recursions instead of the traditional dummy calculation method . However, the conventional NII technique requires additional memories for storing all of the final backward states of the current iteration, which denote the starting confidence levels of the following

iteration. If the sliding-window technique is used for practical realization, moreover, the number of NII metrics to be stored increases drastically according to the number of window boundaries. More recent research represents a dynamic scaling factor for encoding of NII metrics. However, the previous schemes still require a large amount of storage bits as all of the state metrics have to be collected after an individual compressing process.

During the last few years, 3G wireless communication standards, firmly established themselves as an enabling technology for data-centric communication. The advent of smart-phones, net-books, and other mobile broadband devices finally ushered in an era of throughput-intensive wireless applications. The rapid increase in wireless data traffic now begins to strain the network capacity and operators are looking for novel technologies enabling even higher data-rates.

Recently, the new air interface standard LTE (Long Term Evolution) has been defined by the standards body 3GPP and aims at improving the data-rates by more than 30 in the next few years. LTE specifies the use of turbo-codes to ensure reliable communication. Parallel turbo-decoding is deploying the multiple soft-input soft-output (SISO) decoders operates concurrently, will be the key to achieve the high data-rates offered by LTE. However, the implementation of such will be among the main challenges in terms of computational intensity and power consumption.

II. EXISTED SYSTEM

Conventional Turbo Decoding Architecture is shown in Fig. 1 which describes the generalized turbo decoding architecture based on the soft-input soft output (SISO) decoders. The turbo decoder alternatively processes two decoding phases, i.e., in-order and interleaved phases.

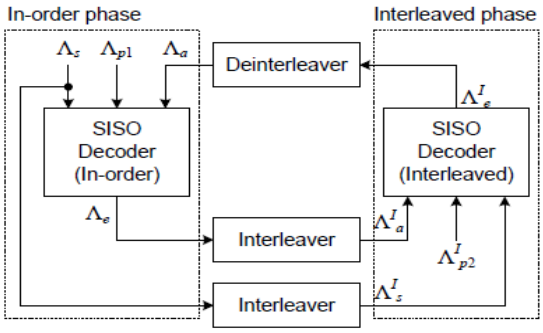

Fig. 1. The generalized turbo decoding architecture

In the figure, the input log-likelihood ratio (LLR) sequences of the systematic bits and parity bits are denoted as Λs (or ΛI s) and Λp1 (or ΛI p2), respectively, where superscript I denotes the sequences related to the interleaved phase. Based on the input LLRs and a priori information Λa (or ΛI a), a SISO decoder generates a posteriori information, i.e., the extrinsic information Λe (or ΛI e), which will be a priori information of the opposite phase after passing through an inter leaver (or deinterleaver). As the two different phases are exclusive in time, only one SISO decoder is normally adopted in practice for realizing the time-interleaved process.

SLIDING-Window Technique with NII Metric Compressions: The sliding-window technique is widely accepted for the recent turbo decoders for reducing the

size of internal buffers. Fig. 2 illustrates the decoding procedure for the n-bit codeword which is associated with sliding windows of w bits. Based on the maximum a posteriori (MAP) decoding algorithm, each sliding window first computes state metrics recursively in forward direction by using the corresponding branch metrics.

For the sake of simplicity, k forward state metrics of the ith trellis step are defined as $\alpha i(0), \alpha i(1), \ldots, \alpha i(k-1)$. Then, as shown in Fig. 2, the backward recursion computes the extrinsic information of each trellis step as well as the next state metrics in backward direction. Similar to the forward state metrics, k backward state metrics of the ith trellis step are represented as $\beta i(0), \beta i(1), \ldots, \beta i(k-1)$.

Before starting the backward recursion, it is important to properly initialize the starting confidence levels of each backward state. To reduce the storage demands caused by the NII scheme, the static encoding method is widely used in the recent turbo decoders.

Compared to the conventional NII scheme, the previous 3-bit static compression reduces the number of storage bits to $6 \times (k-1) \times n/w$. As each NII metric has to be compared with the reference values, hence, the work of additionally requires numerous comparisons. As shown in Fig. 2(b), more precisely, each state metric is compared with six reference values, and the comparison results are used for generating the 3-bit compressed metric at the encoding network. The 3-bit saved NII metrics are read from the NII memory and fed into the recovery network to reconstruct the starting values of backward recursions.

Similar to, the recent work in presents a dynamic scaling algorithm for each NII metric; however, it requires more storage bits as well as the hardware resources to provide an acceptable BER performance, which consumes more power than. Note that the previous works are based on the independent compression of each state metric. As all of the $k-1$ original state metrics have to be encoded and stored to the NII memory, the reduction in memory bits is limited by nature.

III. PROPOSED SYSTEM

The critical path of non-parallel turbo-decoders is usually in the state-metric recursion units, since the associated recursive computations exacerbate pipelining. Corresponding speed-optimized implementations achieve not more than tens of Mb/s. The decoding time per half-iteration must therefore be reduced. To this end, the trellis is divided into trellis segments of equal to length and parallel SISO decoding is carried out in the assigned trellis-segment in parallel fashion. This approach roughly increases the turbo-decoding throughput by a factor of N compared to (non-parallel) turbo-decoders.

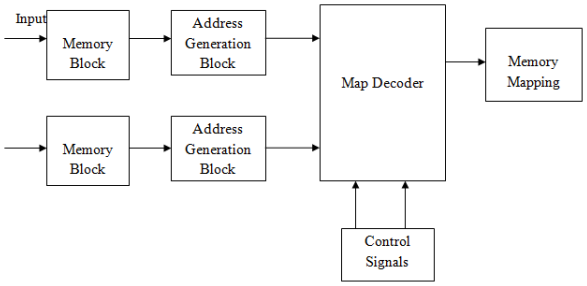

Fig 2. Parallel Turbo Decoder

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The proposed architecture shown in Fig. 2 is based on the (non-parallel) HSDPA turbo-decoder. SISO decoding is operated by alternating between the non-interleaved and interleaved phases which decode the first and second convolutional code, respectively.

The architecture consists of max-log Turbo decoder instances, input memories for the storage of the systematic and parity LLRs, and one intermediate memory for the storage of the extrinsic LLRs. The LTE interleaver contains an address-generator unit for the computation of all interleaved and non-interleaved addresses, and of dedicated permutation networks located at the input and intermediate memories. We note that the use of radix-4 recursions entails 2 increased memory-bandwidth, since the PRPGs associated with even- and odd-numbered trellis-steps are required per clock cycle. To cope with this (potentially) high memory-bandwidth, the following memory architecture is used.

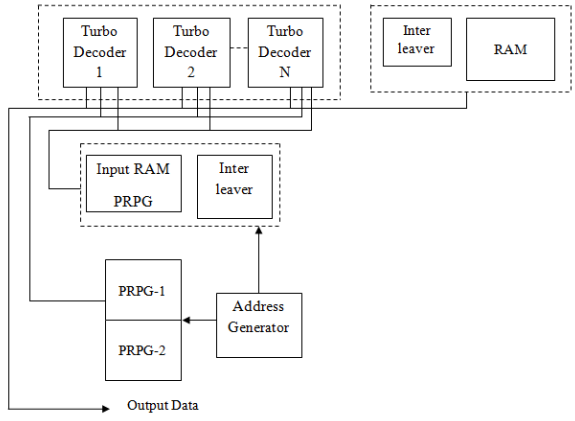

Fig 3. Proposed Architecture

Memory Architecture: The instantiated input and intermediate memories store up to 6144 LLRs in support of the maximum LTE code-block length. Each memory contains Pseudo Random Pattern Generation (PRPG) values per address. When performing radix-2 computations, the systematic, parity 1-and-2, and extrinsic PRPG are stored in separate RAMs. Since access to either the parity-1 or parity-2 PRPG is required (in the non-interleaved or interleaved phase), one single-port (SP) RAM storing both sets of parity PRPG is used to minimize silicon area.

The systematic RAM only requires SP-capability, whereas the intermediate memory requires two-port (TP) capability to provide the required memory bandwidth. The 2 higher memory bandwidth required by radix-4 recursions can be provided by instantiating two RAMs for the systematic PRPGs and two for the extrinsic PRPGs, all providing half the amount of storage. One RAM instance is then used for the PRPGs associated to the even numbered and the other for the odd-numbered trellis-steps. This partitioning enables the 2 X N PRPGs to be read per clock cycle. Note that splitting of the parity RAM can be avoided by storing the two sets of PRPGs for and K – 1 per address.

IV. RESULTS

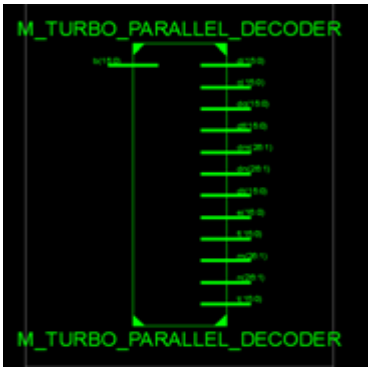

Fig 4. RTL Schematic

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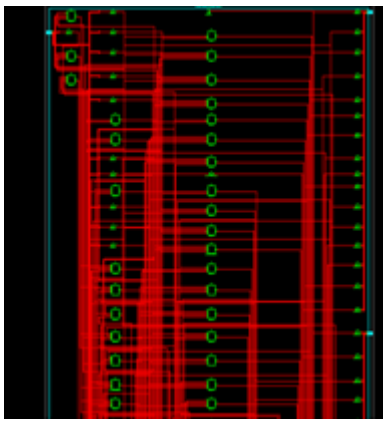

Fig 5. Technology Schematic

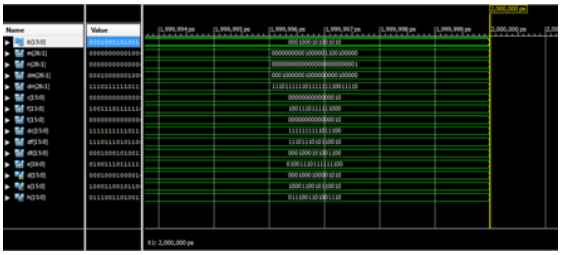

Fig 6. Output

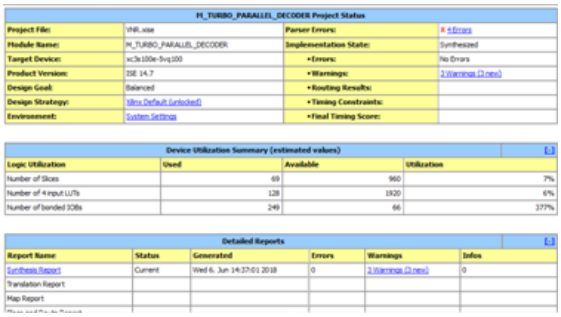

Fig 7. Report

V. CONCLUSION

In this paper, we detailed the design of a parallel turbo-decoder for the 3GPP-LTE standard. The analysis of the throughput/area tradeoffs associated with parallel turbo-decoders have shown that radix-4 in combination with eight Turbo decoder instances are necessary for the LTE peak data-rate. Parallel and interleaved access for the memories at high throughput was achieved through the development of a master-slave Batcher network. Optimizations in the radix-4 turbo decoder unit finally led to a high-performance and low-area turbo-decoder architecture. Additionally, for setting a record in turbo-decoding throughput, both ultra low-power and cost-effectiveness have been demonstrated by the presented implementation concept.

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